

Apple
SoC

Process Analysis Report

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Device Summary Sheet

Manufacturer: Apple Inc.

Part Number: [REDACTED]

Date Code: [REDACTED]

IC Type: SoC

Technology synopsis

Package Type: InFO PoP

Pin Count: 1523

Package Size: 13 mm x 17.3 mm x 0.9 mm

Die Count: 5. One Apple [REDACTED] processor die and four [REDACTED] SDRAM dice

[REDACTED] Processor Die Size: 8.61 mm x 12.75 mm (by edge of physical silicon)
8.57 mm x 12.54 mm (by edge of seal)

[REDACTED] SDRAM Die Size: 8.03 mm x 4.28 mm (by edge of physical silicon)
8 mm x 4.24 mm (by edge of seal)

[REDACTED] SDRAM: 50 um

Die Thickness

[REDACTED] Processor Die Thickness: 202 um

Fan-Out Area:

Number of Redistributive layers (RDL):

RDL Stack Thickness in the Fan-Out Area: 40 um

Passive Element Die Thickness:

Passive Element Die Thickness: 65 um

Apple [REDACTED] processor die technology synopsis

Number of Metal Layers: 16. One layer of aluminum interconnect, fifteen layers of copper interconnect, one cobalt local interconnect layer LI1 and one tungsten local interconnect layer LI2
One layer of metal FinFETs

Gate Layer:

Minimum Printed Gate Length: 11 nm

Gate Pitch: 51 nm

Fin Pitch: 27 nm

Fin Height: 55 nm

Fin Width (middle): 7 nm

Device Isolation Type: STI

Source Device



Figure 1. Apple [REDACTED] front



Figure 2. Apple [REDACTED] back

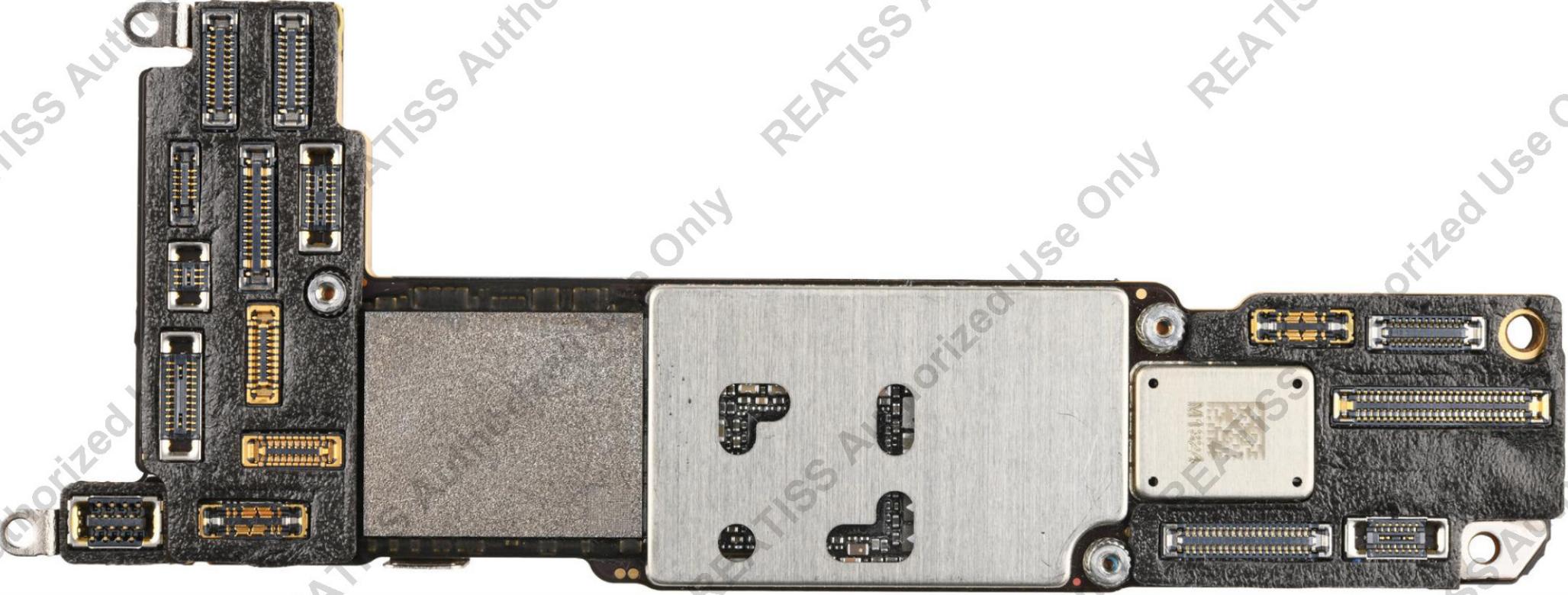


Figure 3. Apple
PCB Assembly front

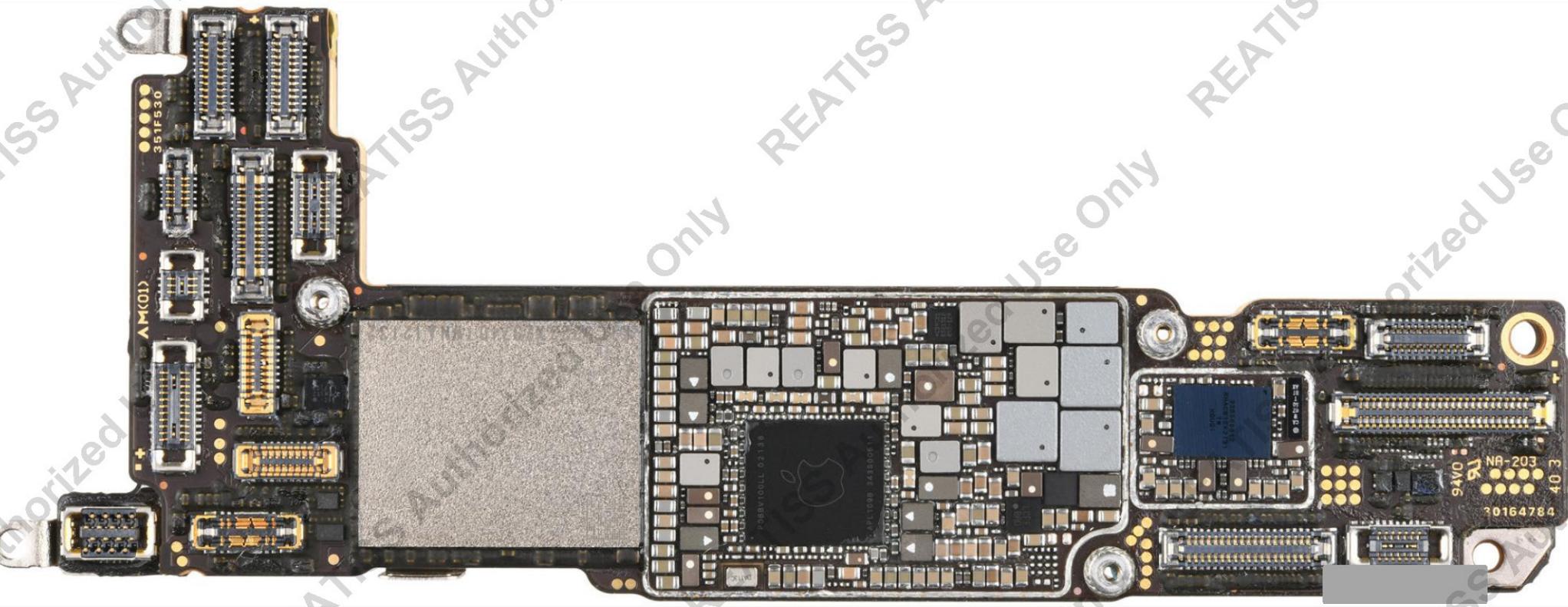


Figure 4. Apple

PCB assembly front with shields removed

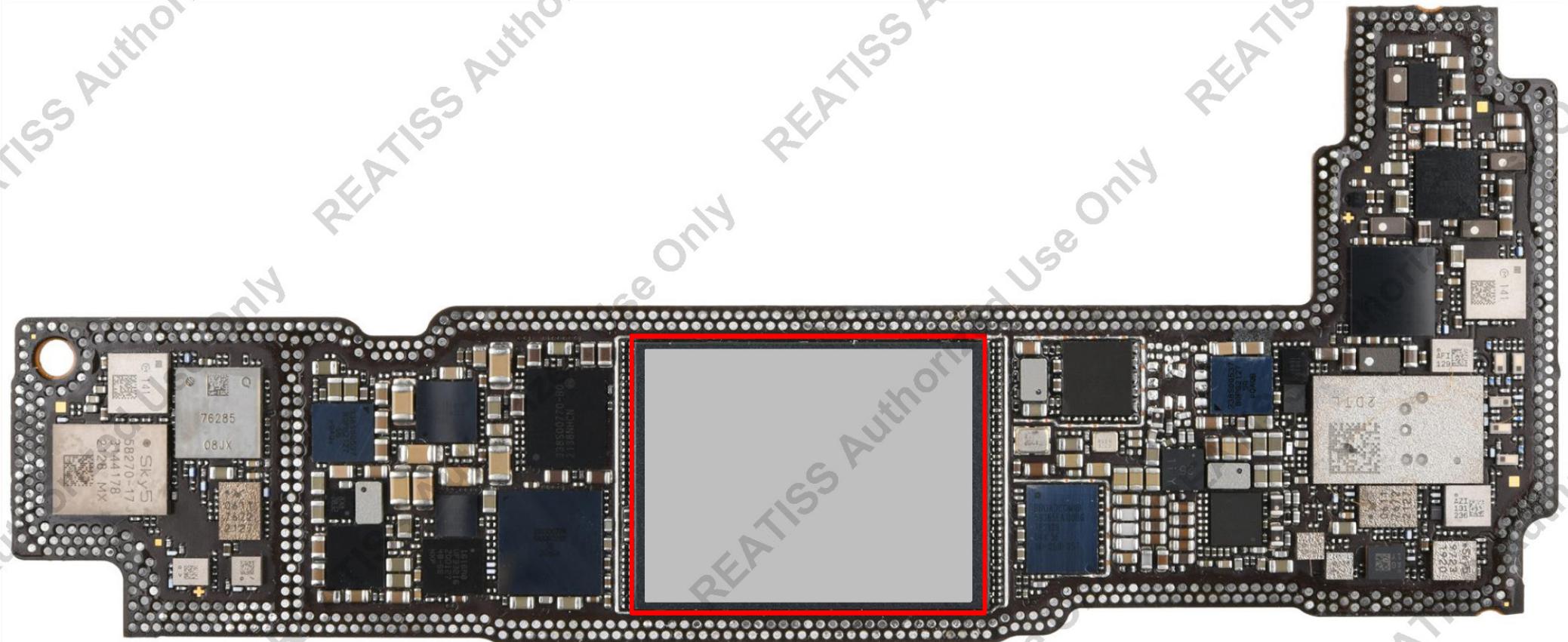


Figure 5. Apple  PCB II Side A



Apple

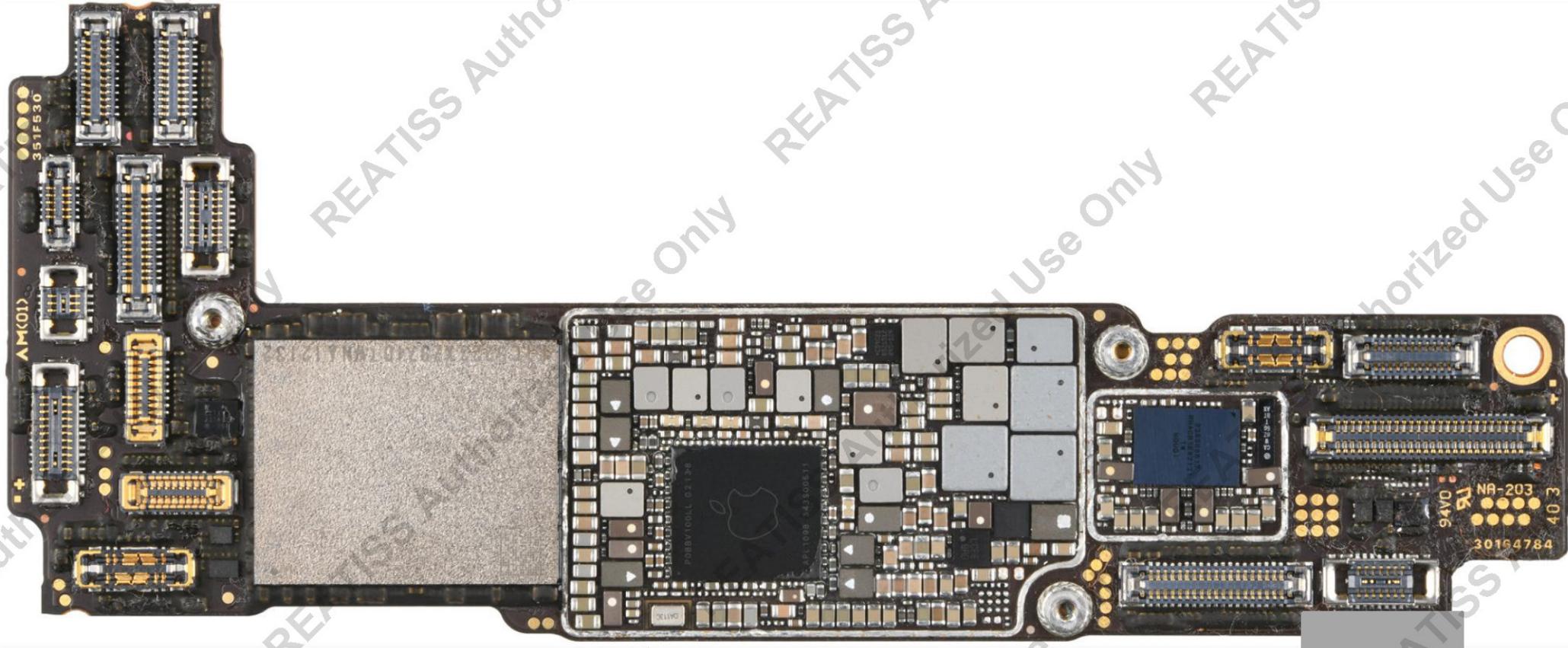


Figure 6. Apple PCB II Side B

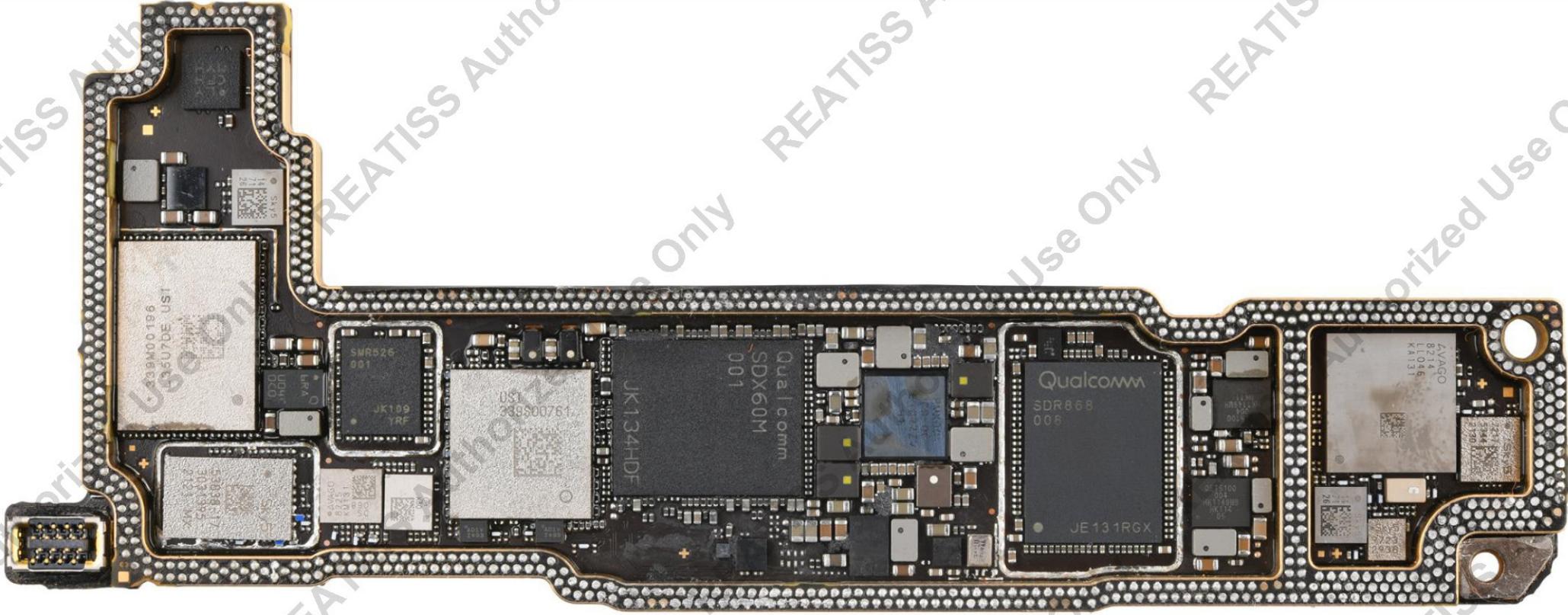


Figure 7. Apple PCB | Side A

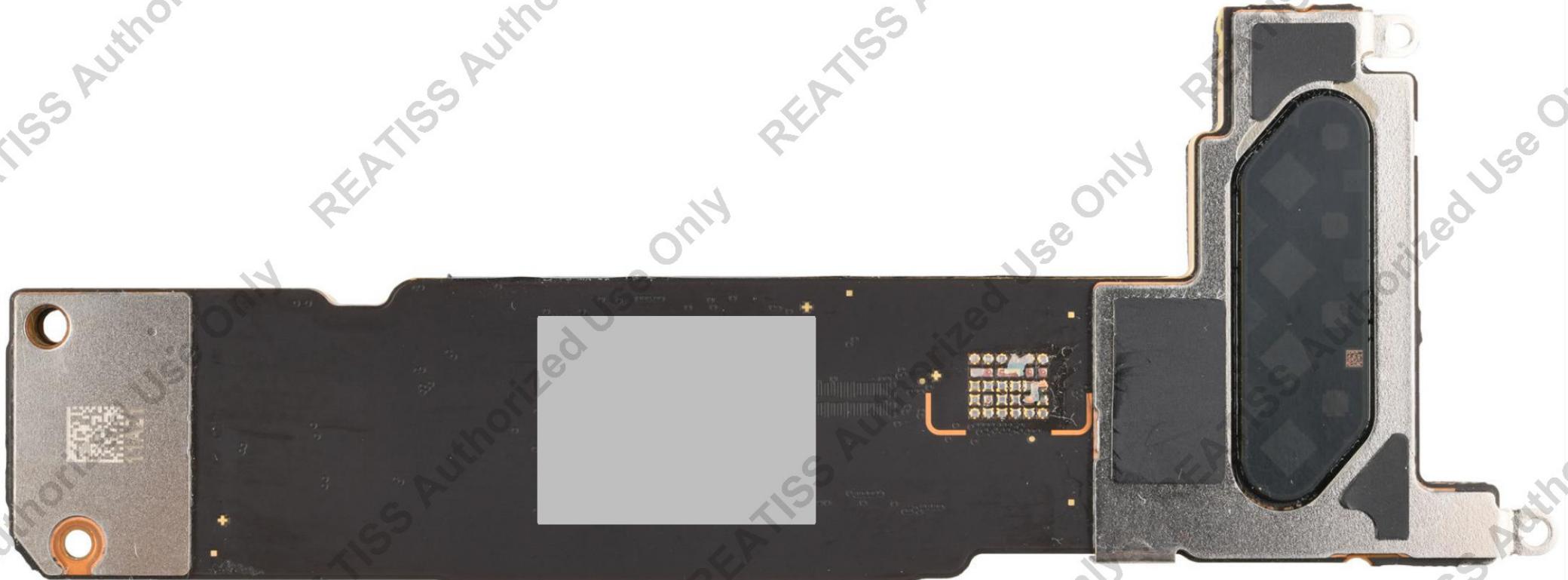


Figure 8. Apple

PCB assembly back (PCB-I Side B)



Figure 9. Apple iPhone 12 Pro Max front



Figure 10. Apple iPhone 12 Pro Max back

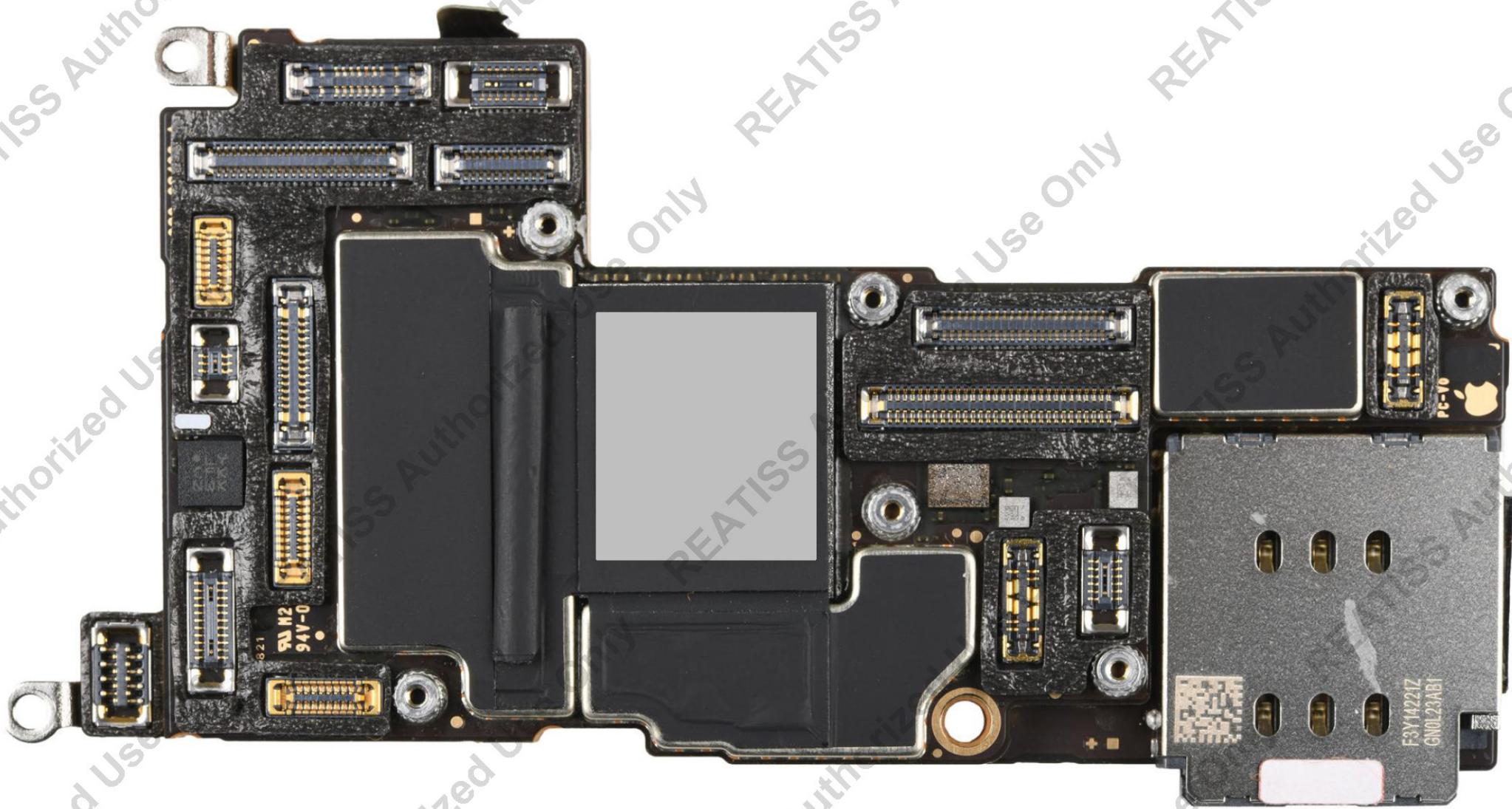


Figure 11. Apple

PCB assembly front

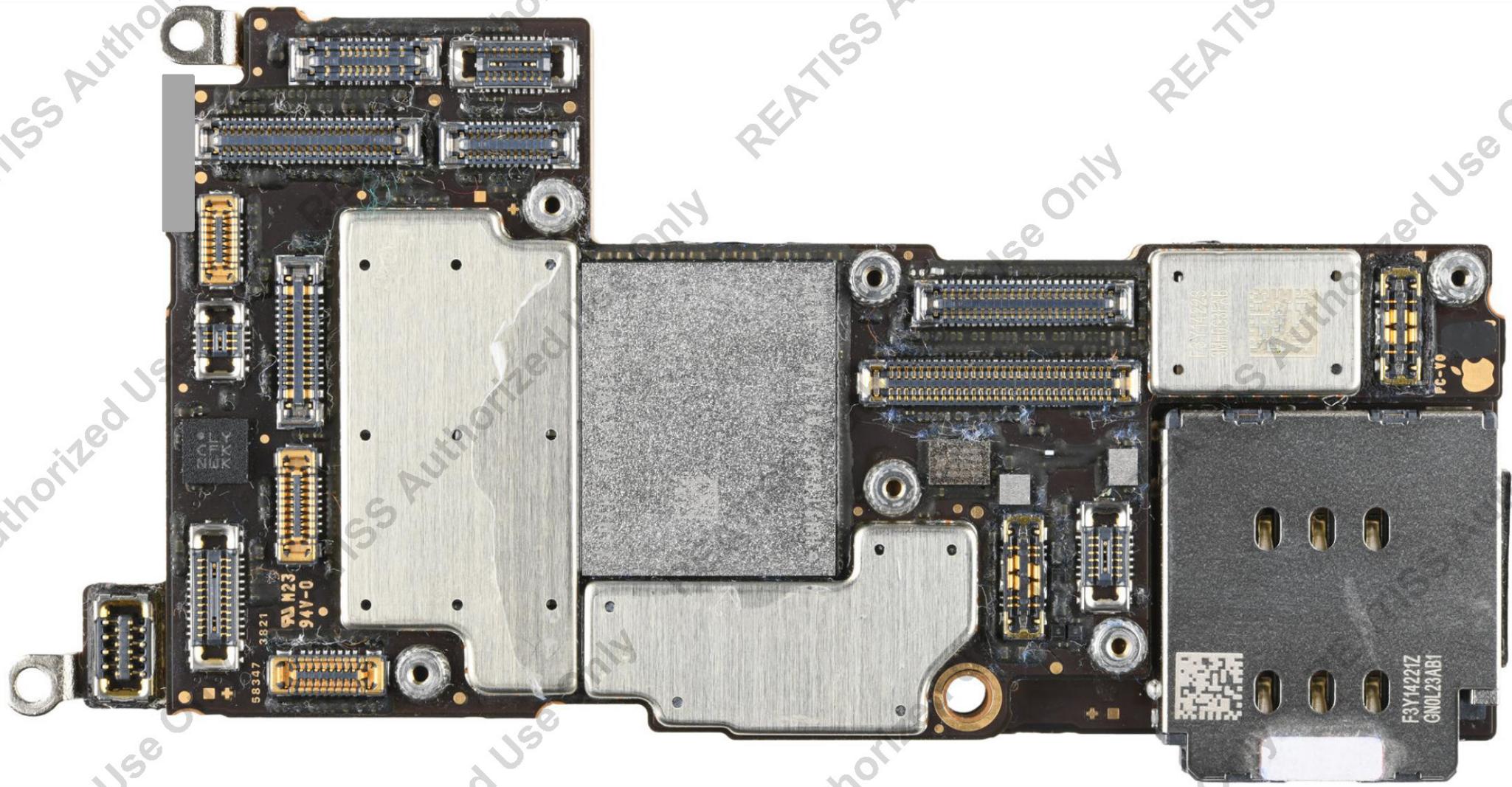


Figure 12. Apple

PCB assembly front with graphite films removed

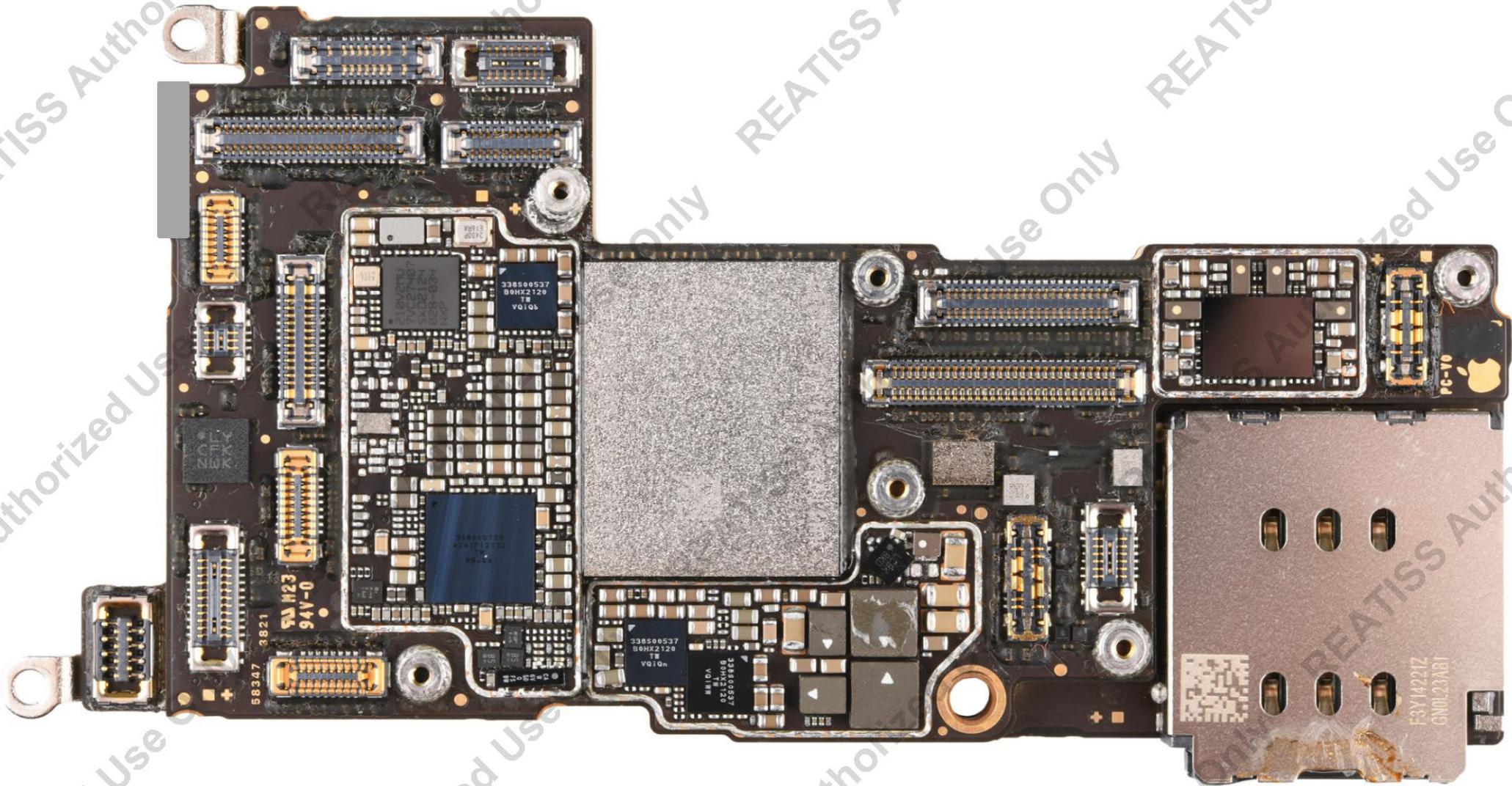


Figure 13. Apple

PCB assembly front with shields removed

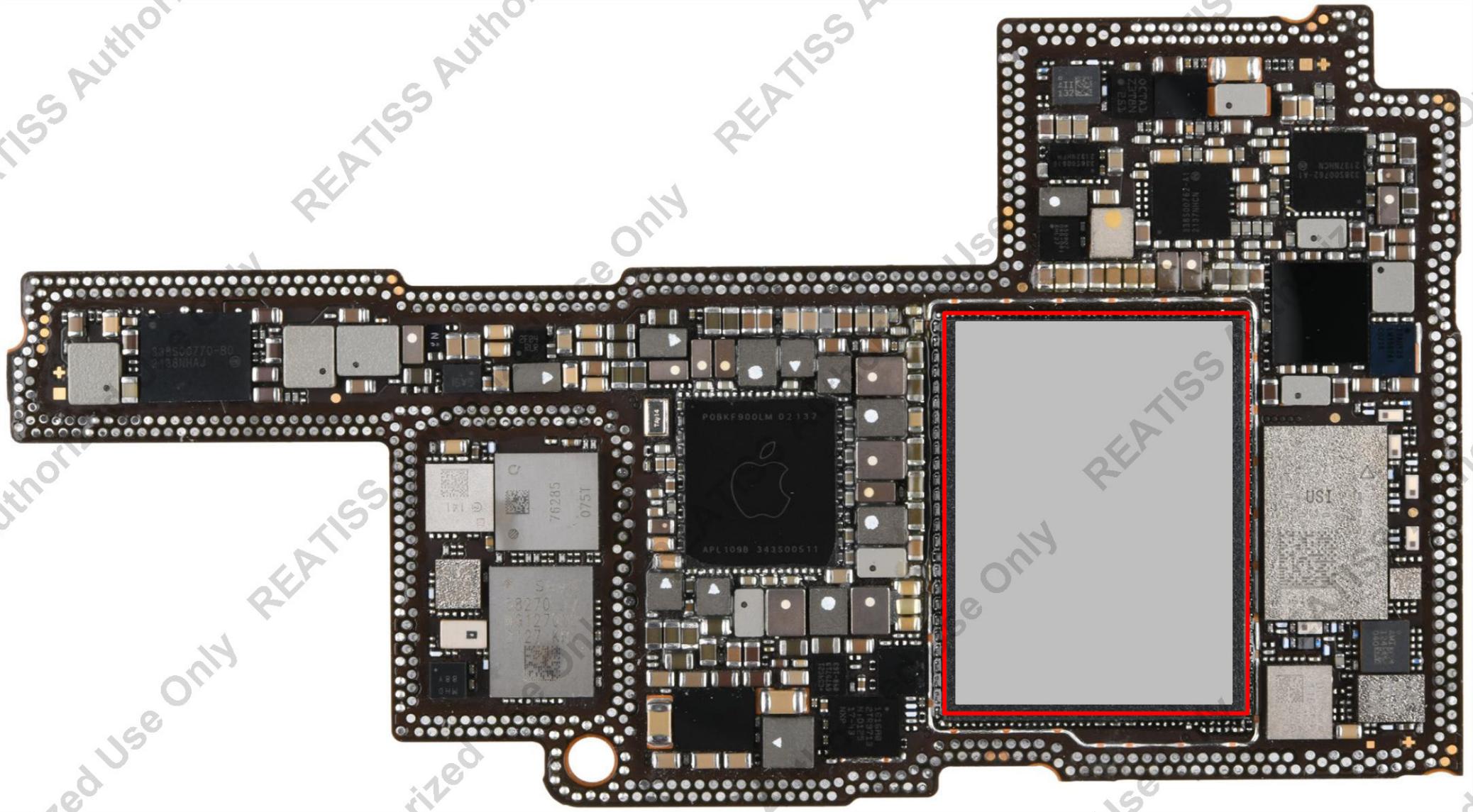


Figure 14. Apple

PCB II Side A



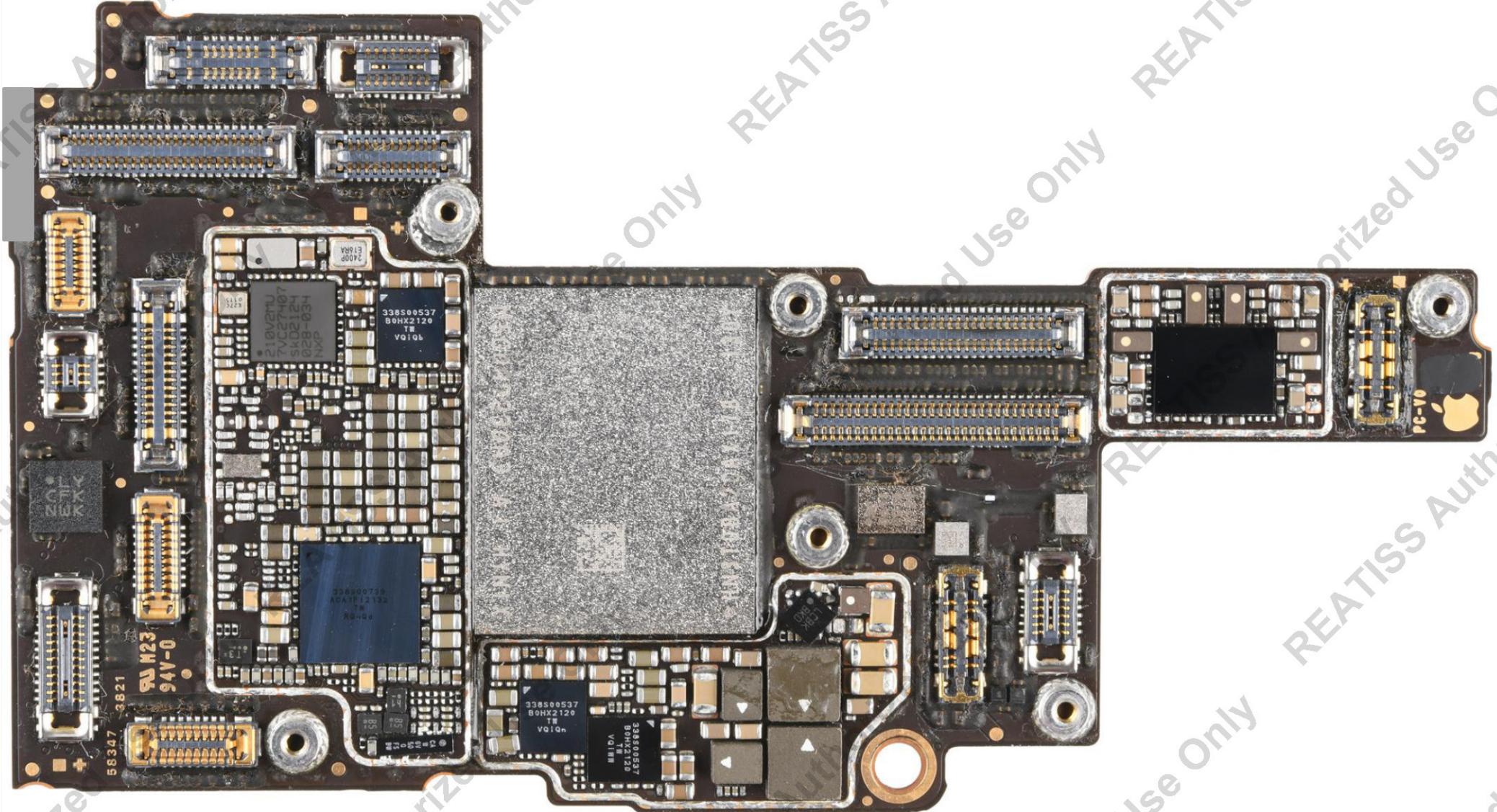


Figure 15. Apple

PCB II Side B

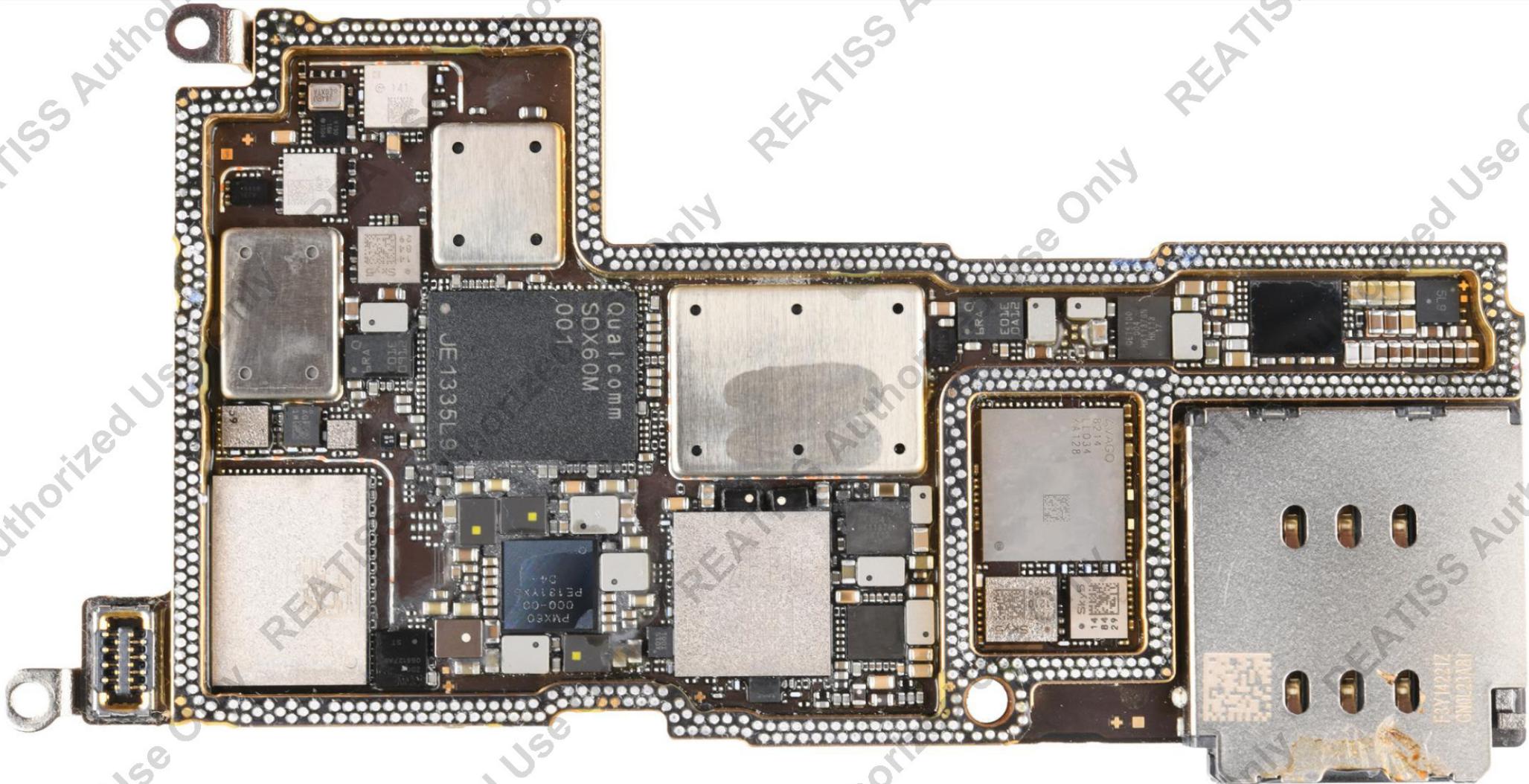


Figure 16. Apple PCB I Side A

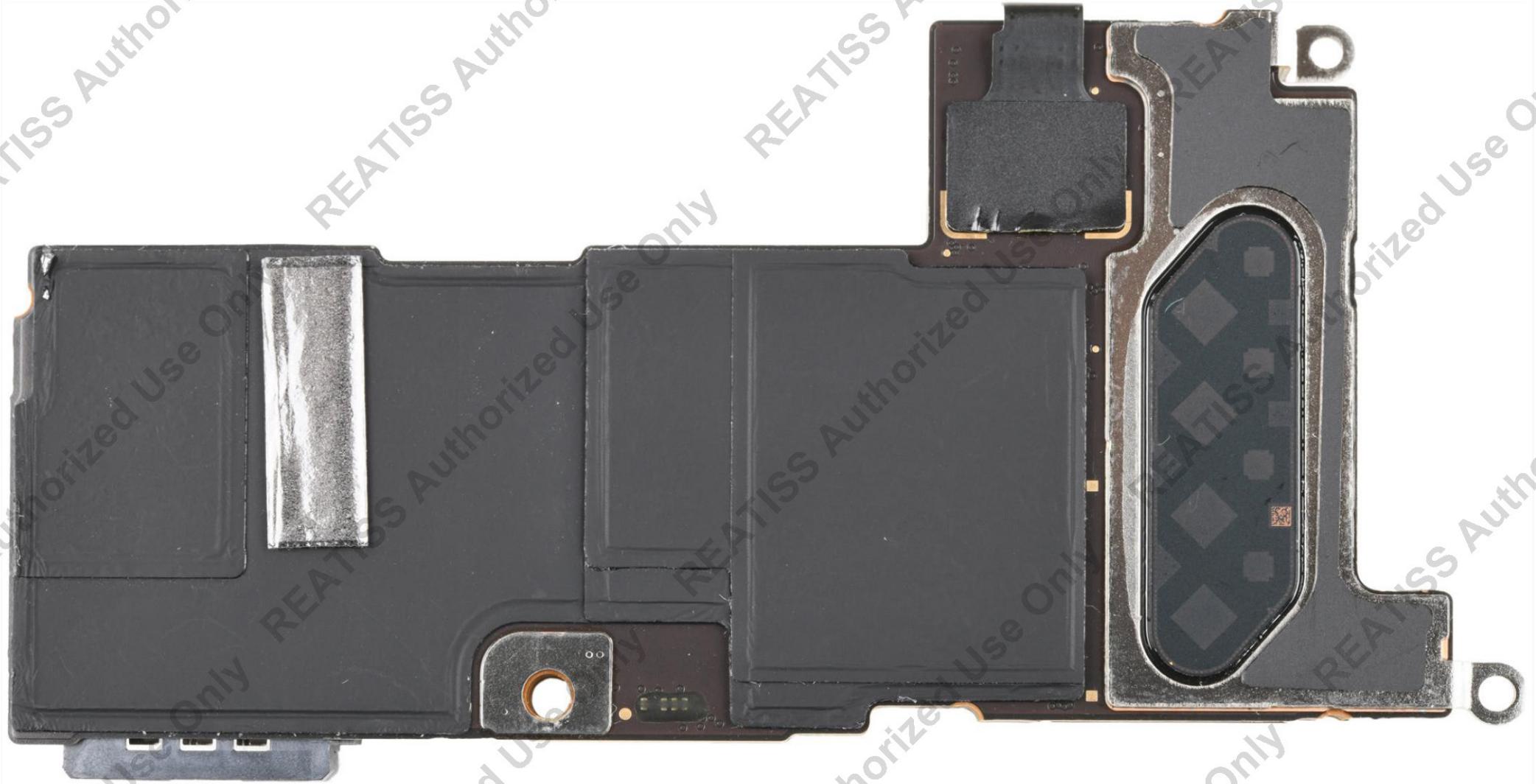


Figure 17. Apple PCB assembly back

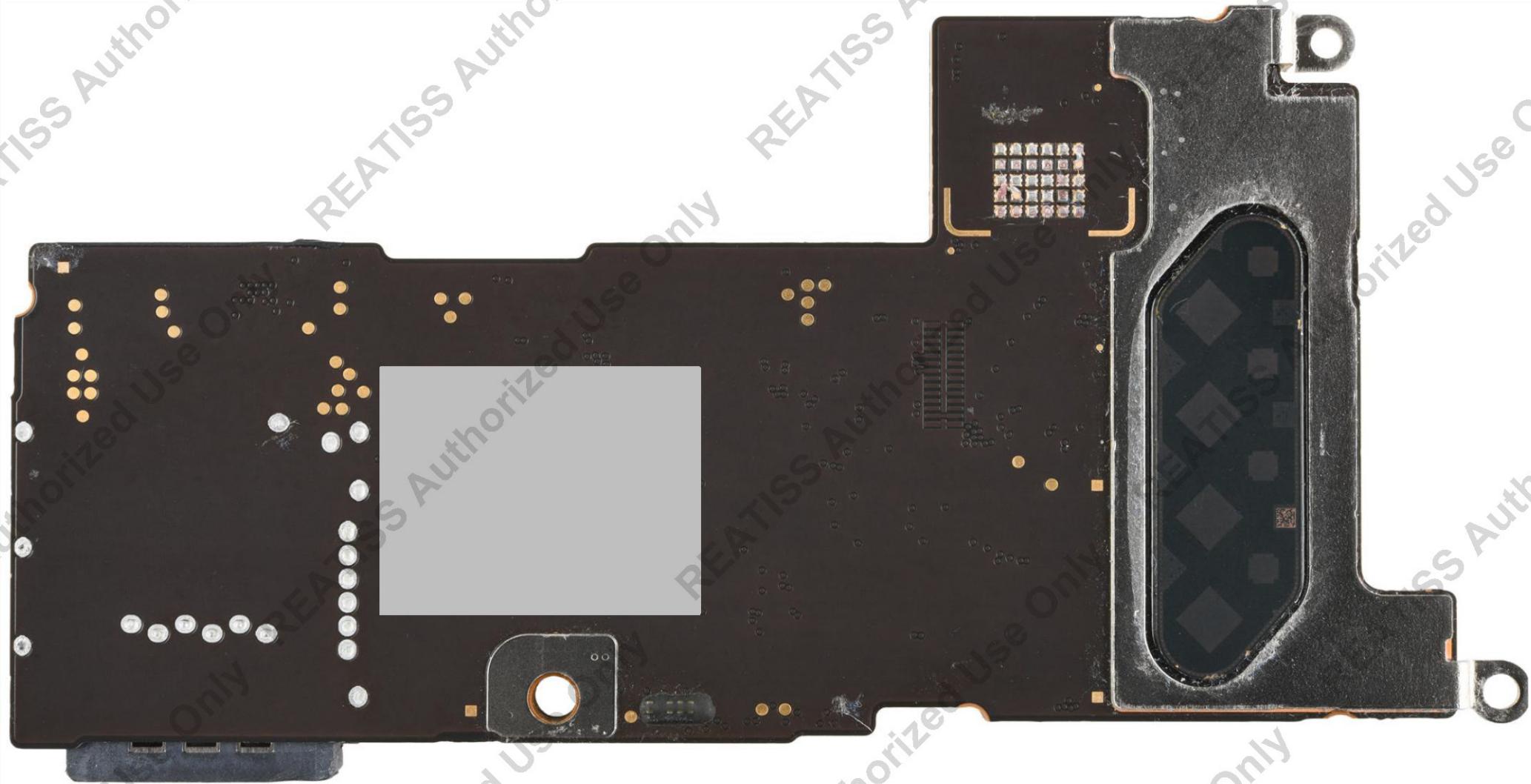


Figure 18. Apple PCB assembly back (PCB I Side B) with graphite films removed



Figure 19. Apple [REDACTED] front



Figure 20. Apple [REDACTED] back

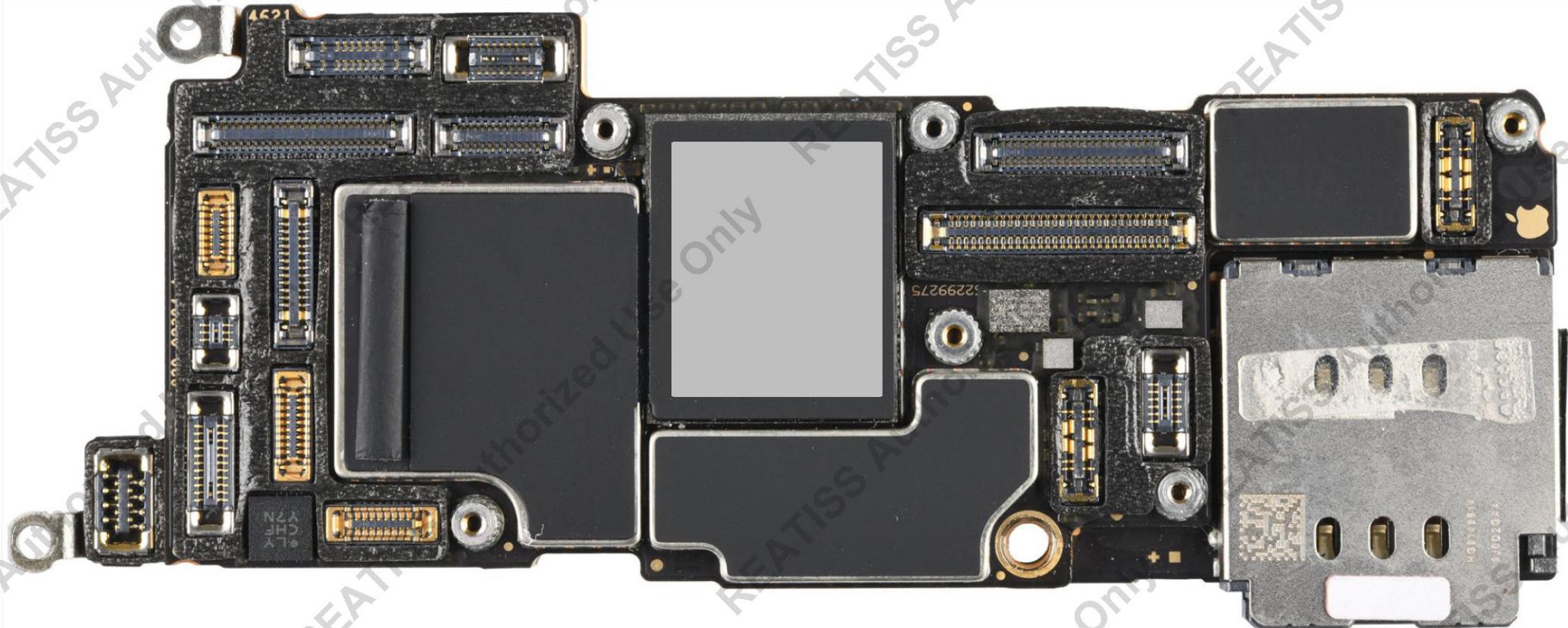


Figure 21. Apple

PCB assembly front

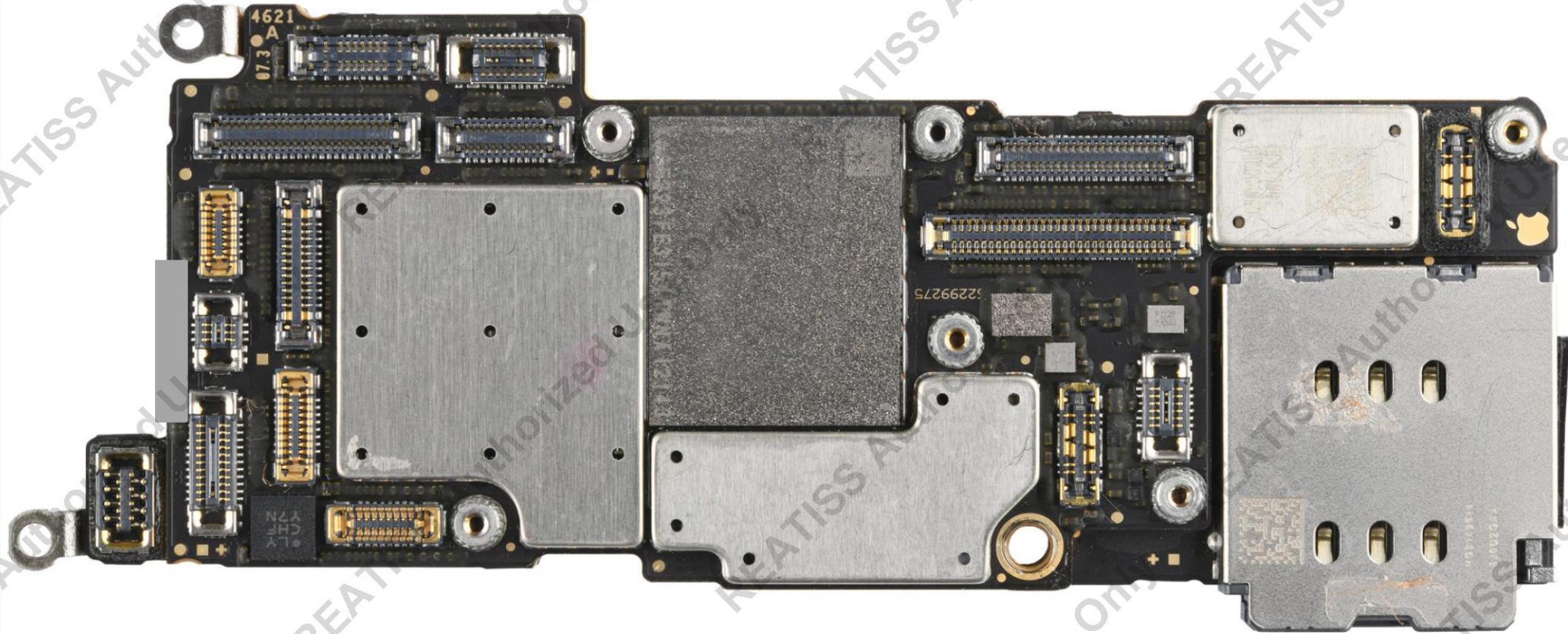


Figure 22. Apple PCB assembly front with graphite films removed

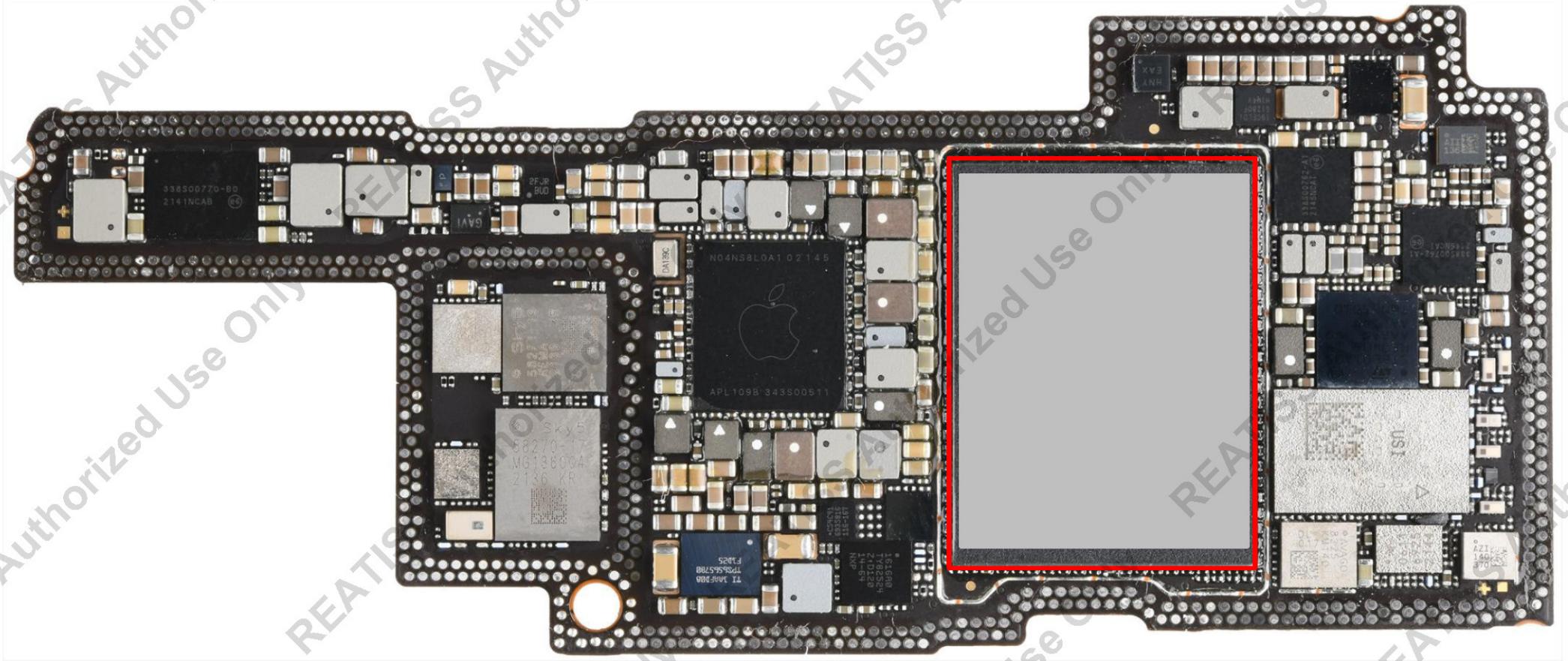


Figure 23. Apple PCB II Side A

Apple

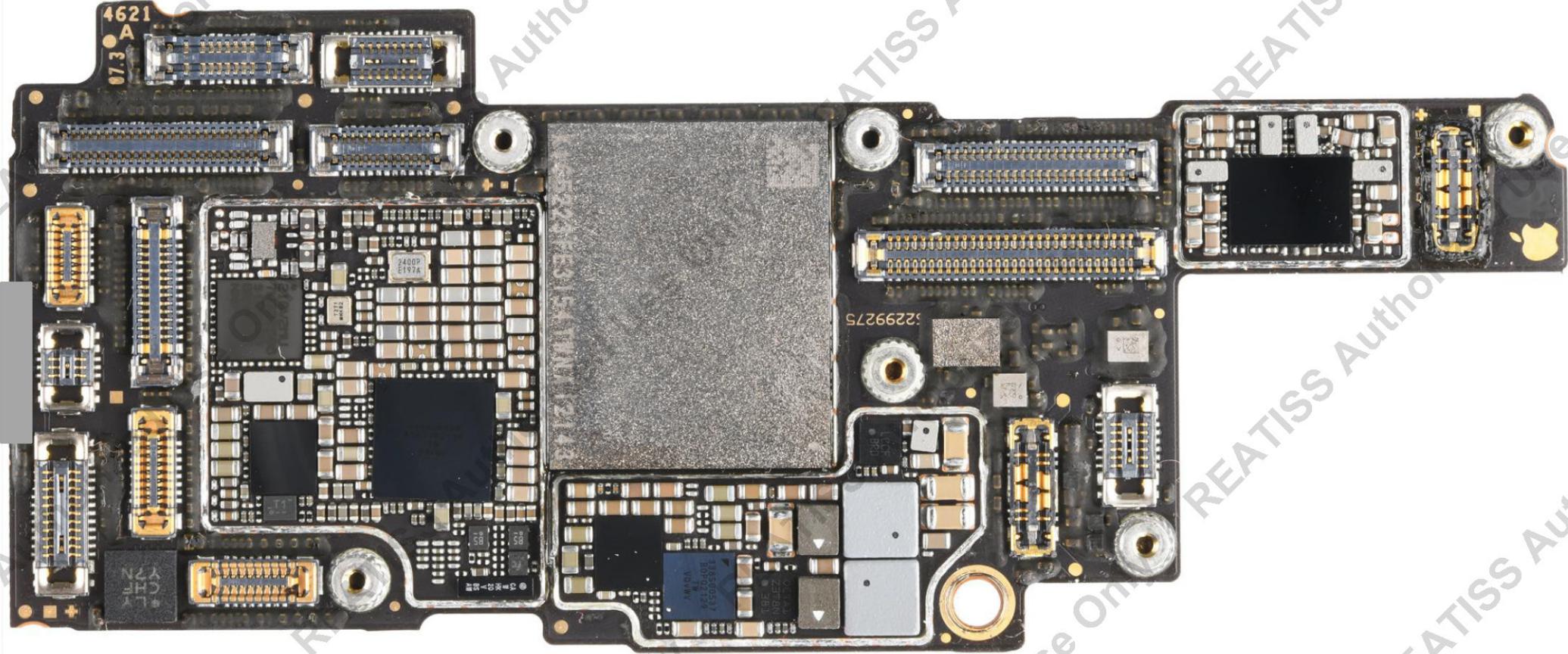


Figure 24. Apple PCB II Side B

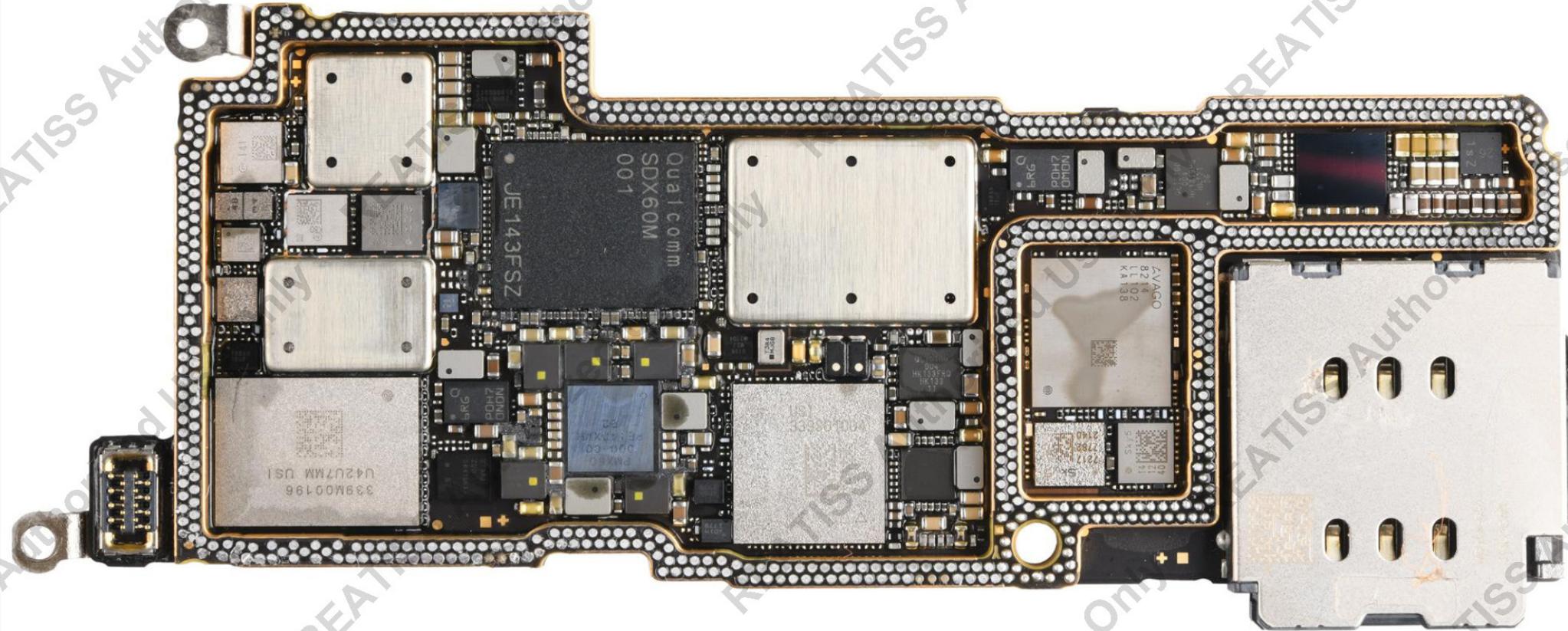


Figure 25. Apple PCB I Side A

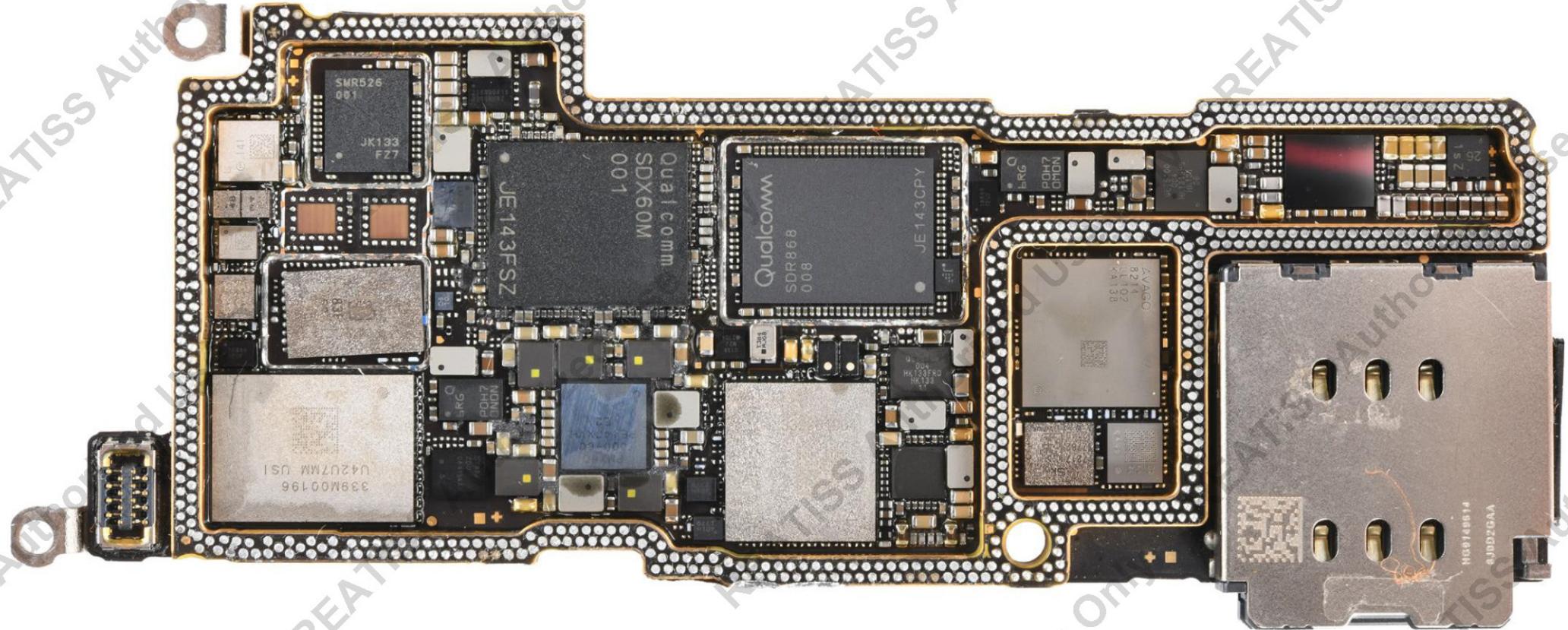


Figure 26. Apple PCB I Side A with shields removed

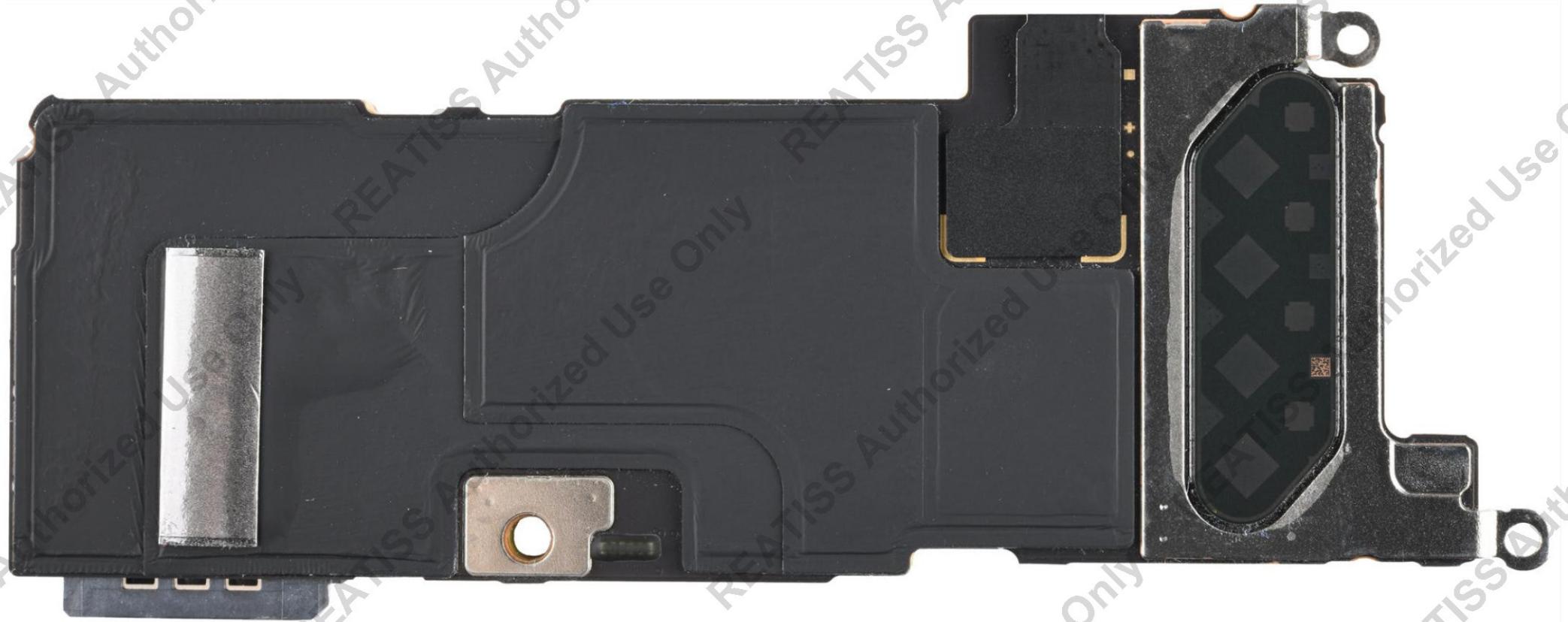


Figure 27. Apple PCB assembly back

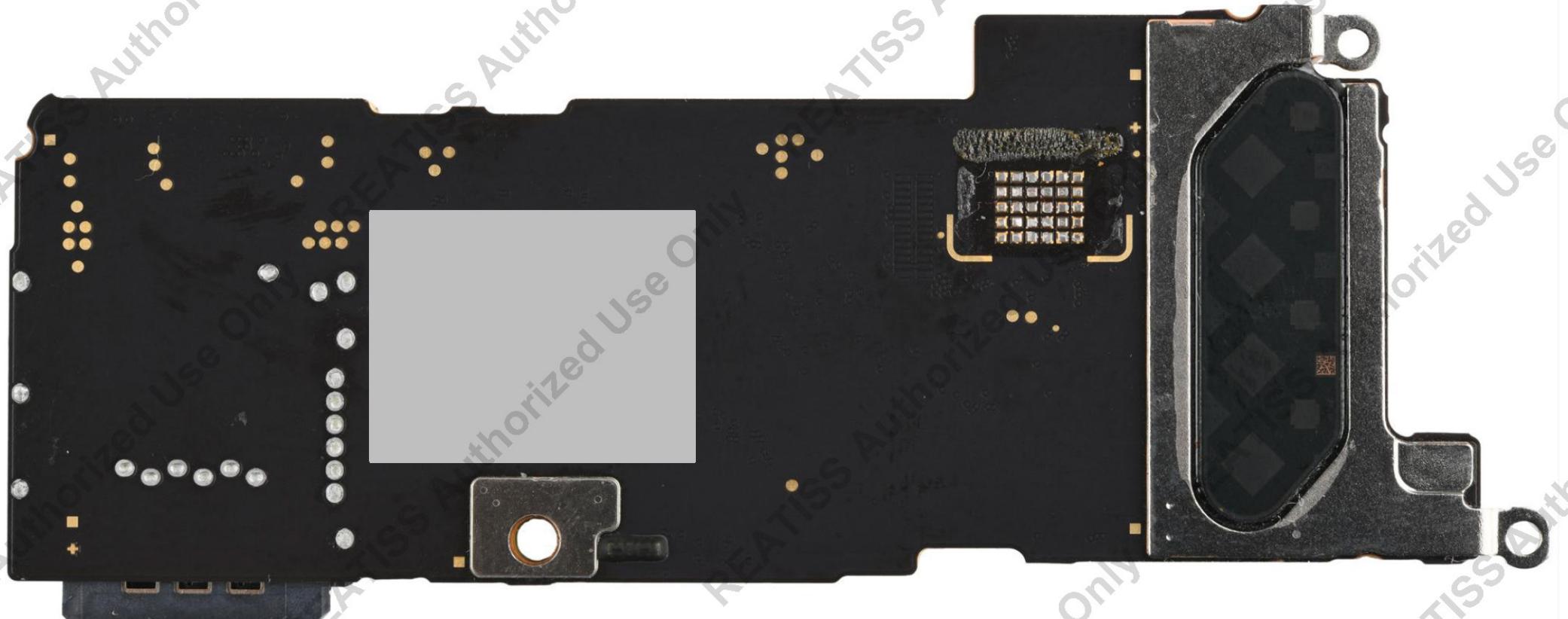


Figure 28. Apple PCB assembly back (PCB I Side B) with graphite films removed

Die and Package



Figure 29. Package top

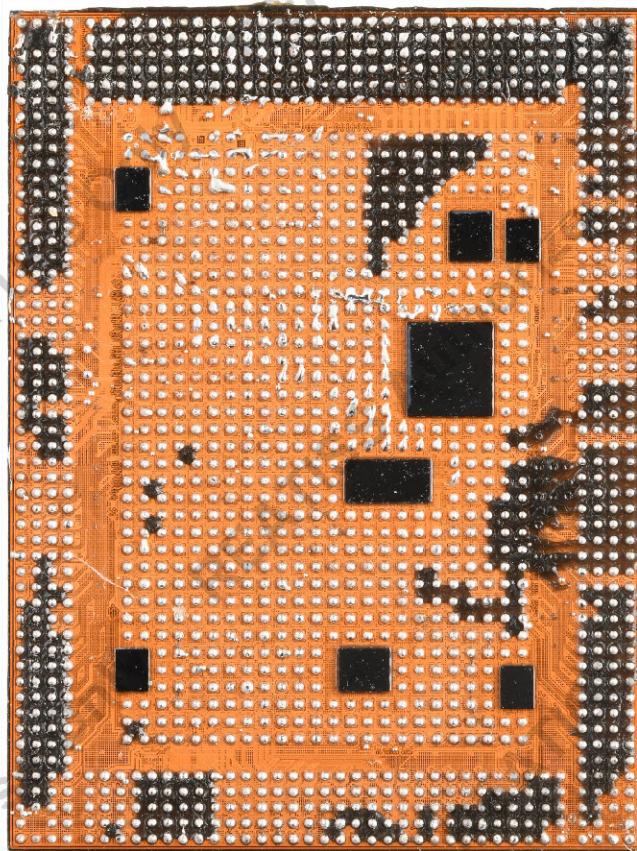


Figure 30. Package bottom

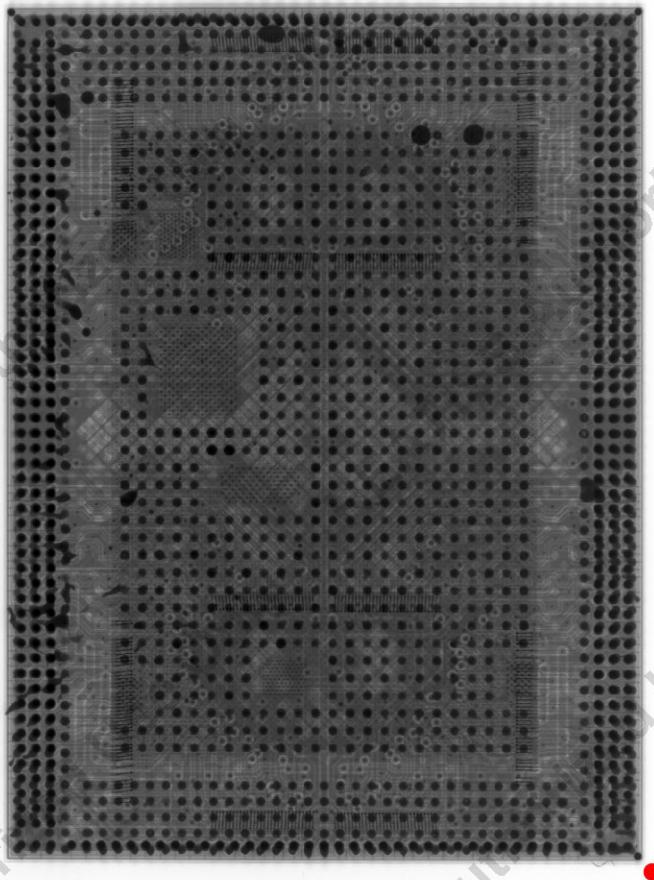


Figure 31. Package X-ray

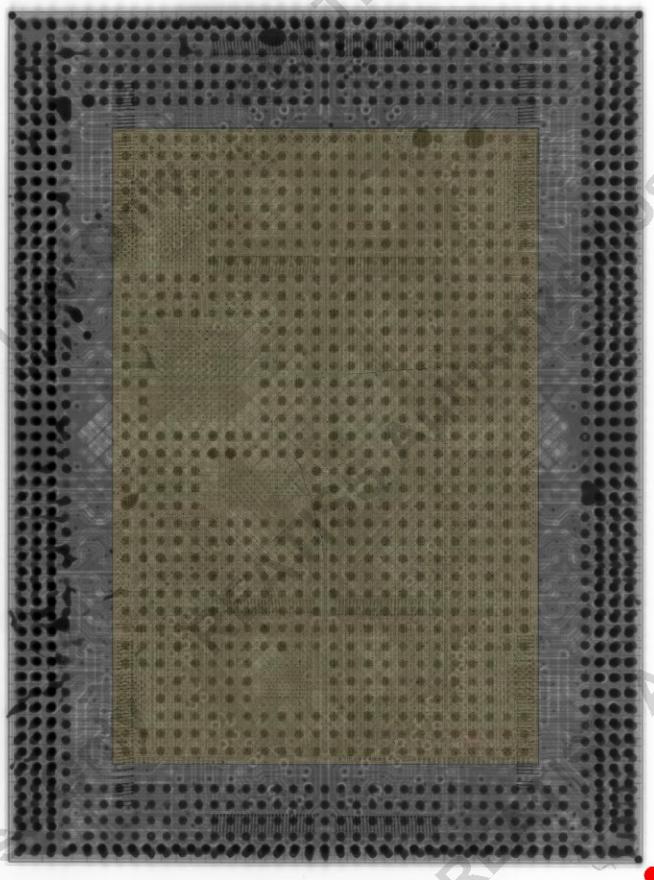


Figure 32. Package X-ray combined with Apple  processor die photo

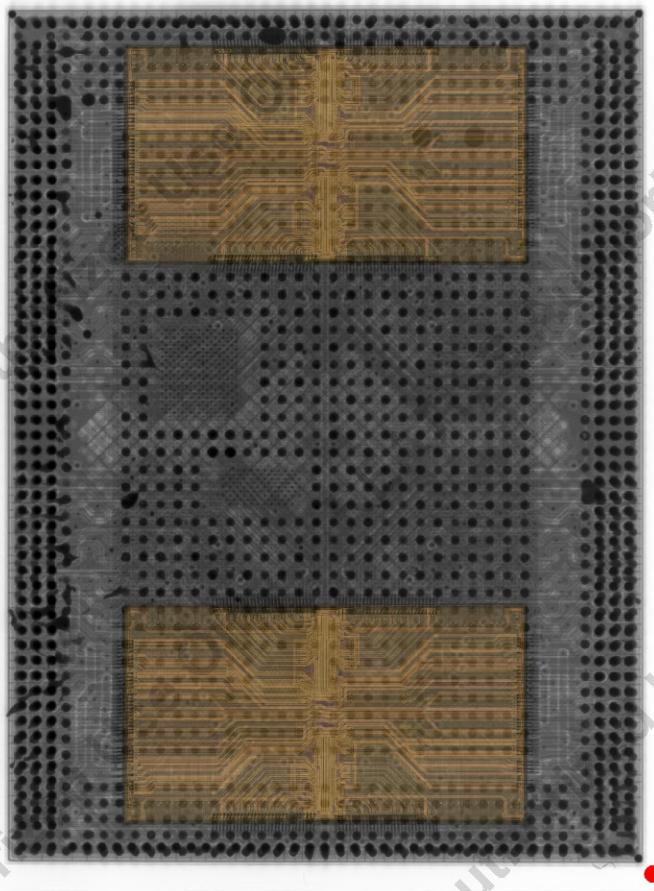


Figure 33. Package X-ray combined with Samsung SDRAM dice photo

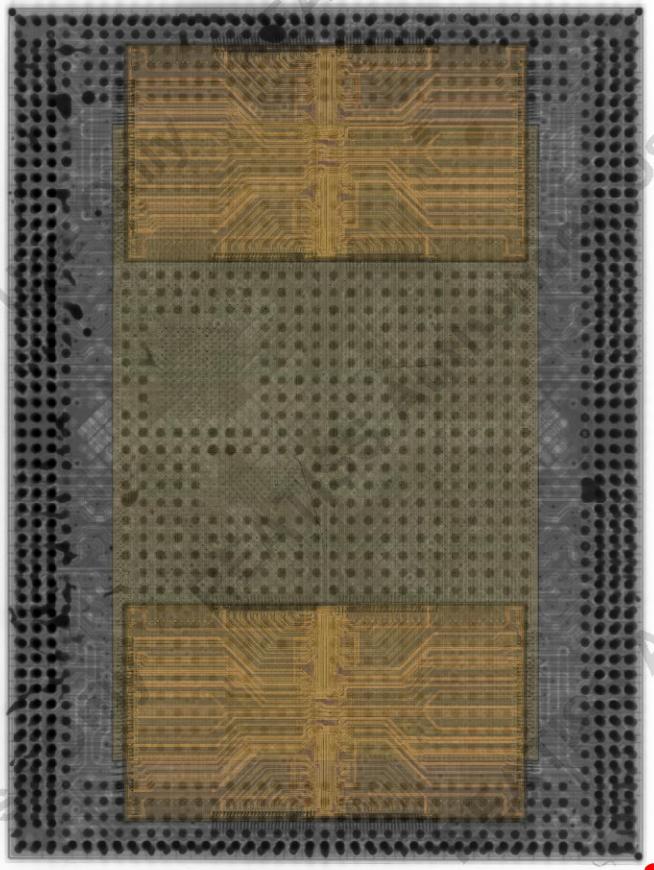


Figure 34. Package X-ray combined with dice photos



Figure 35. Apple [redacted] processor die photo (top metal)



Figure 36. Apple [REDACTED] processor die markings

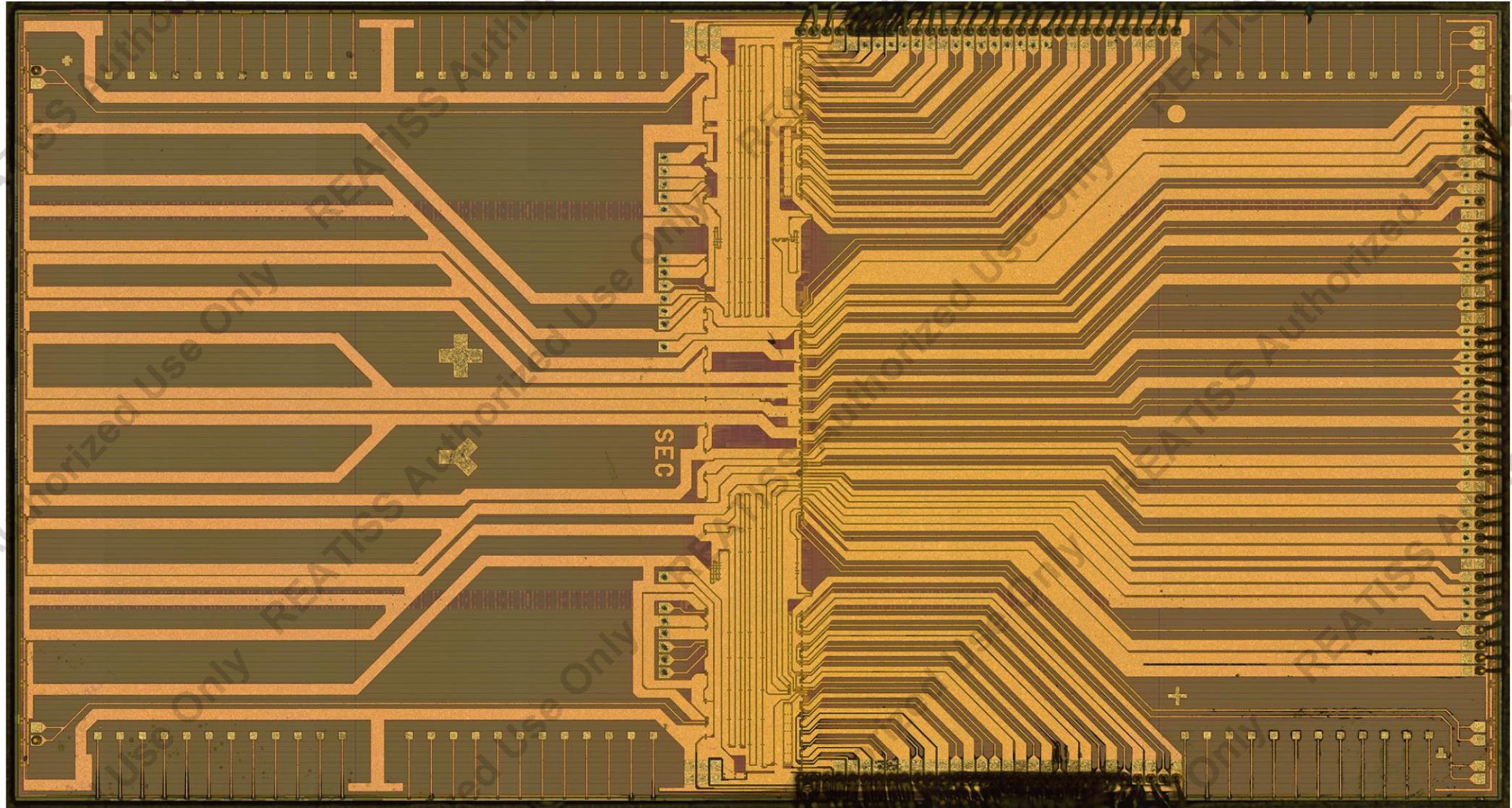


Figure 37. Samsung SDRAM die photo (top metal)



Figure 38. Samsung SDRAM die markings

Package Analysis

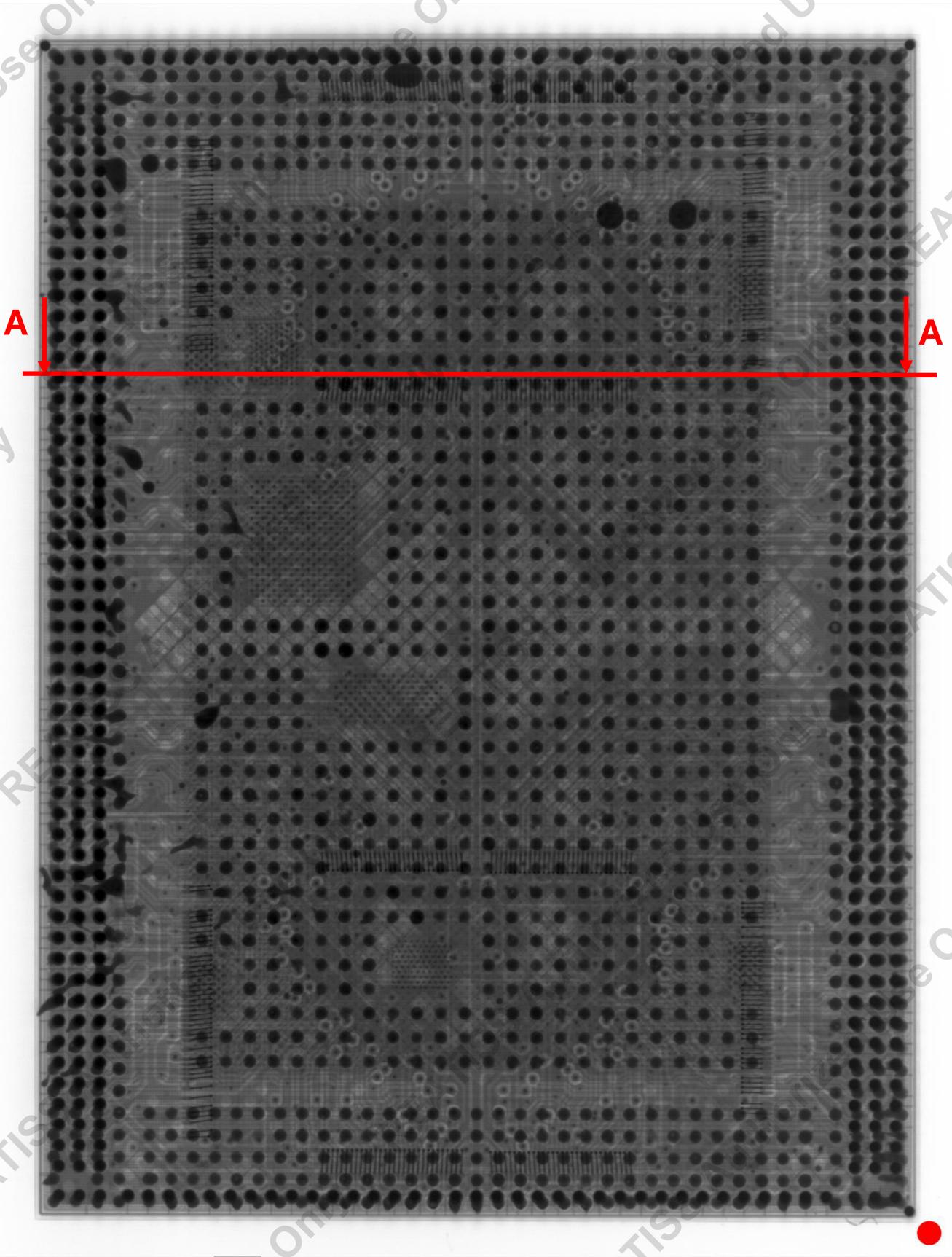


Figure 39. Apple [redacted] package X-ray with cross-section A-A marked



Figure 40. Package cross-section A-A

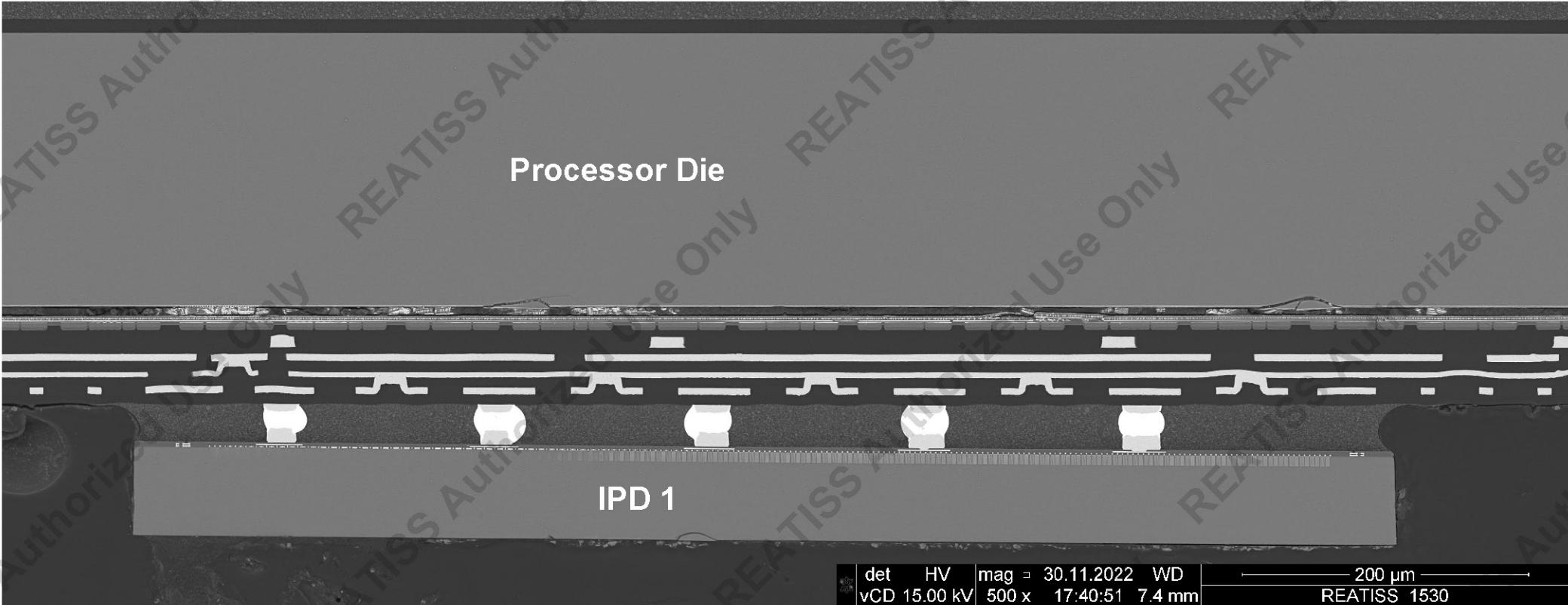


Figure 41. Integrated Passive Device (IPD) 1 cross-section

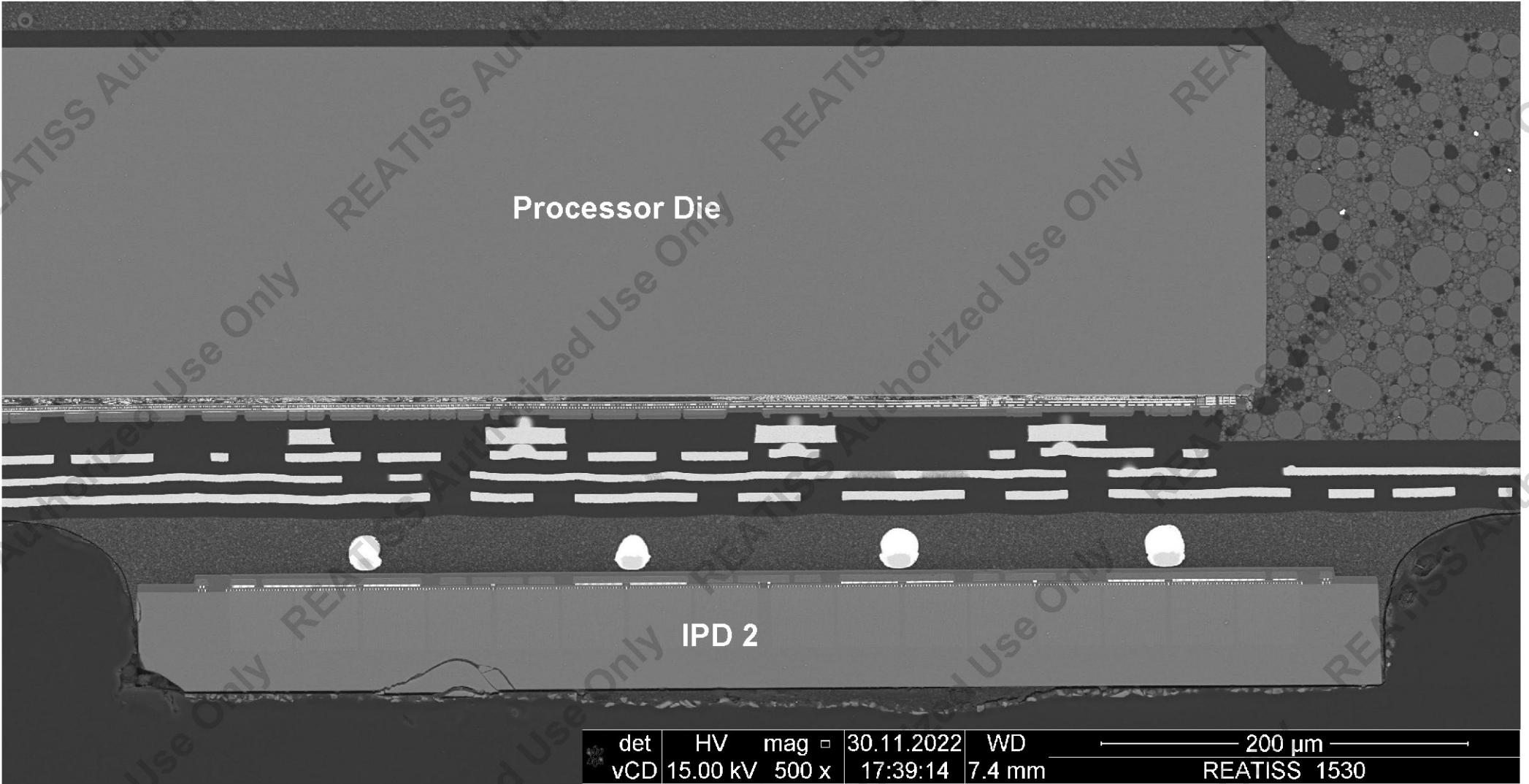


Figure 42. IPD 2 cross-section

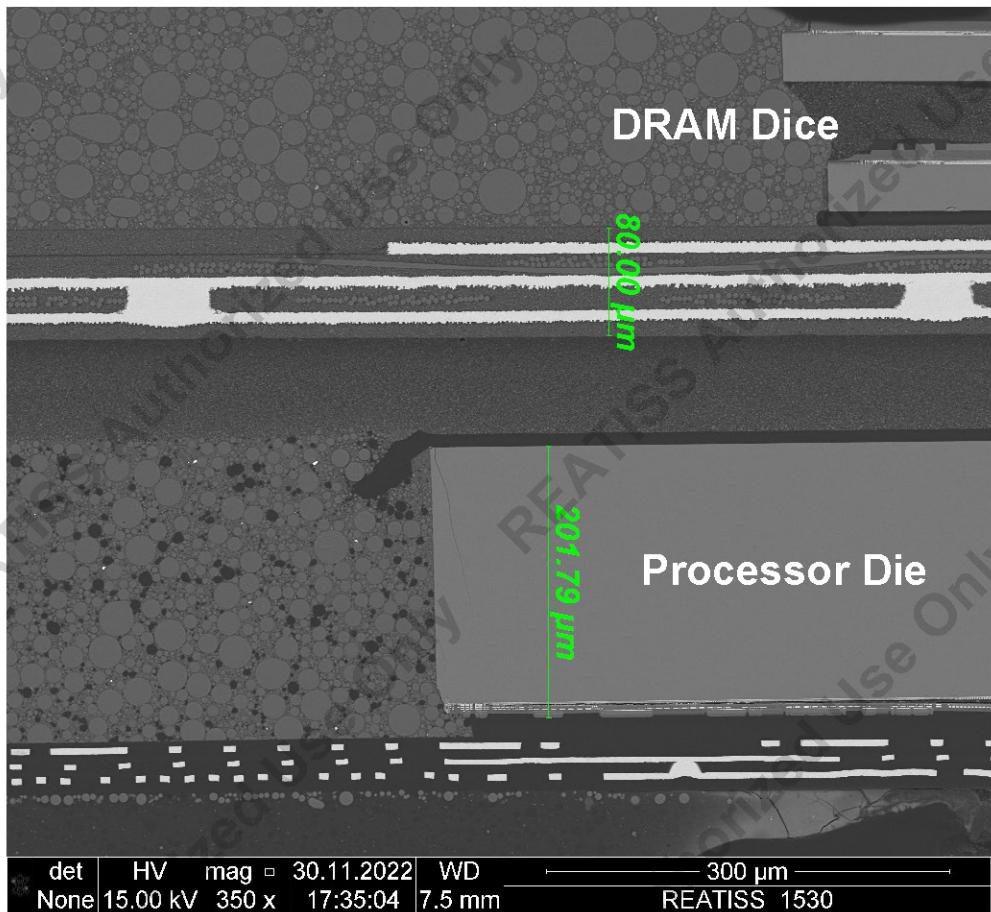


Figure 43. Dice assembly

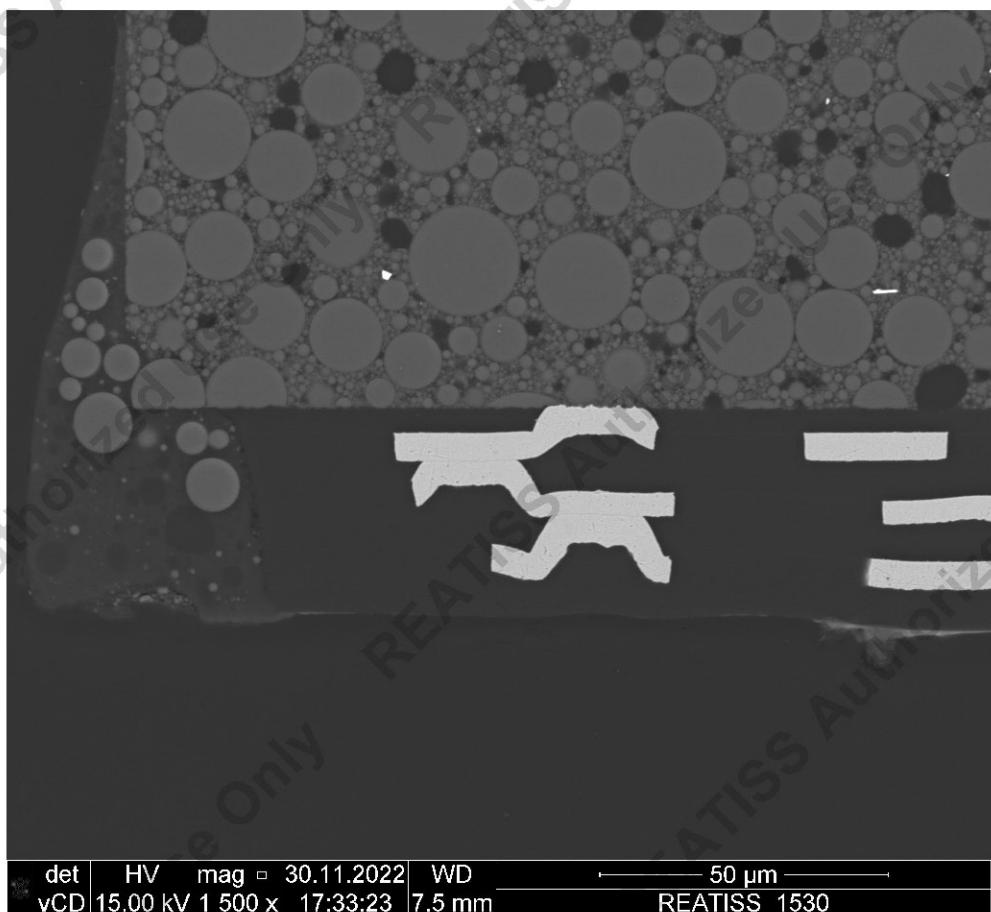


Figure 44. Package corner and RDLs connections

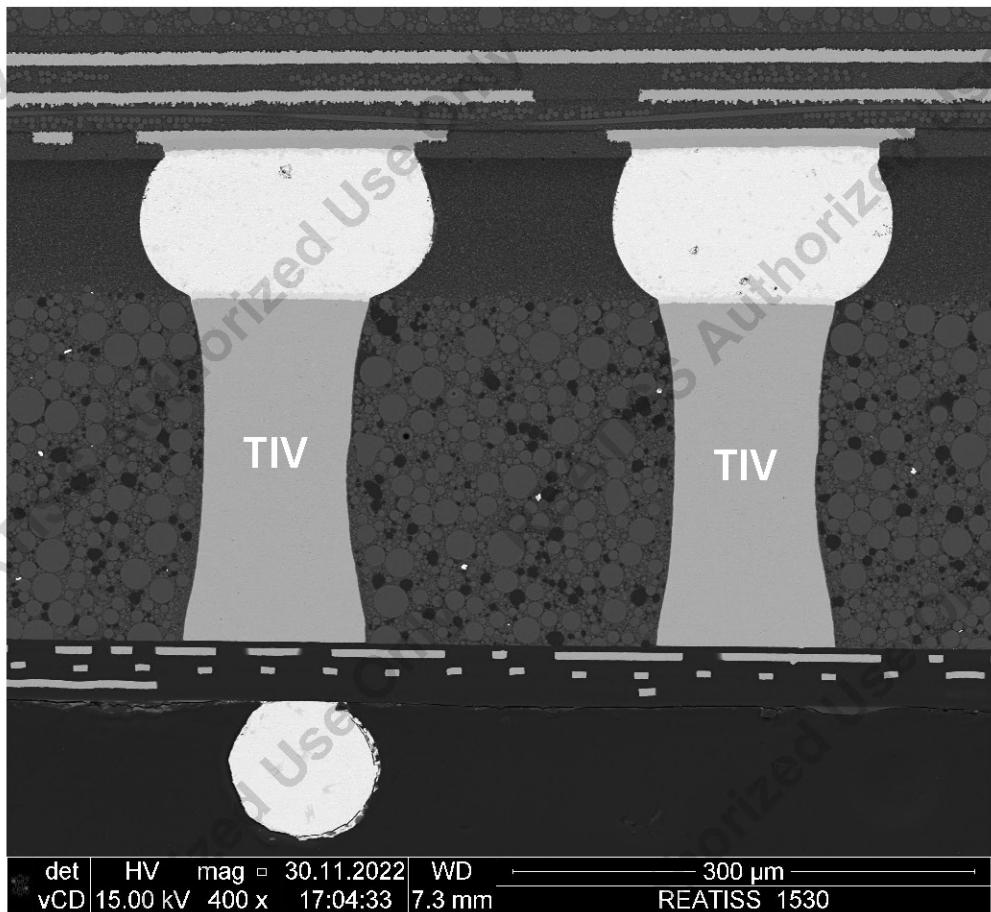


Figure 45. Through InFO vias (TIV)

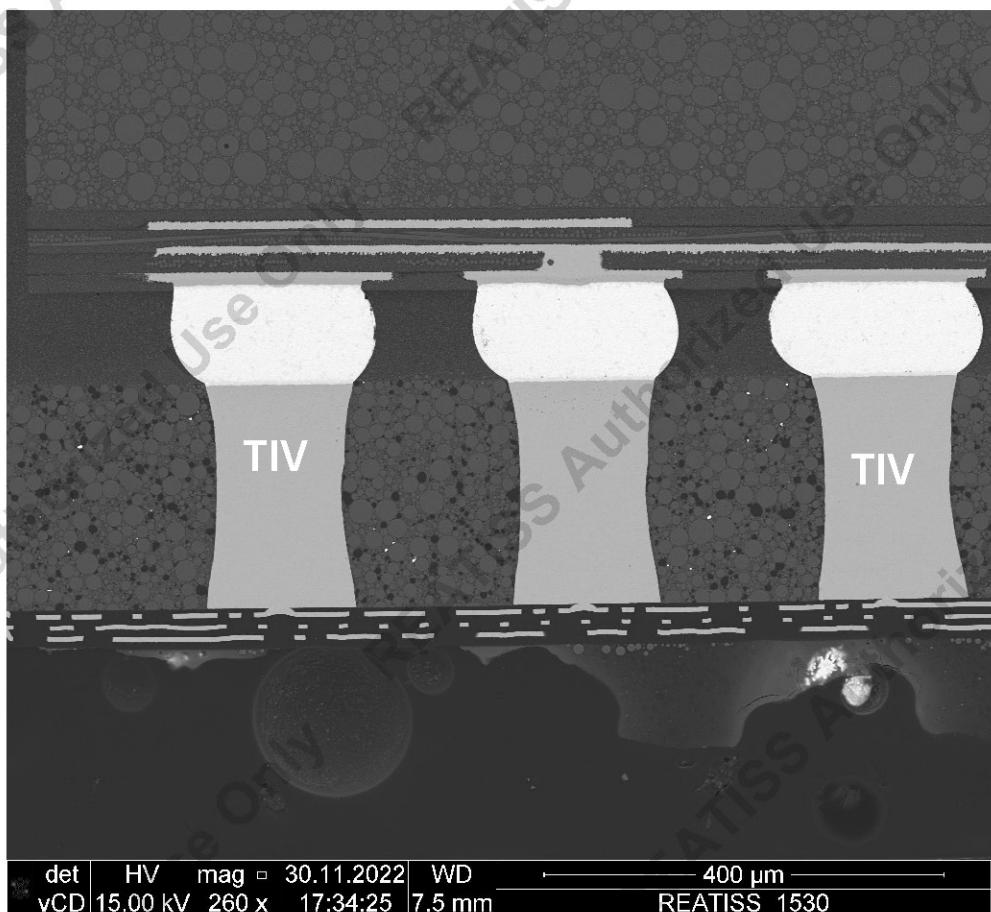


Figure 46. Through InFO vias

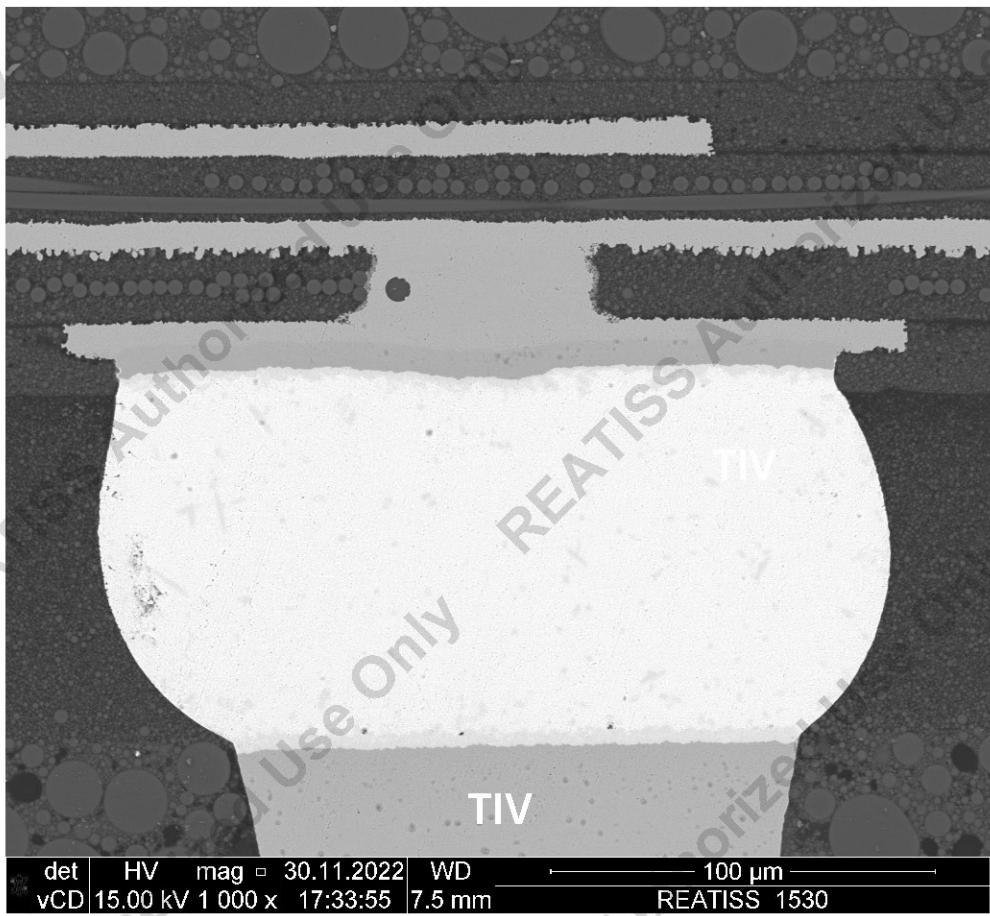


Figure 47. Memory package PCB to through InFO via connection

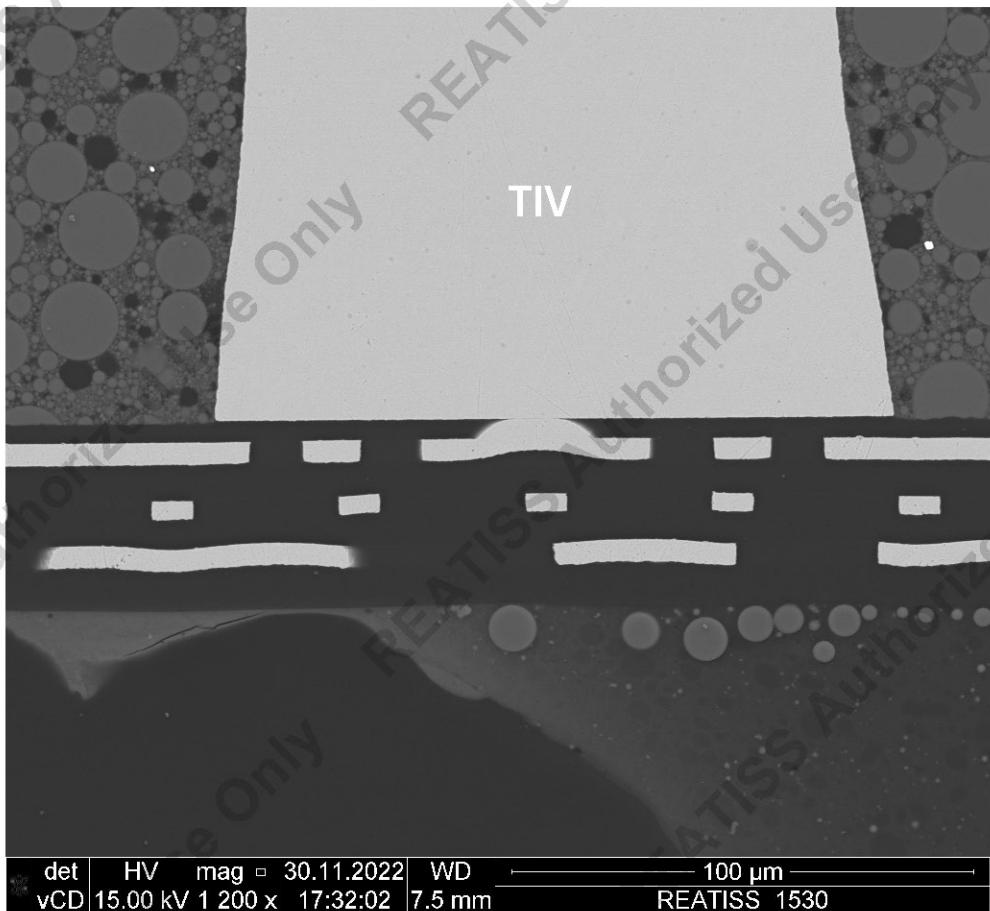


Figure 48. Through InFO via to RDL connection

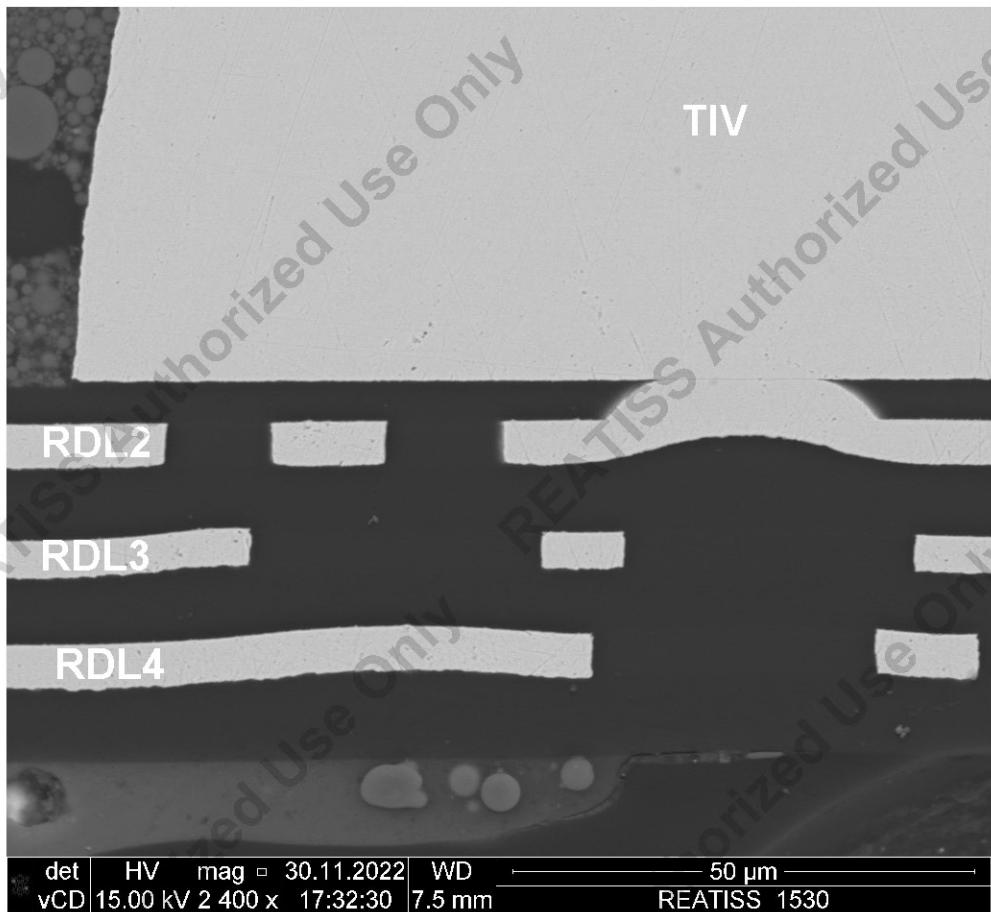


Figure 49. RDL2-RDL4, Through InFO via to RDL connection

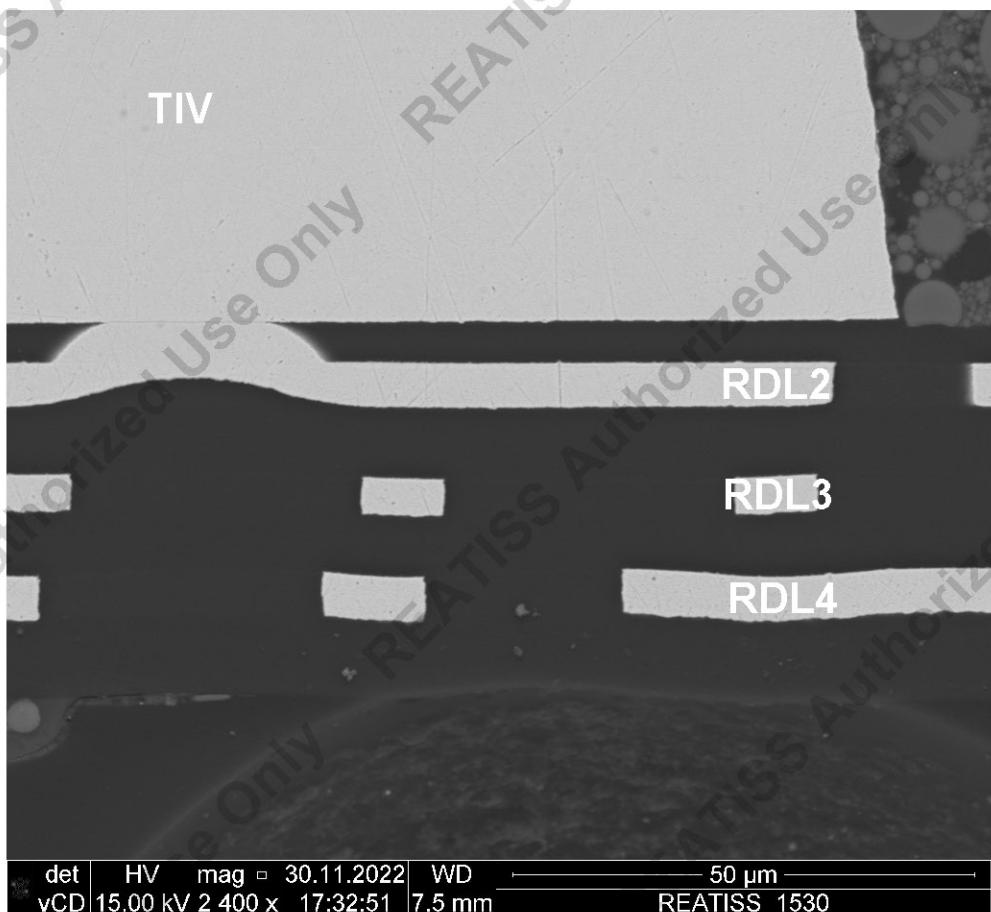


Figure 50. RDL2-RDL4, Through InFO via to RDL connection

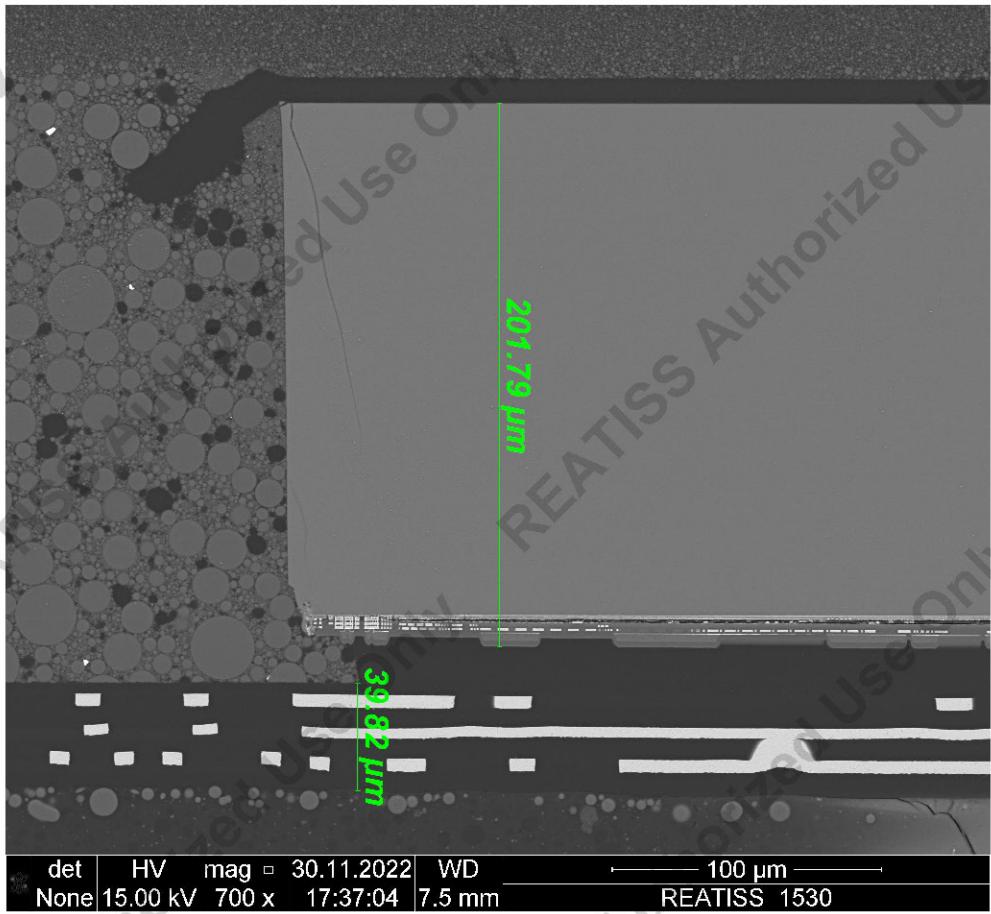


Figure 51. Processor die assembly

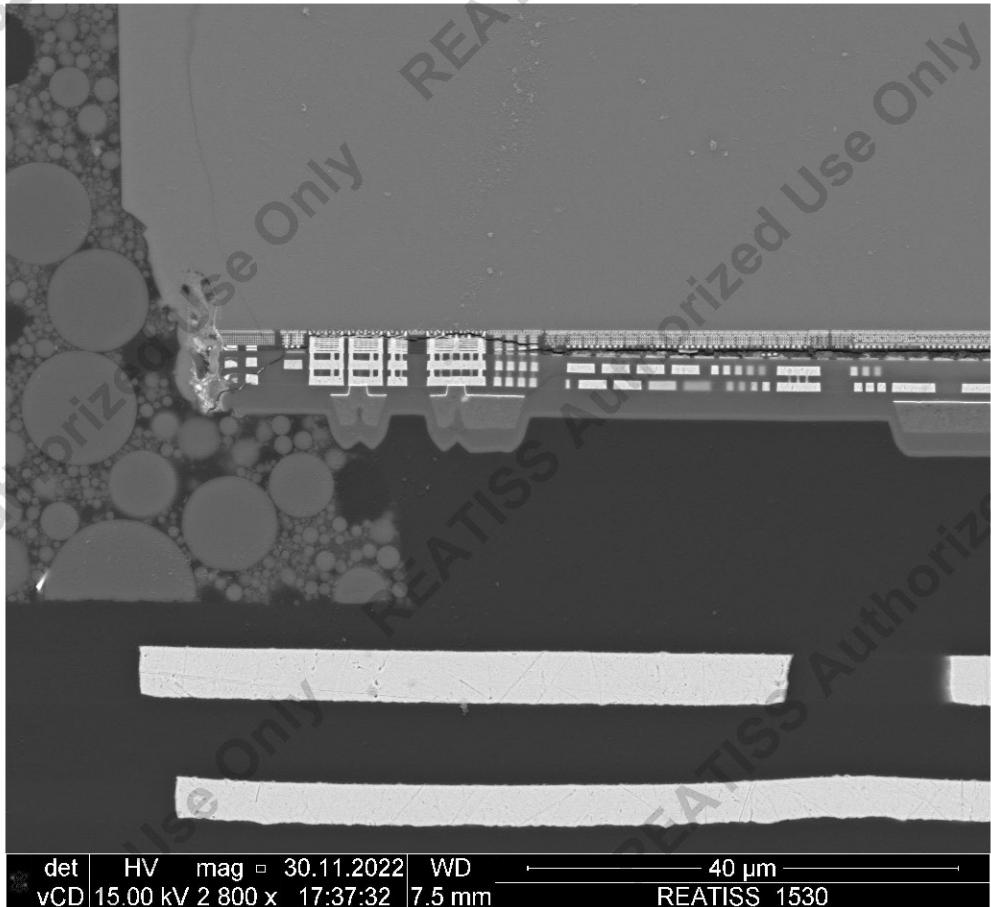


Figure 52. Processor die corner and encapsulation

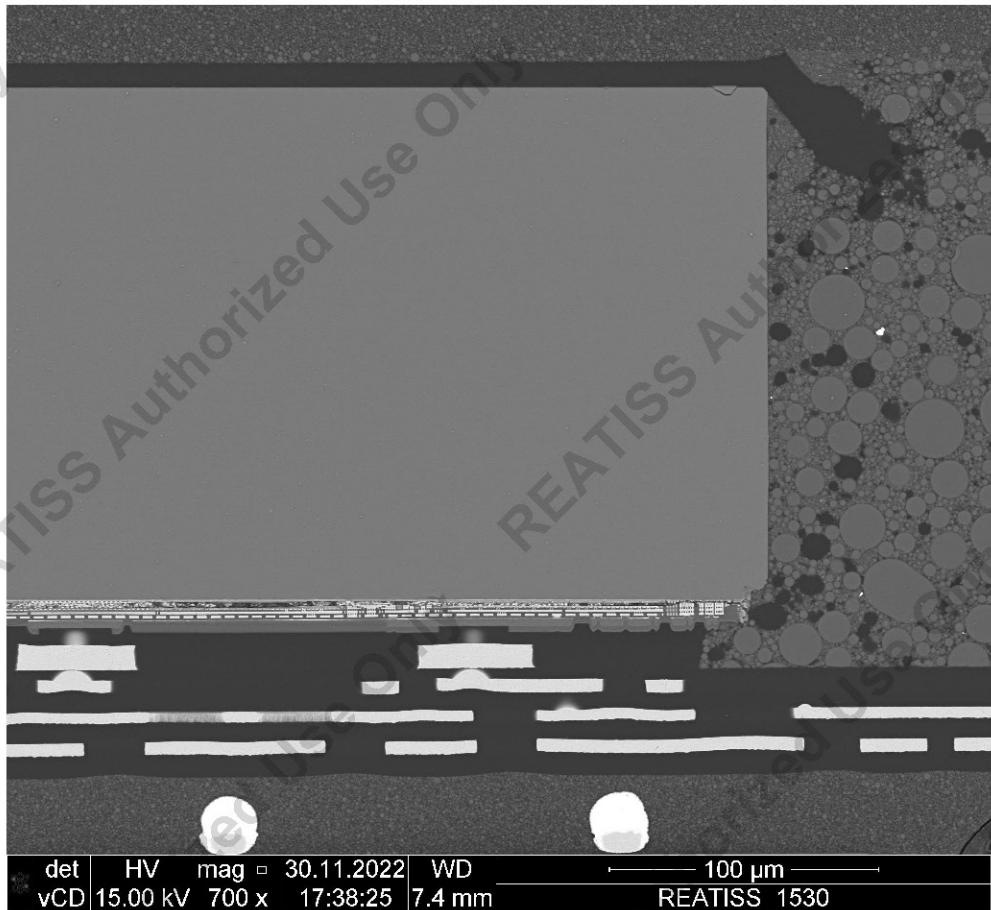


Figure 53. Processor die assembly

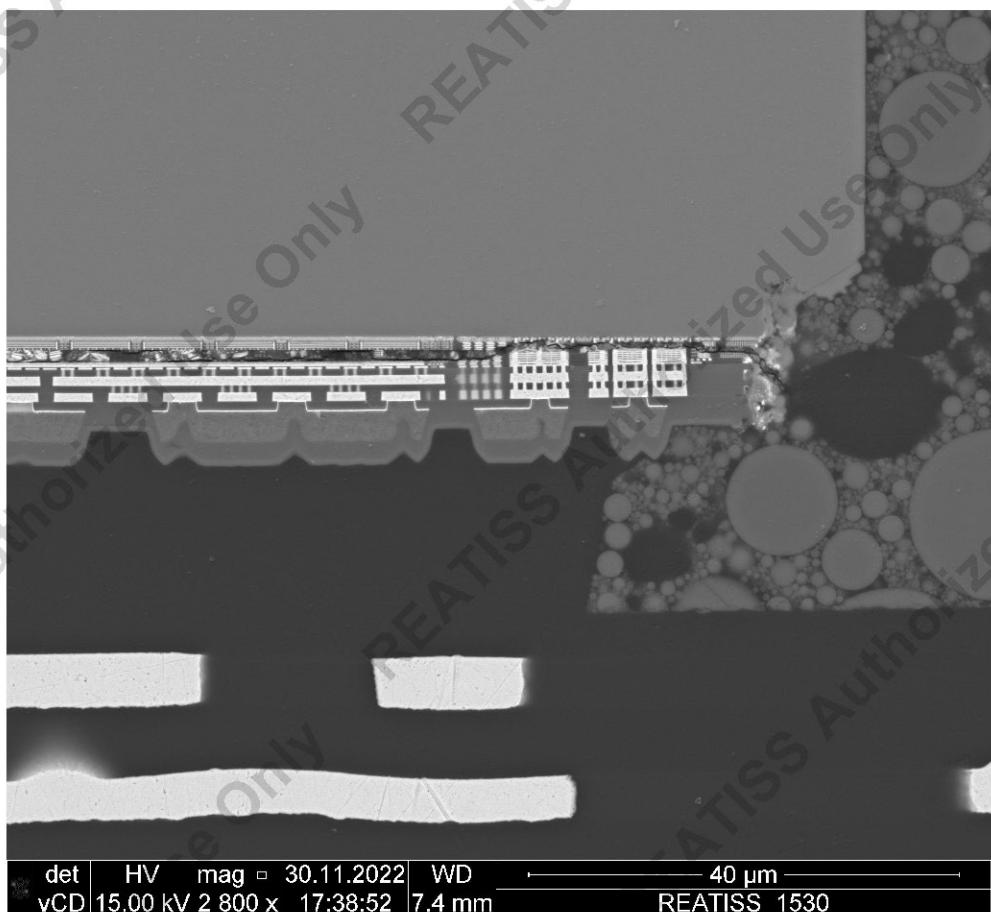


Figure 54. Processor die corner and encapsulation

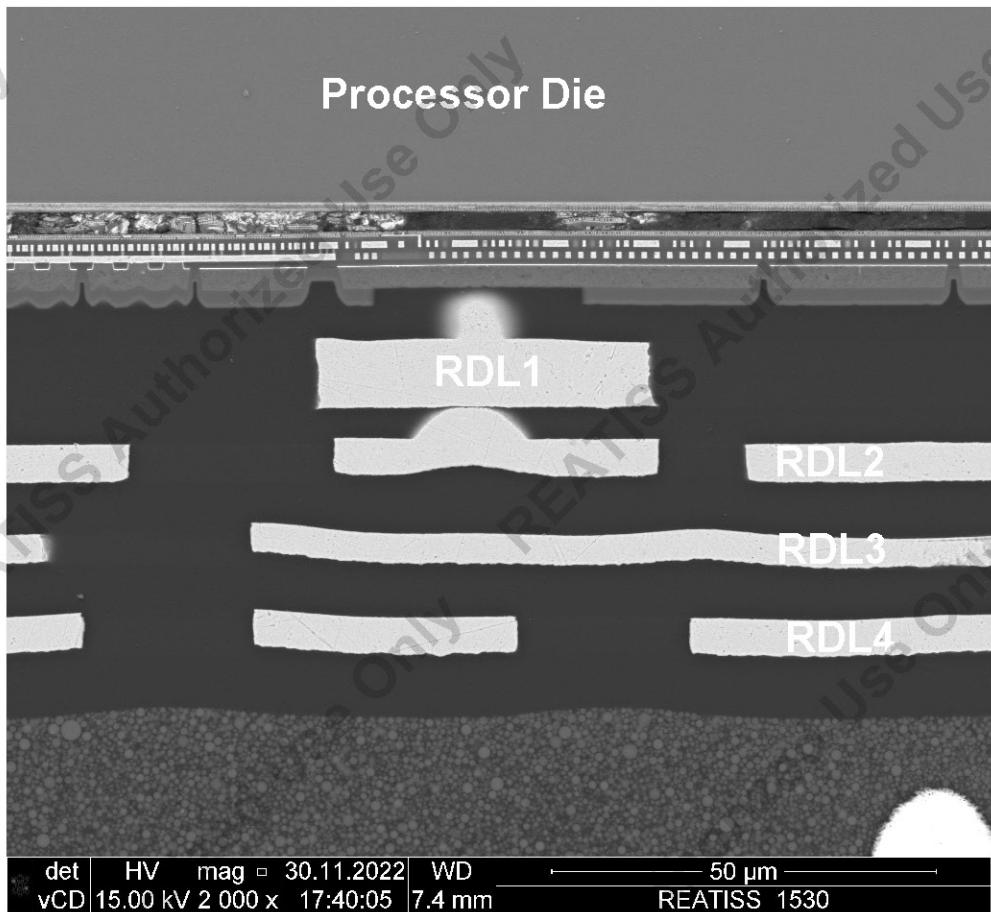


Figure 55. Processor die bond pad, RDL1-RDL4

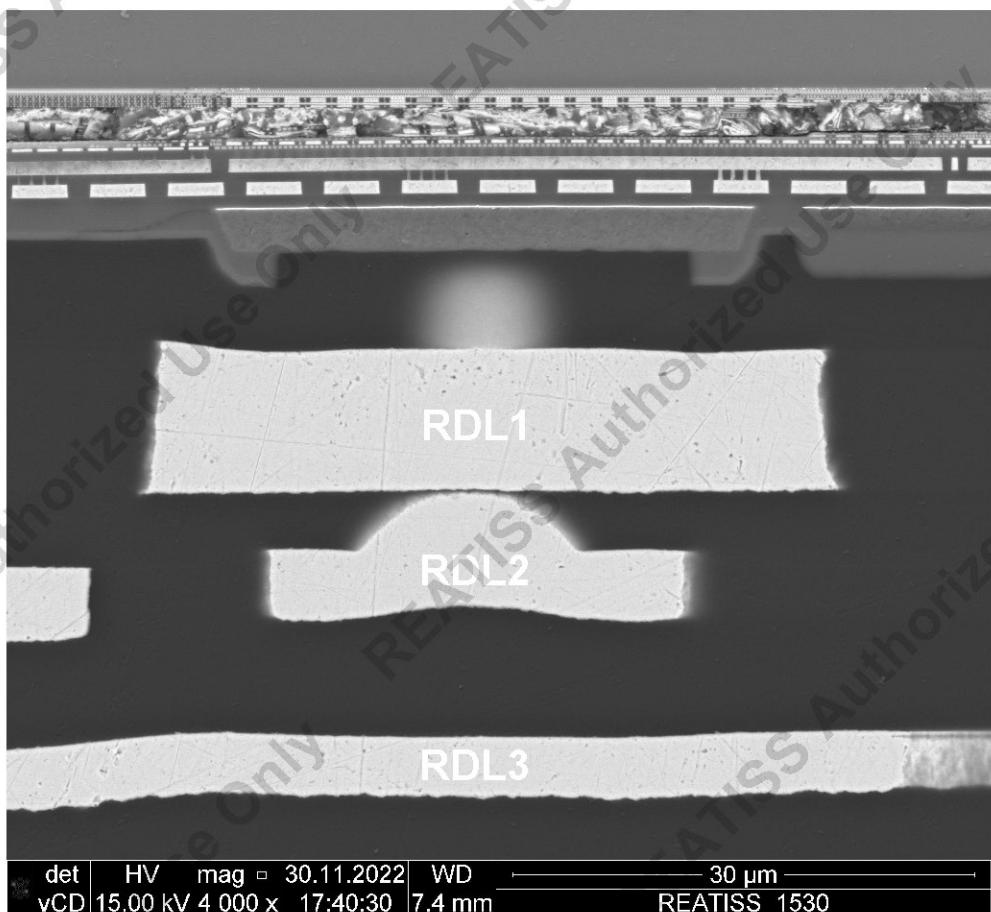


Figure 56. Processor die bond pad, RDL1-RDL3

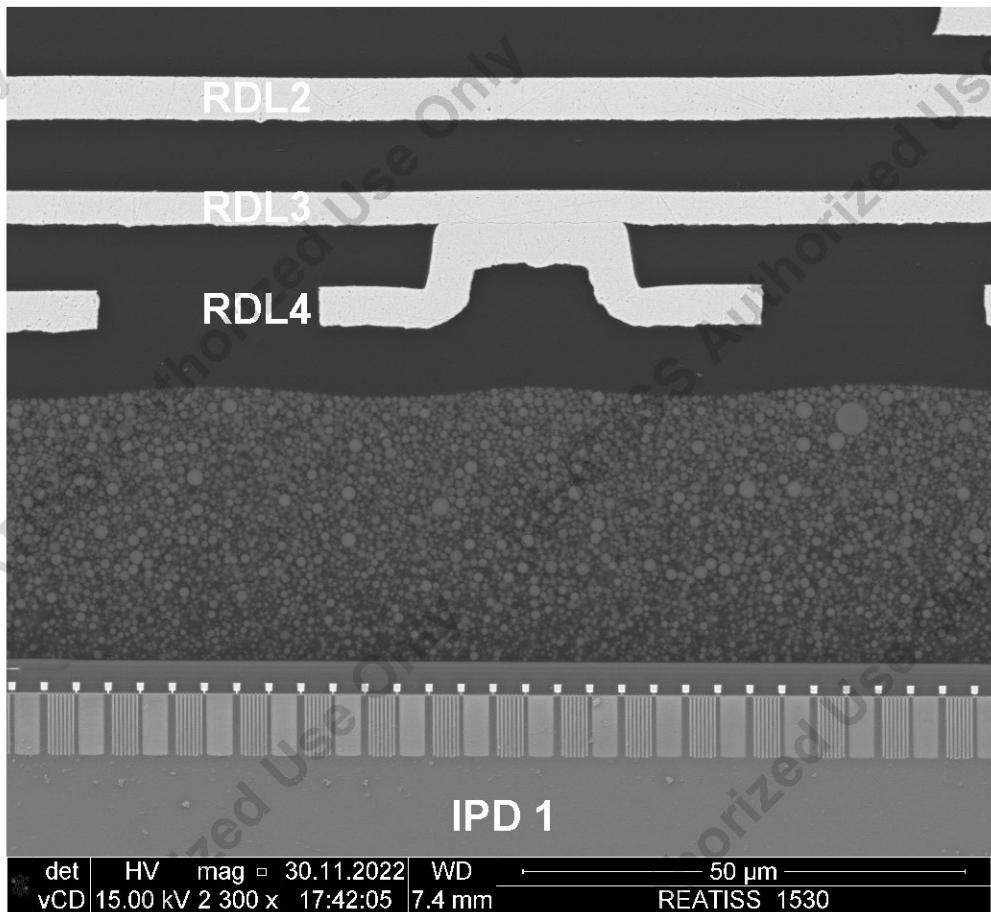


Figure 57. RDL2-RDL4, RDL via, IPD 1

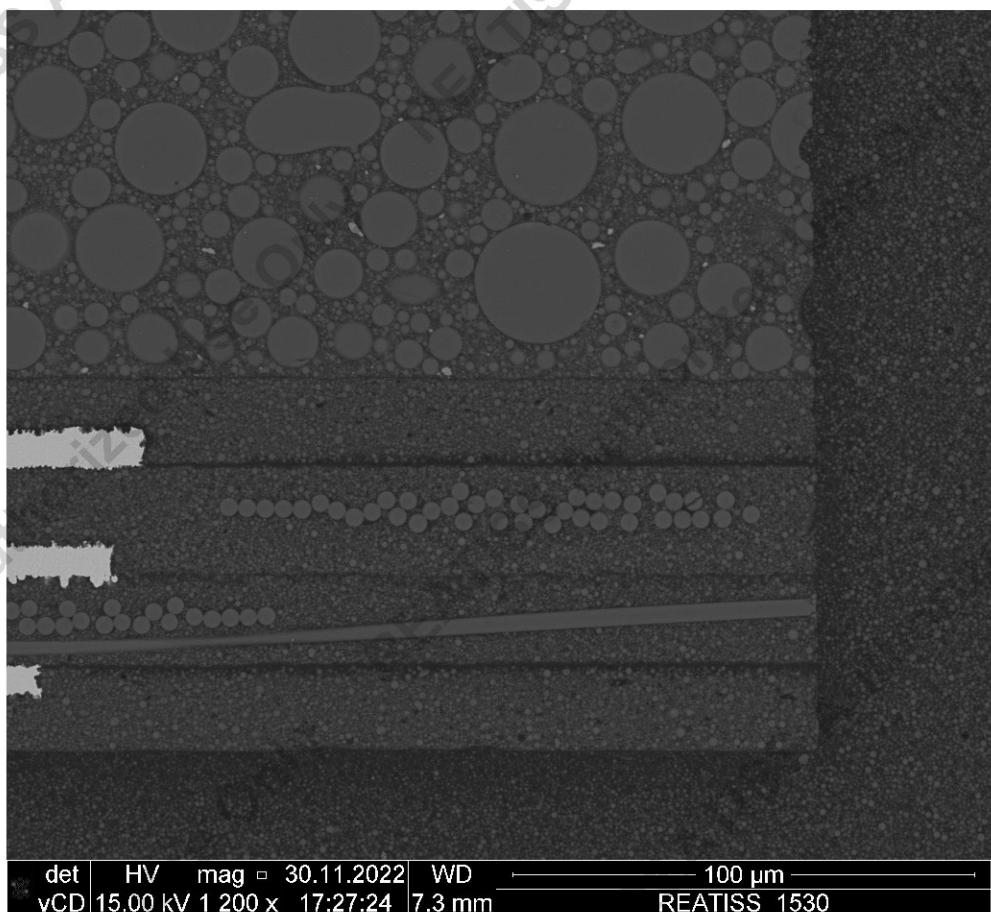


Figure 58. Memory package corner

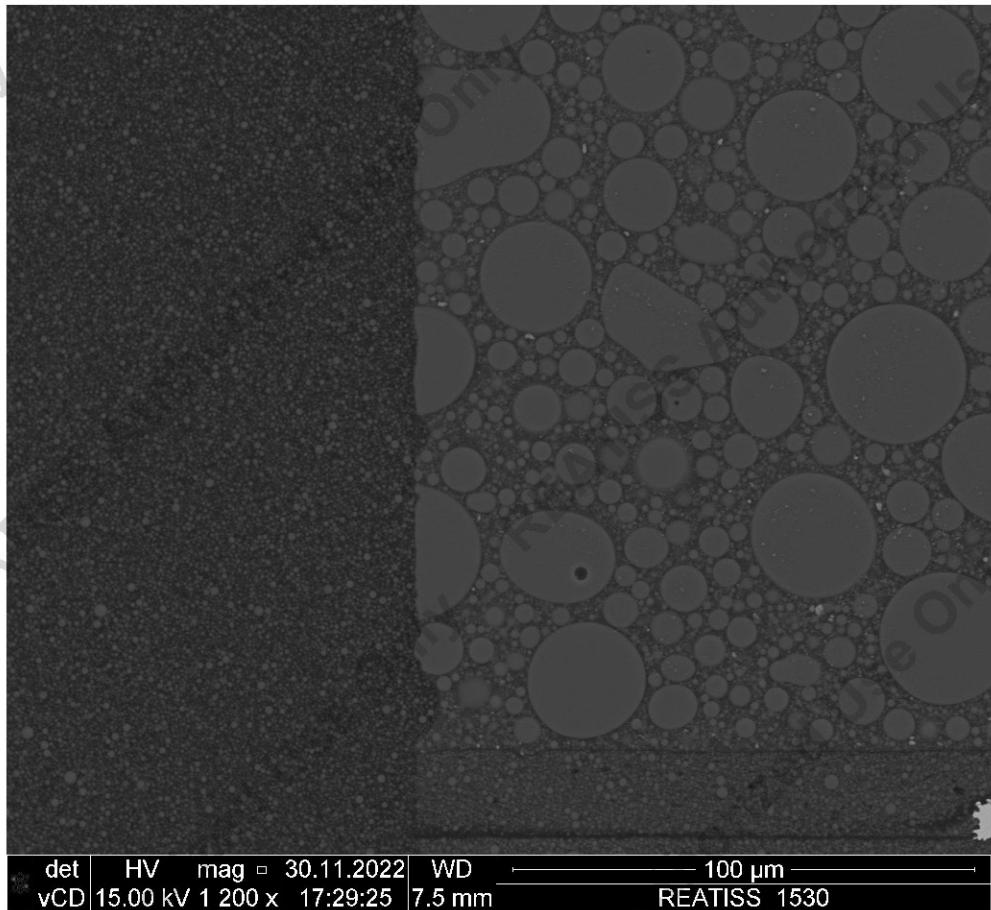


Figure 59. Memory package edge

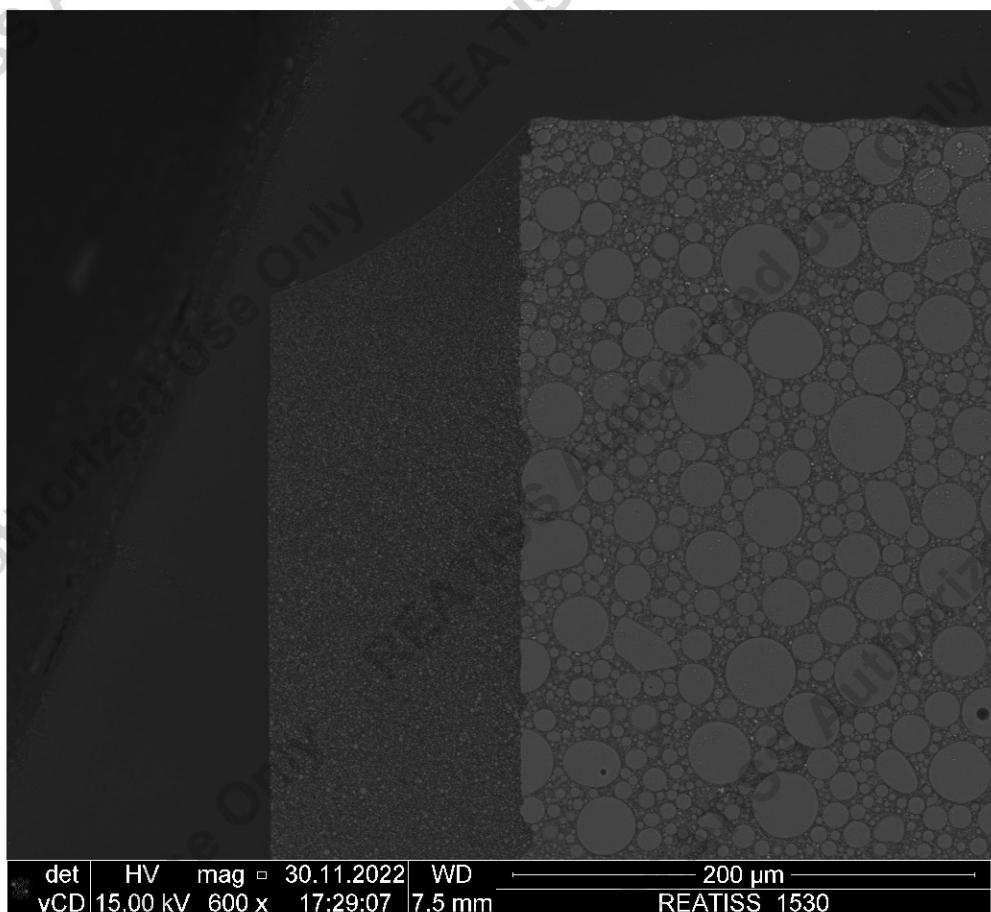


Figure 60. Memory package corner and top surface

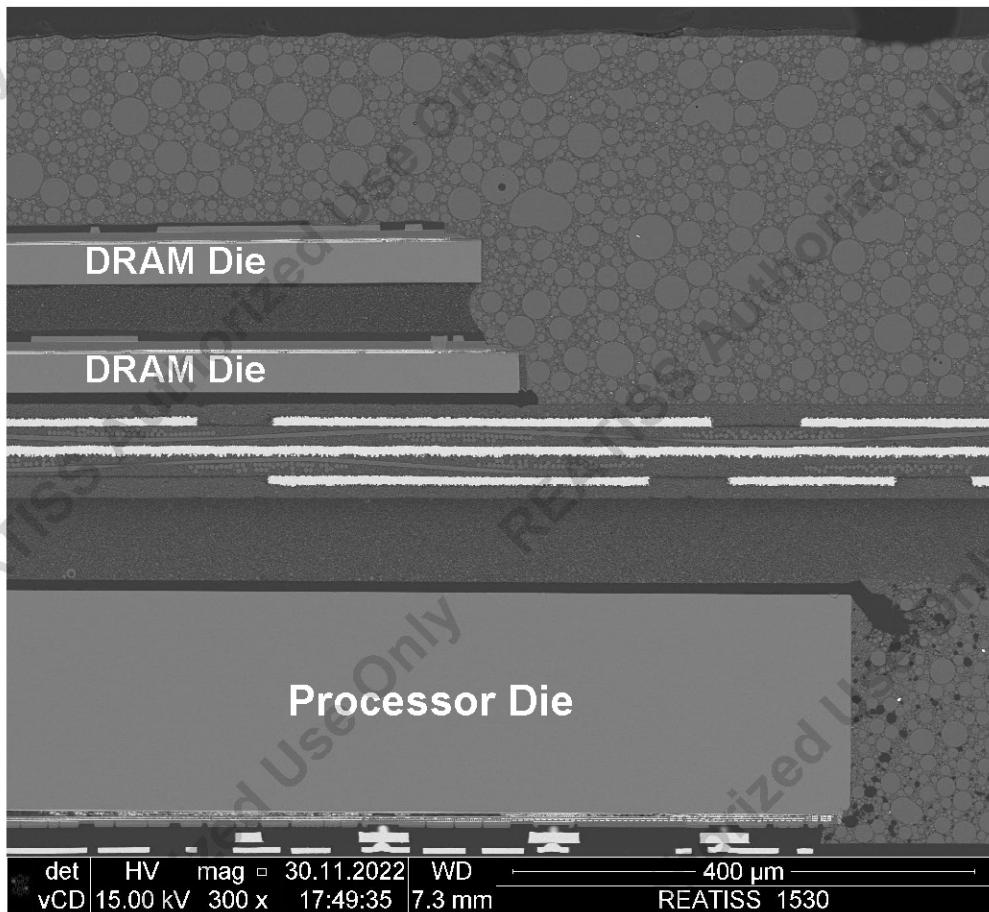


Figure 61. Memory dice and processor die assembly

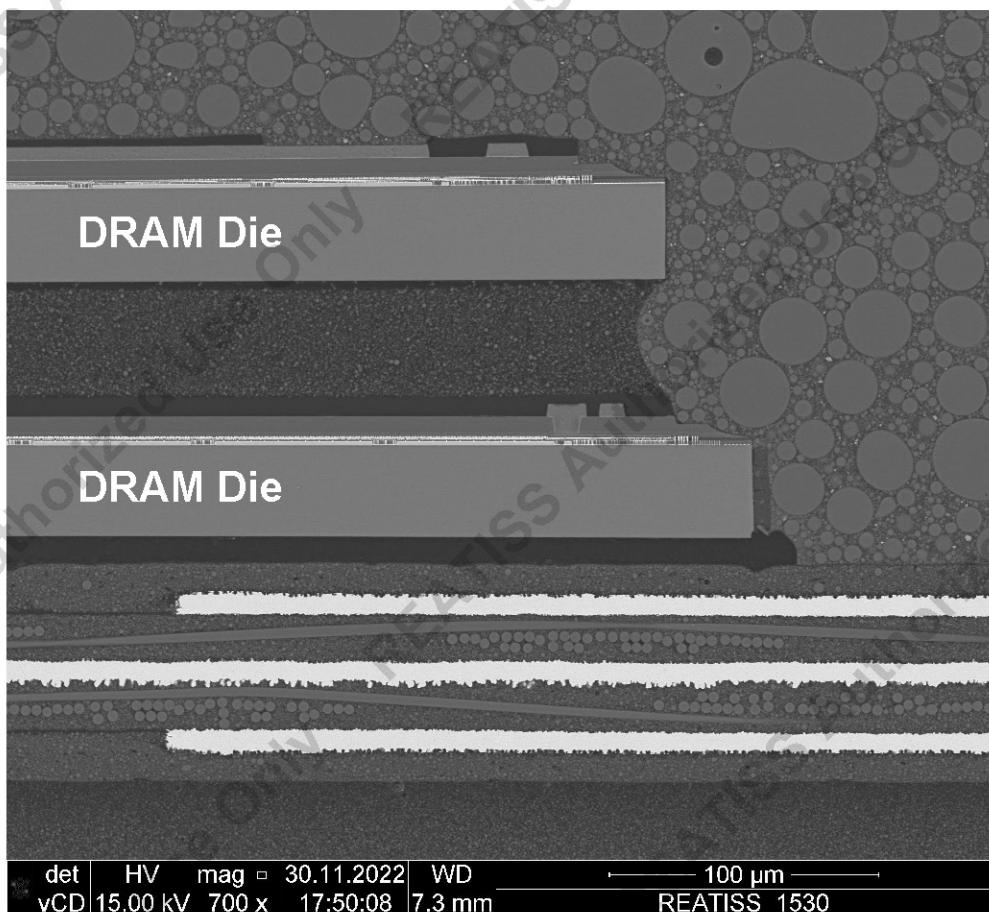


Figure 62. Memory dice assembly

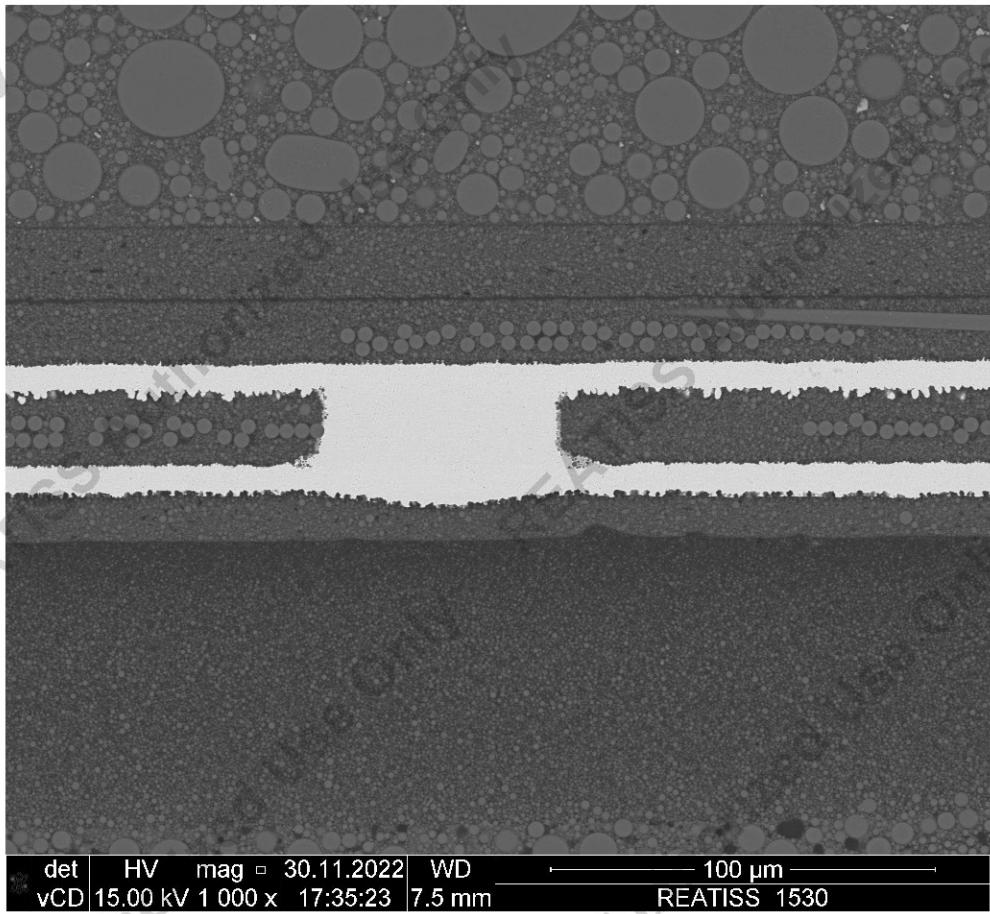


Figure 63. Memory package substrate via

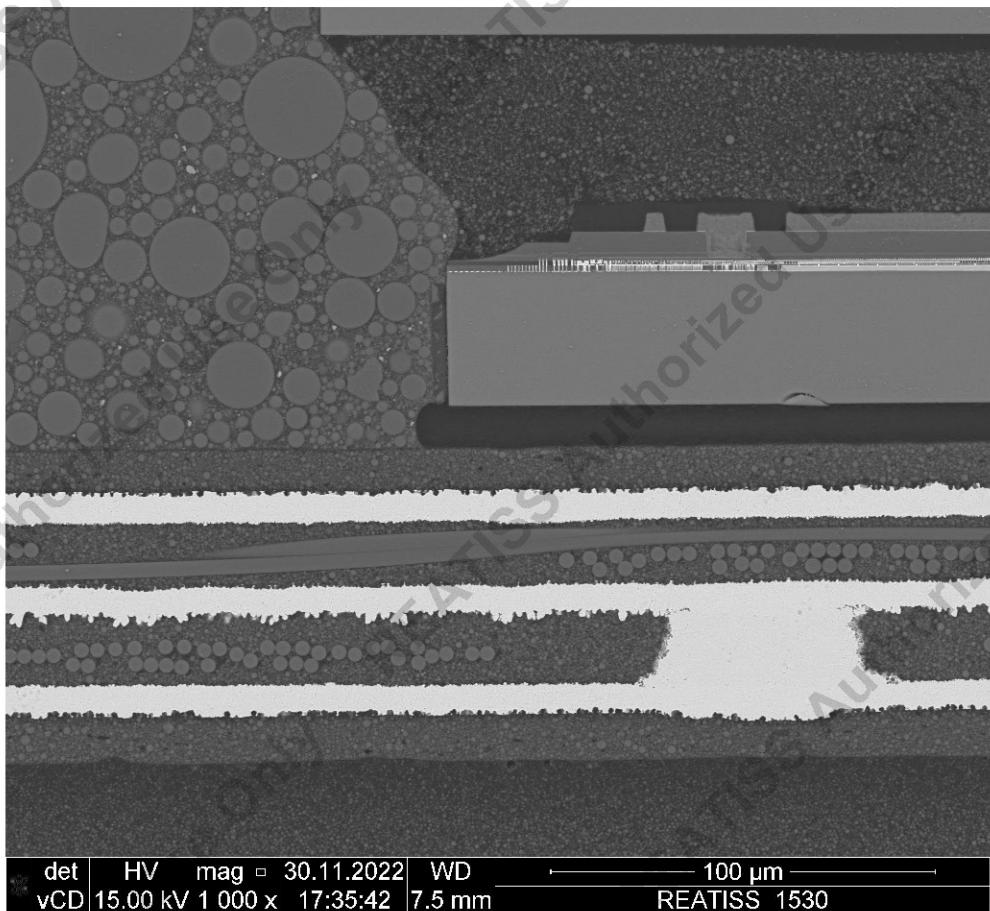


Figure 64. Bottom memory die and substrate via

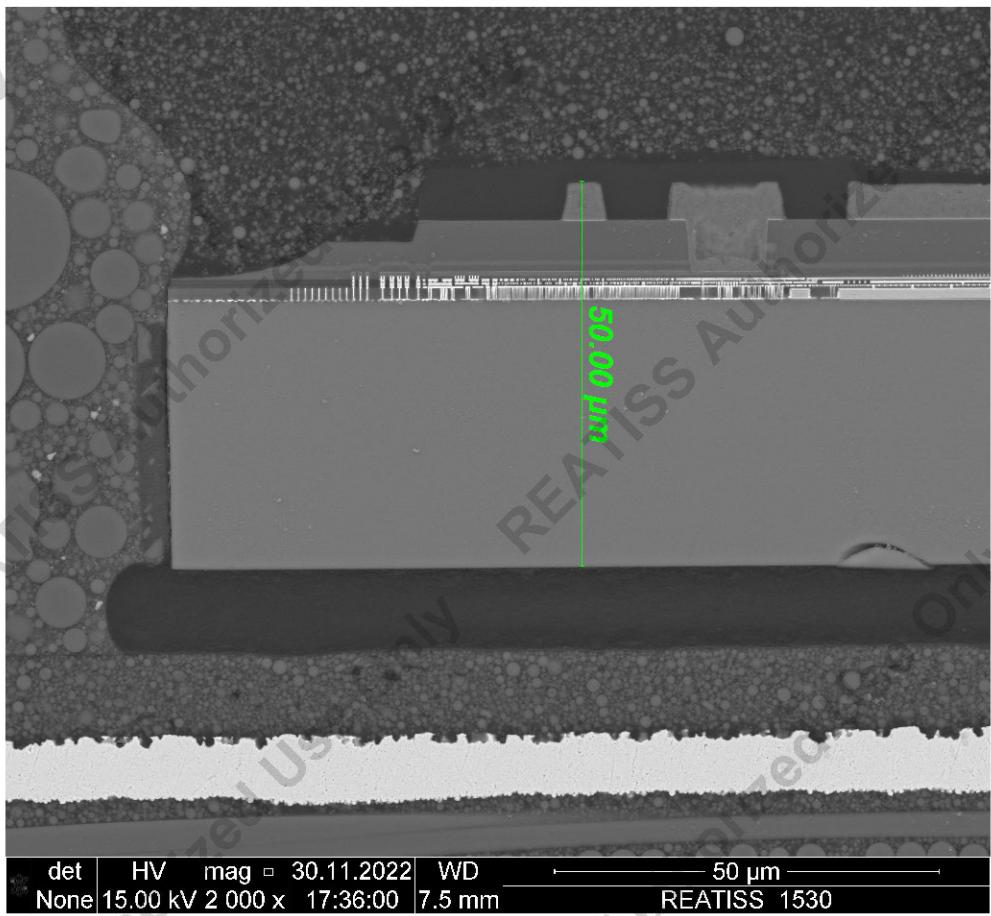


Figure 65. Bottom memory die assembly and encapsulation

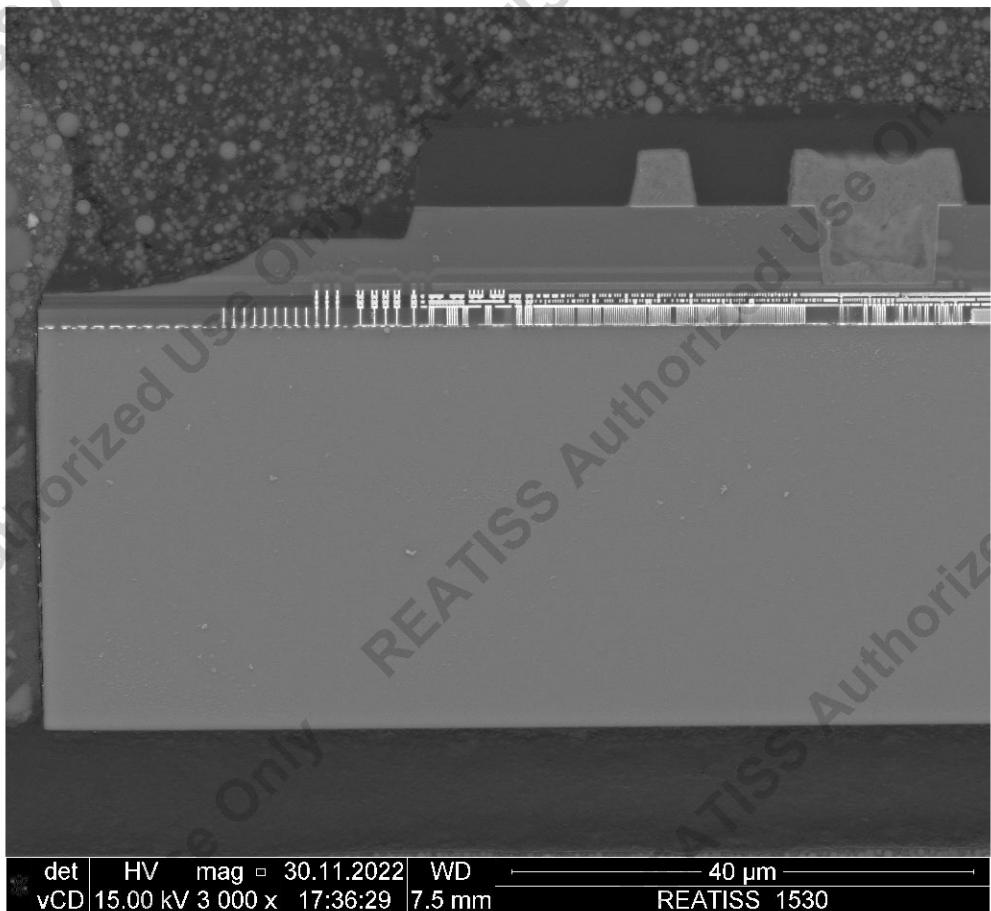


Figure 66. Bottom memory die assembly and encapsulation

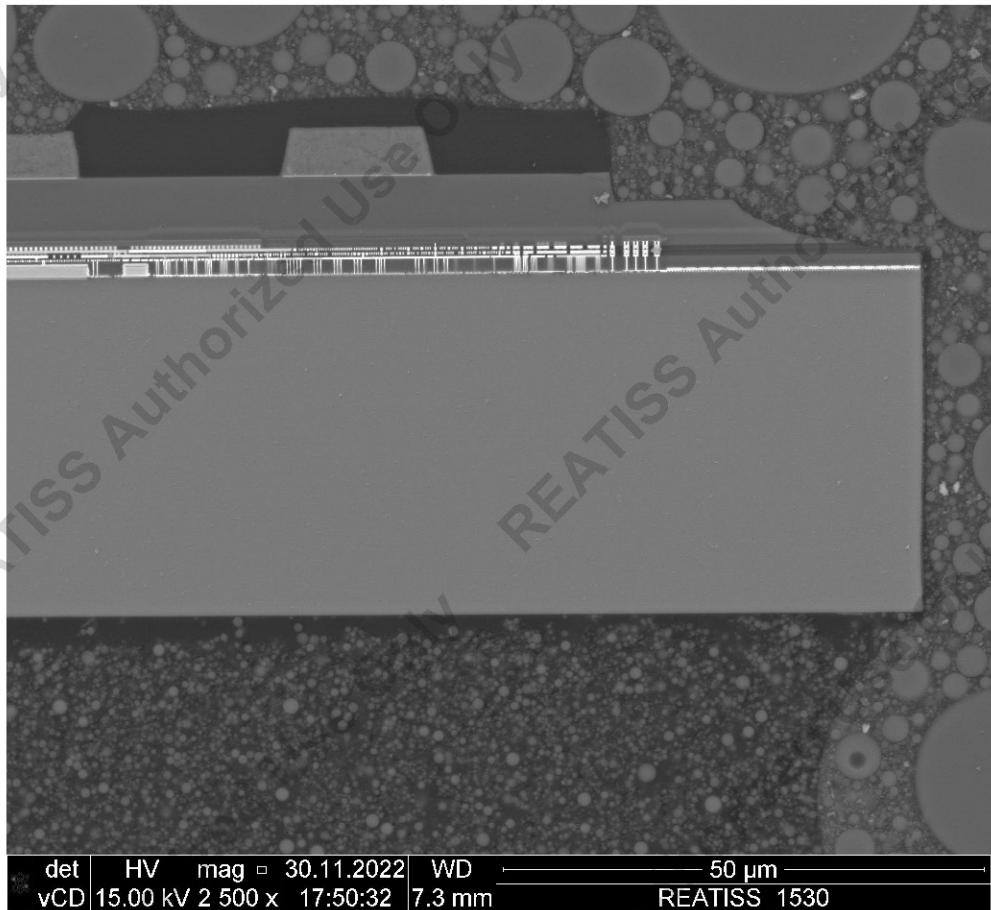


Figure 67. Top memory die assembly

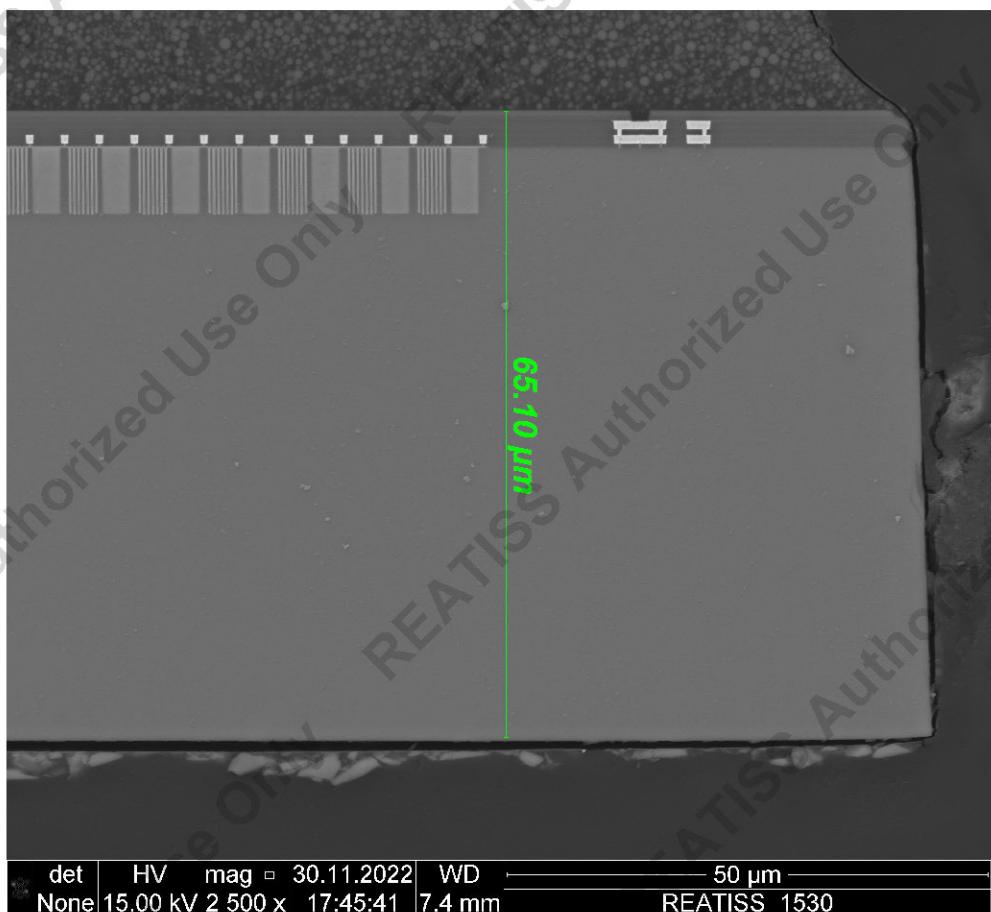


Figure 68. IPD 1 die assembly



Figure 69. IPD 1 die assembly

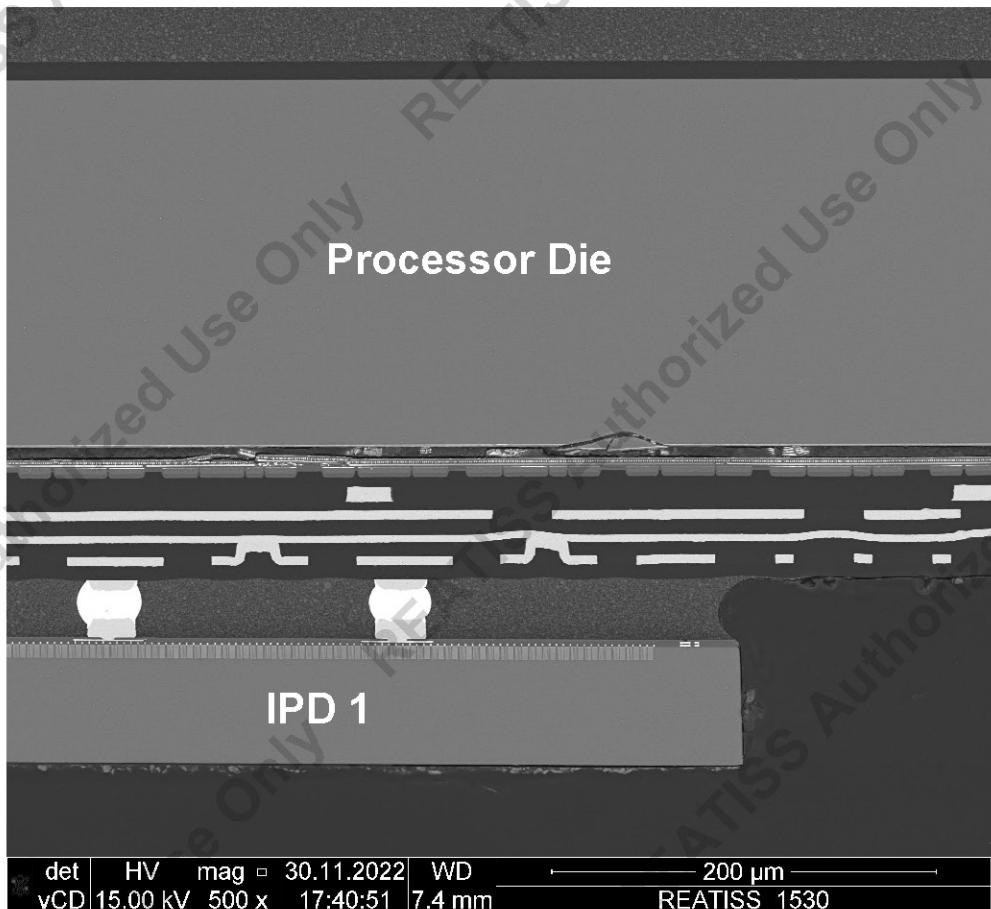


Figure 70. IPD 1 connection to RDL

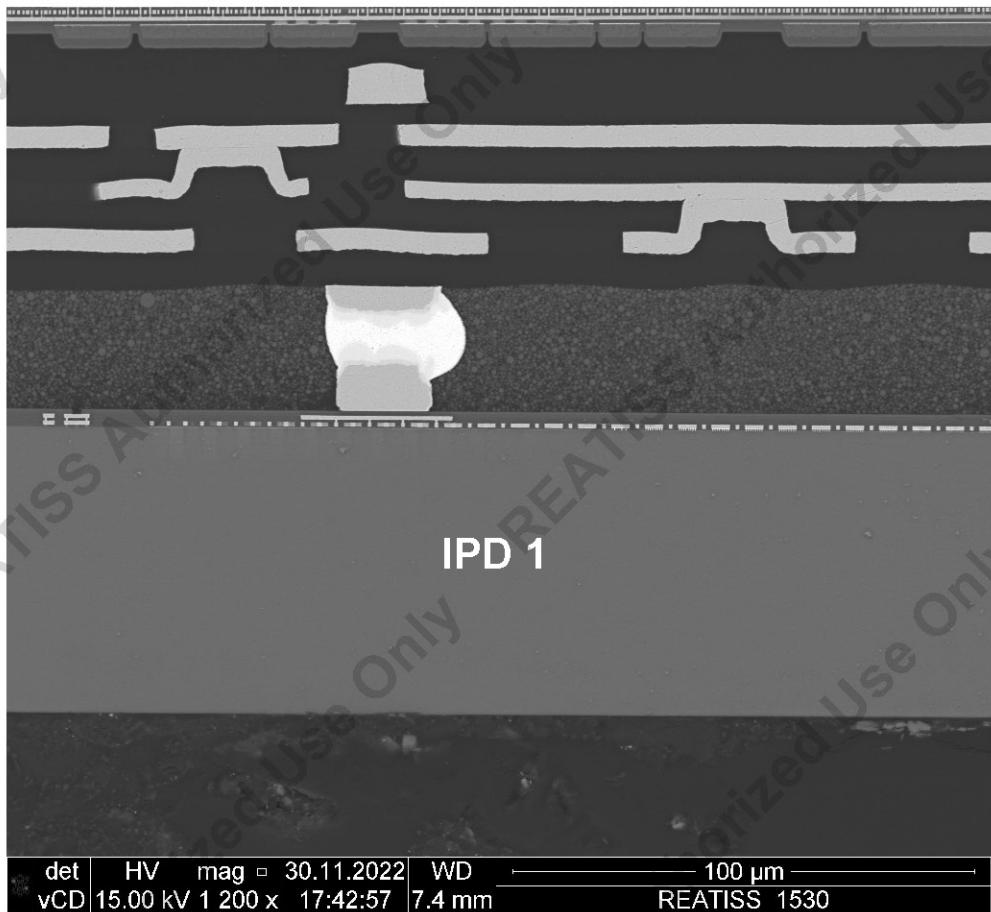


Figure 71. IPD 1 connection to RDL

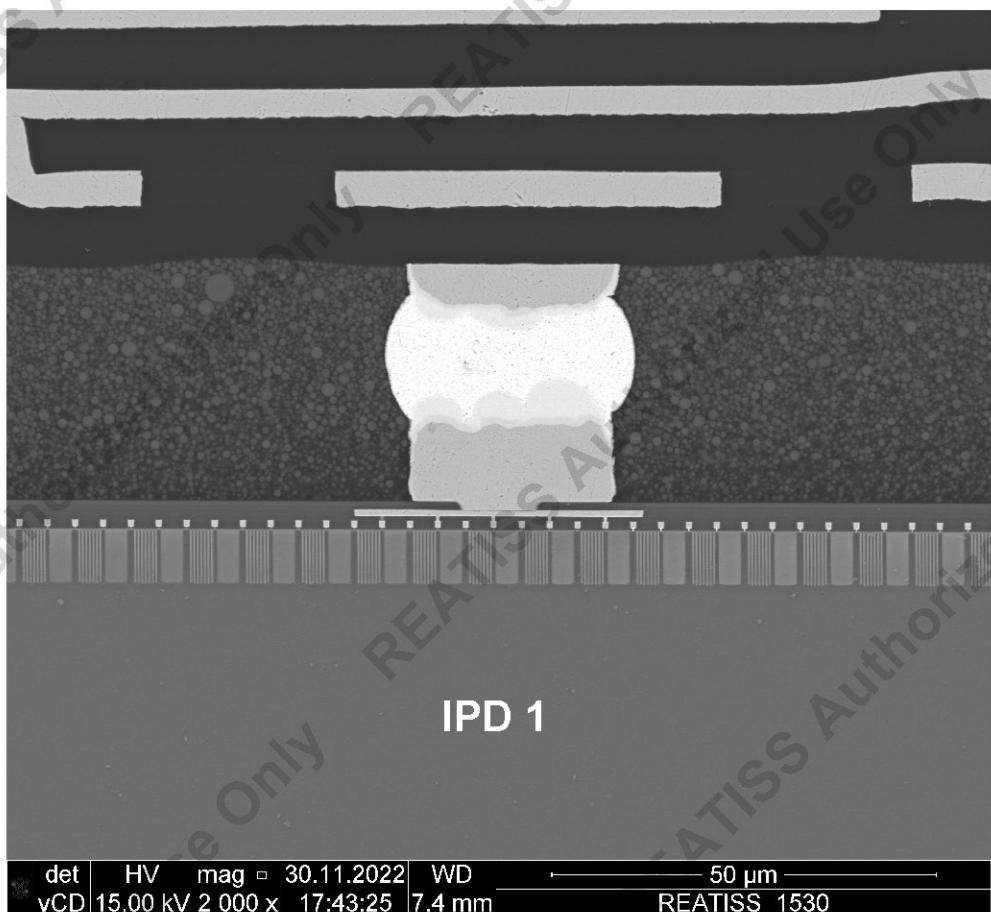


Figure 72. IPD 1 bond pad and copper pillar

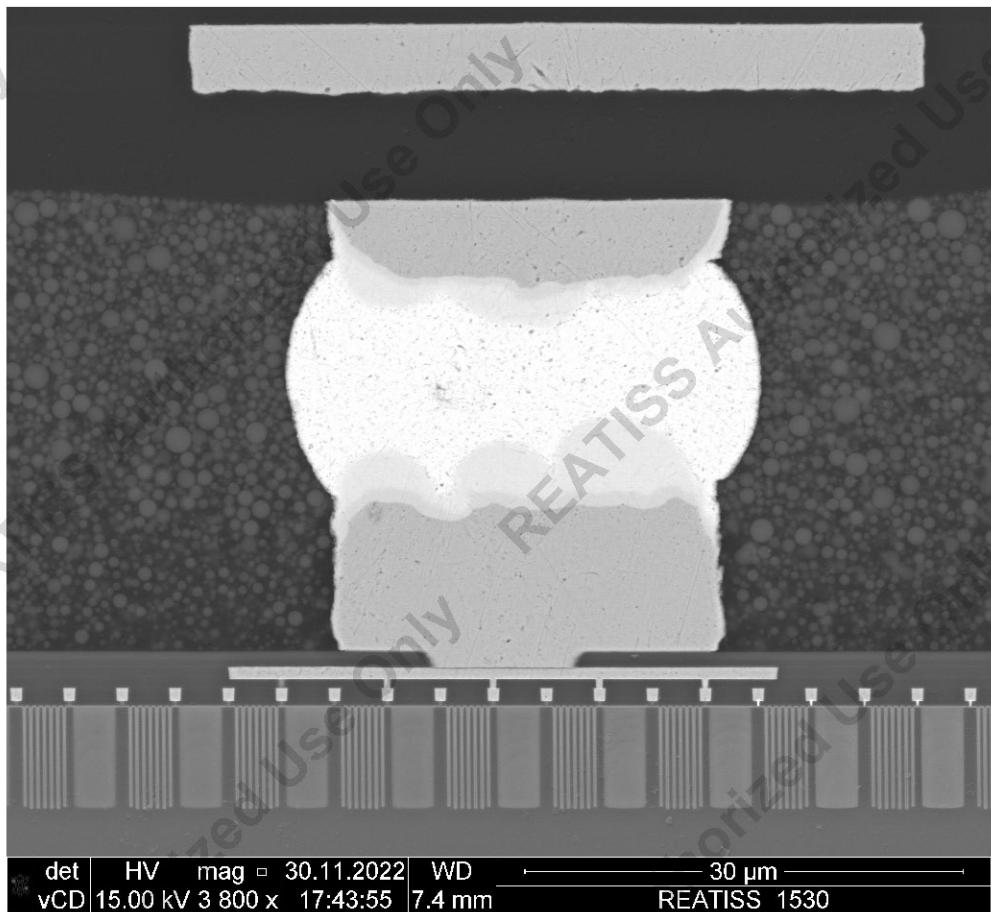


Figure 73. IPD 1 bond pad and copper pillar

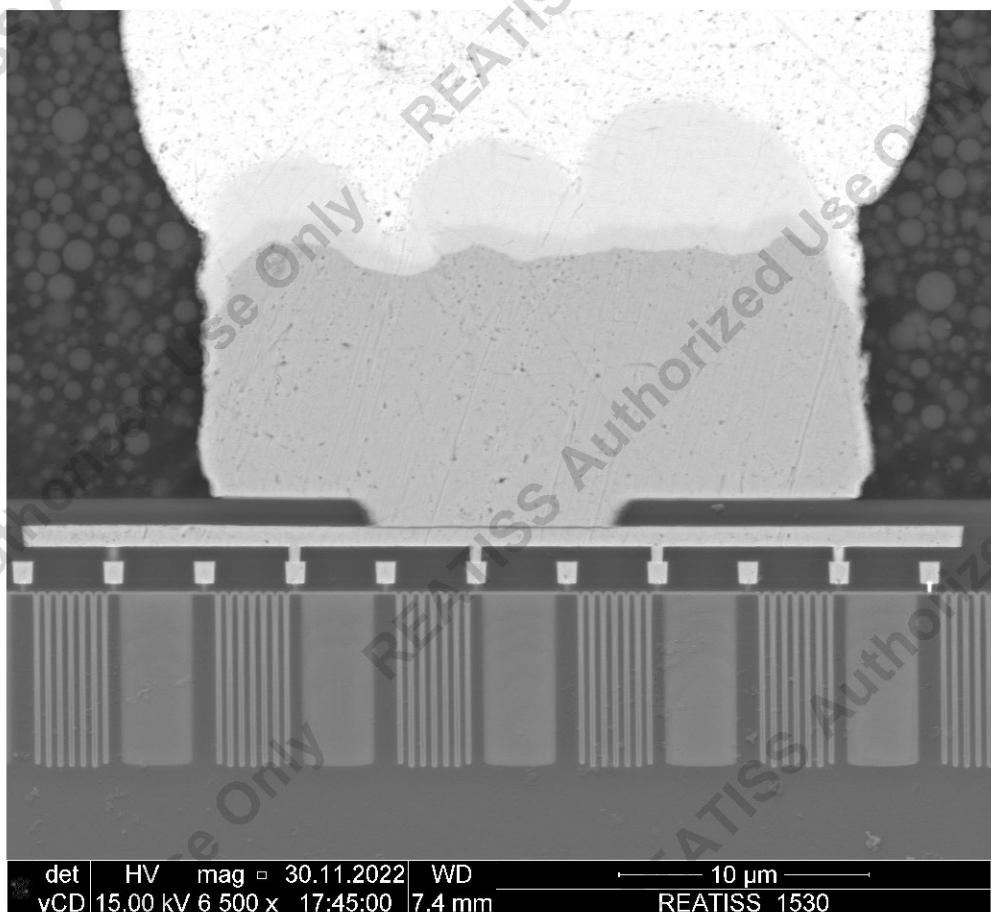


Figure 74. IPD 1 bond pad and copper pillar

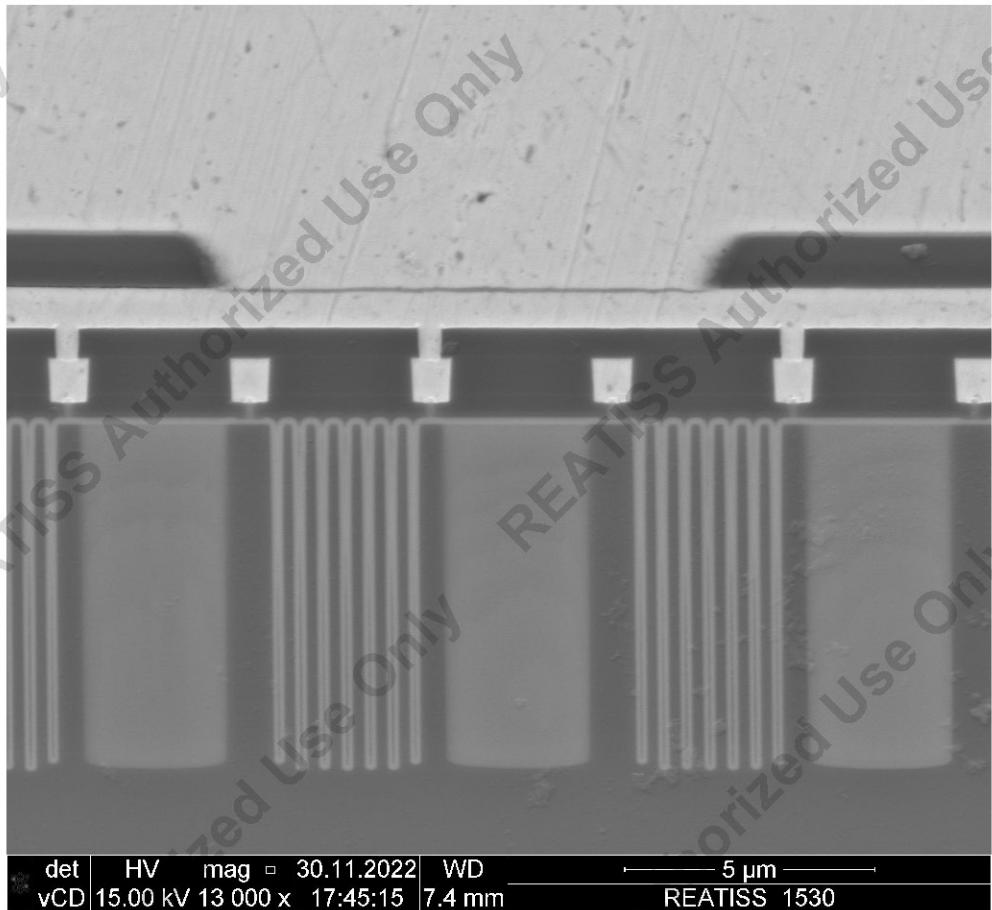


Figure 75. IPD 1 bond pad connection to copper pillar

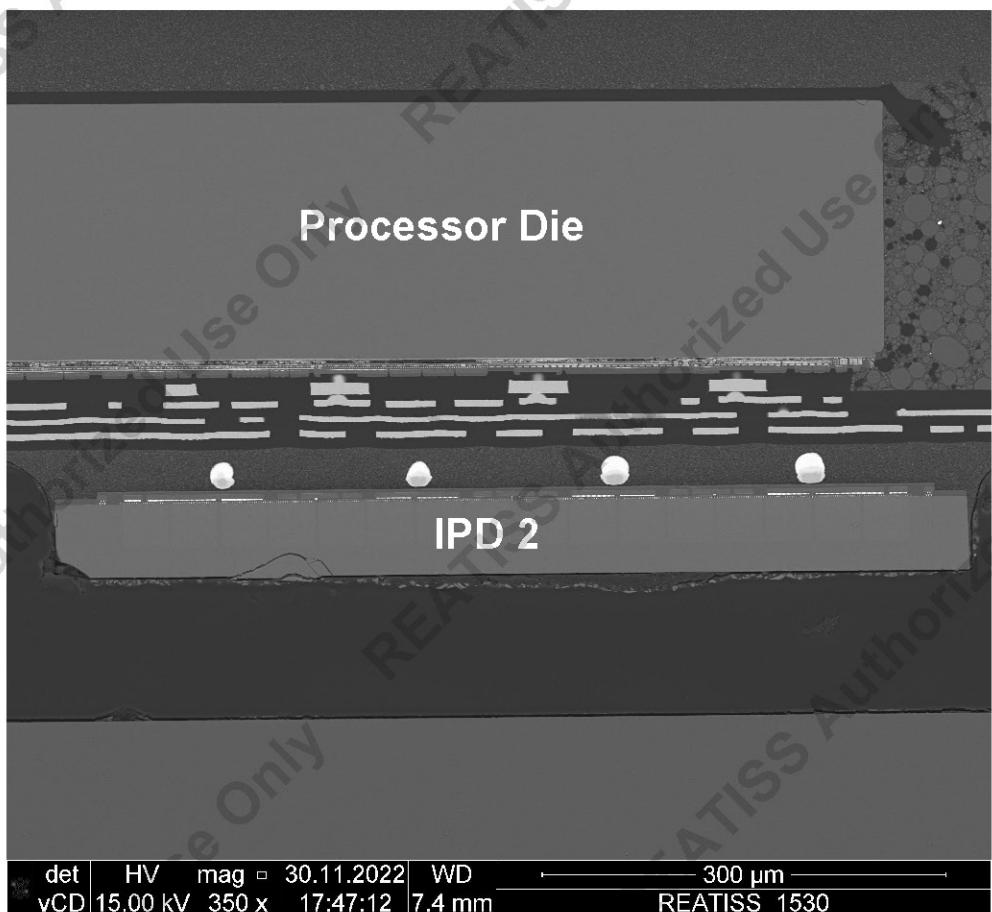


Figure 76. IPD 2 and processor die

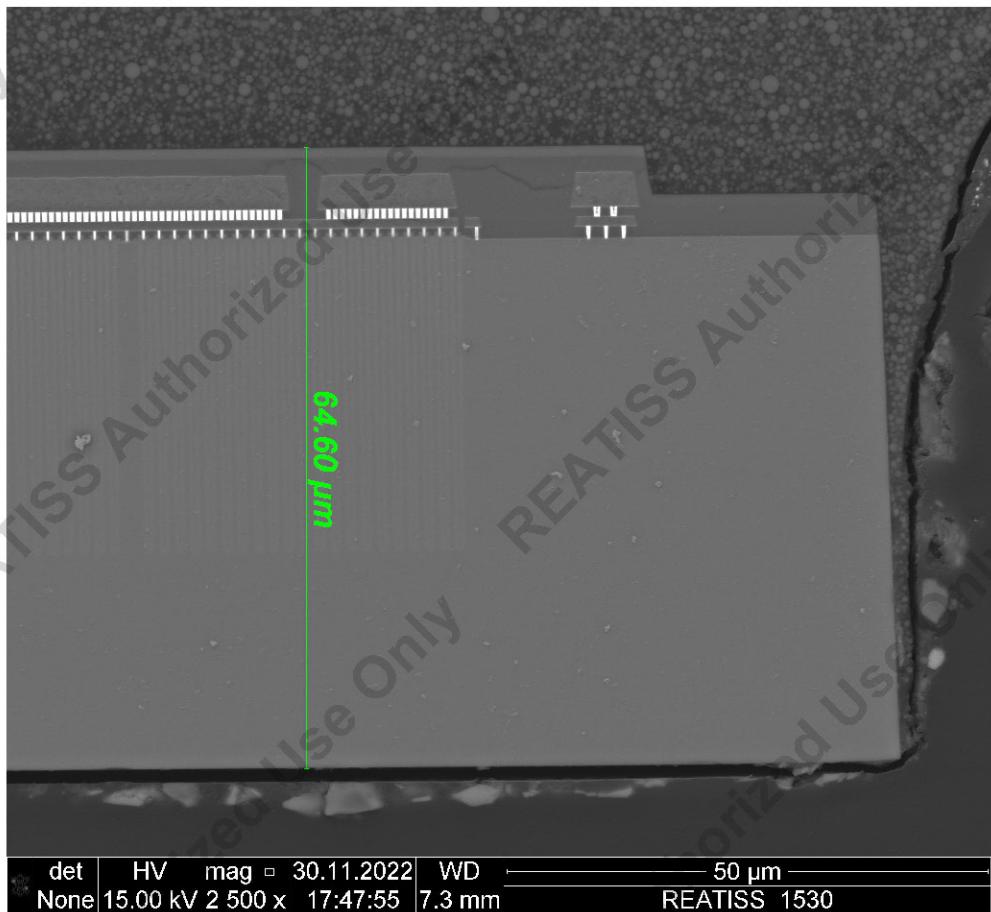


Figure 77. IPD 2 die assembly

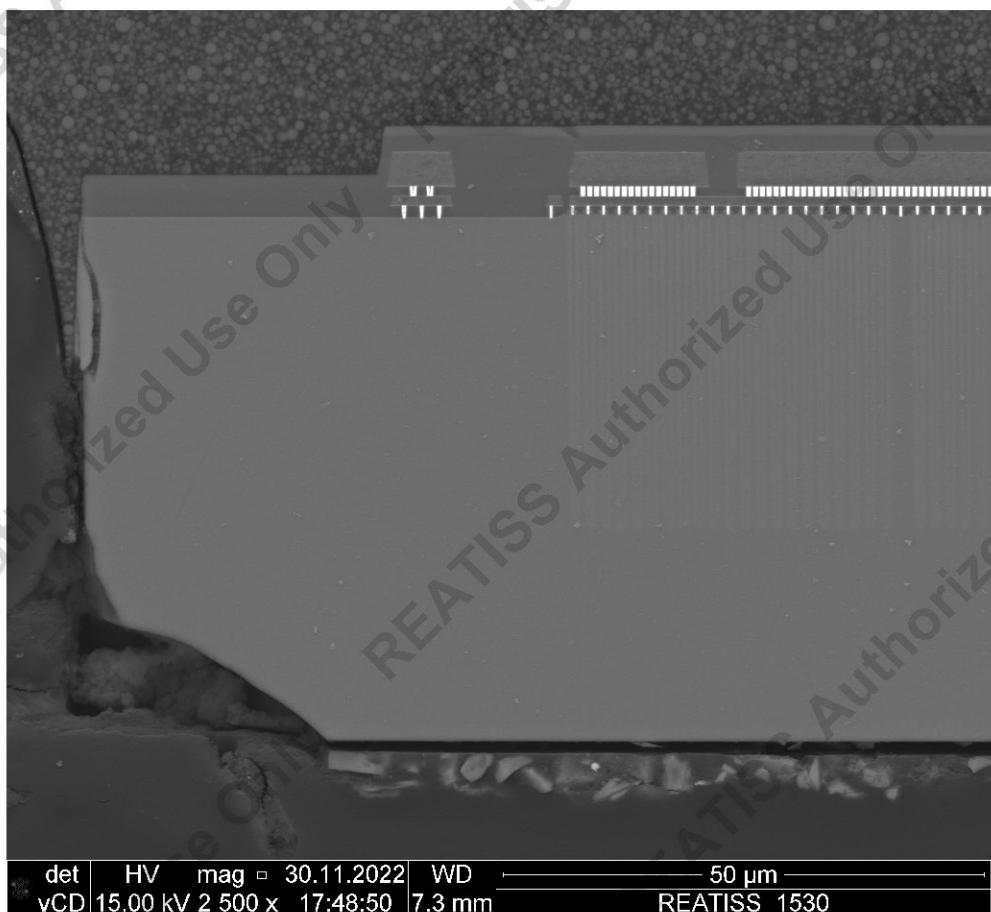


Figure 78. IPD 2 die assembly

Package Material Analysis

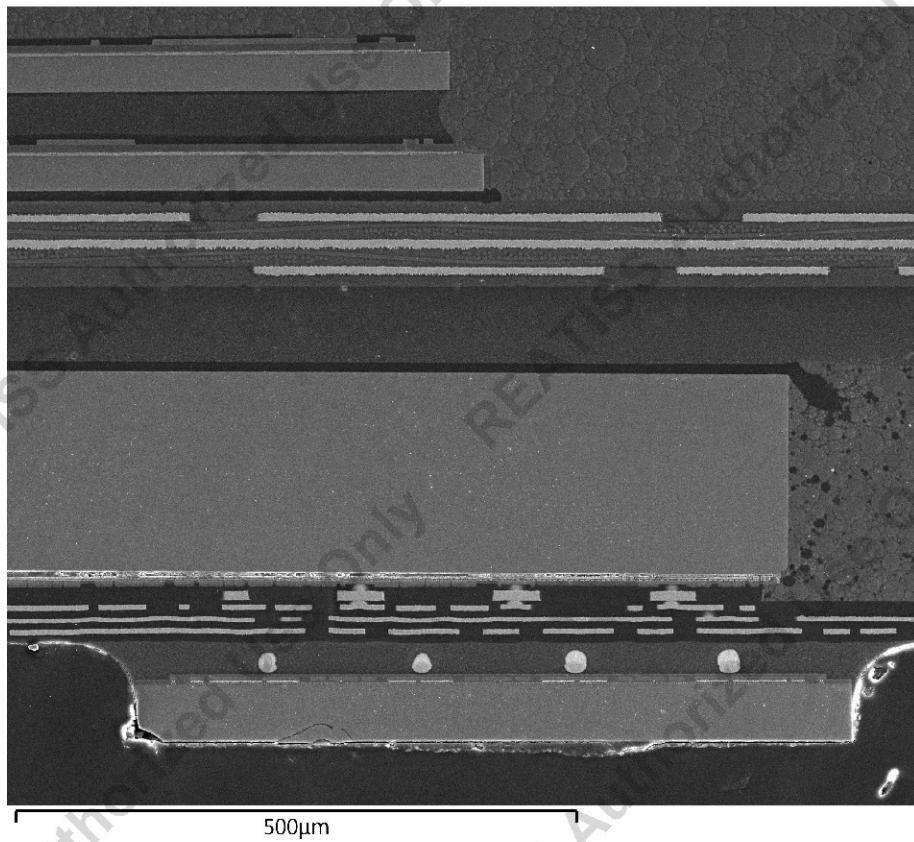


Figure 79. Dice assembly

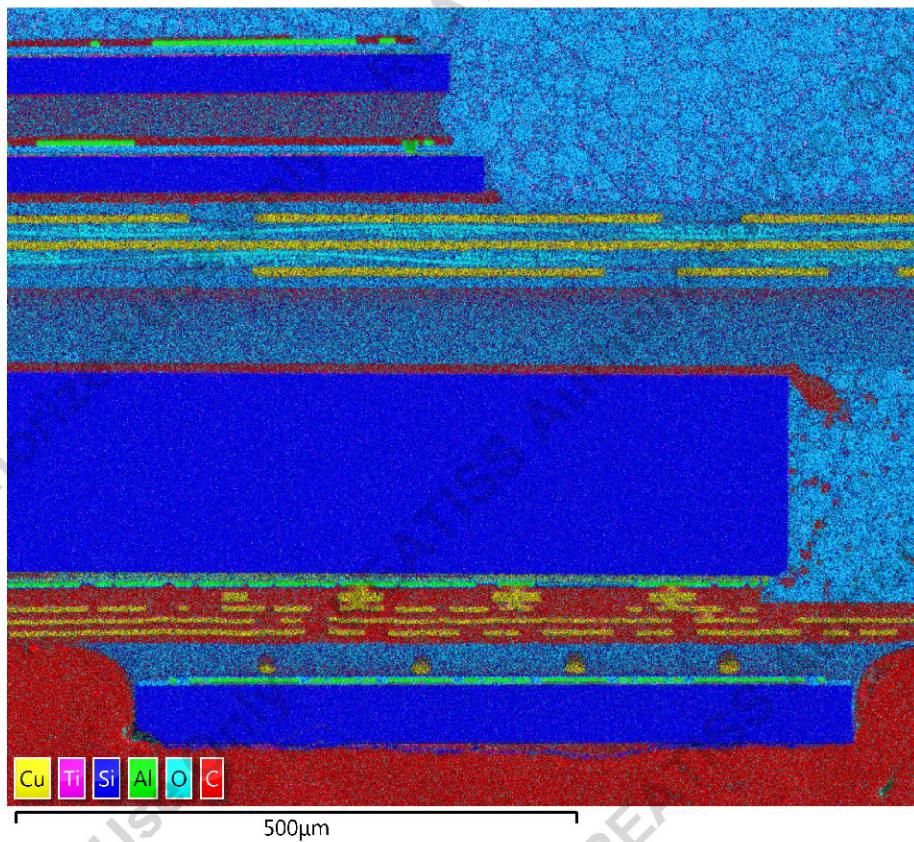


Figure 80. Layered EDX map of dice assembly

Cu K series

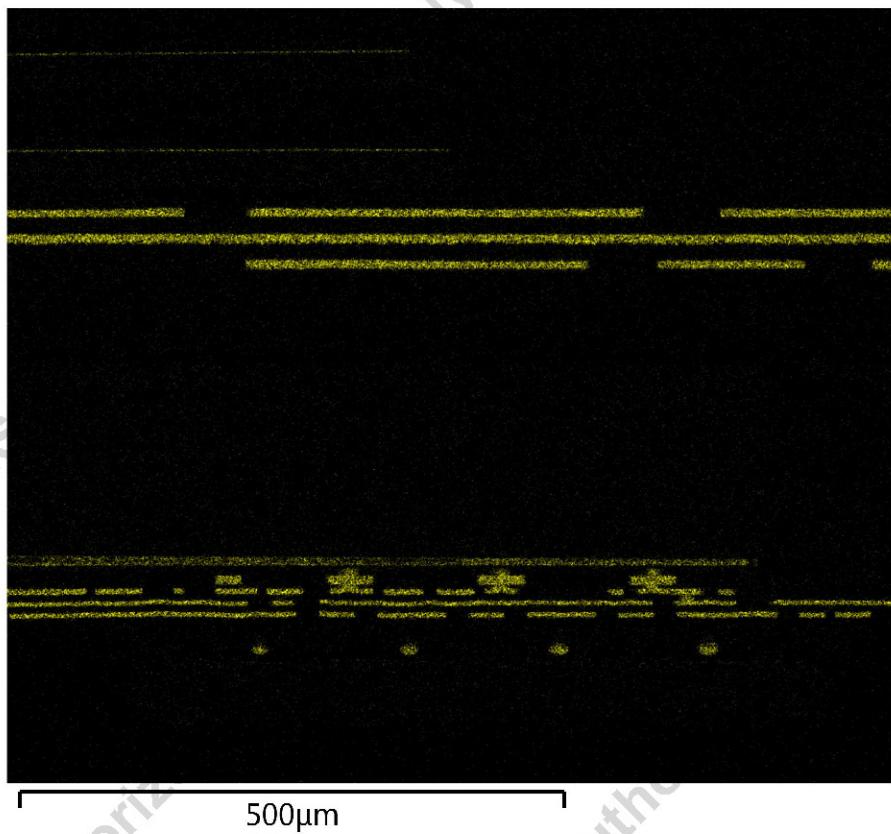


Figure 81. Copper EDX map layer

Ti K series

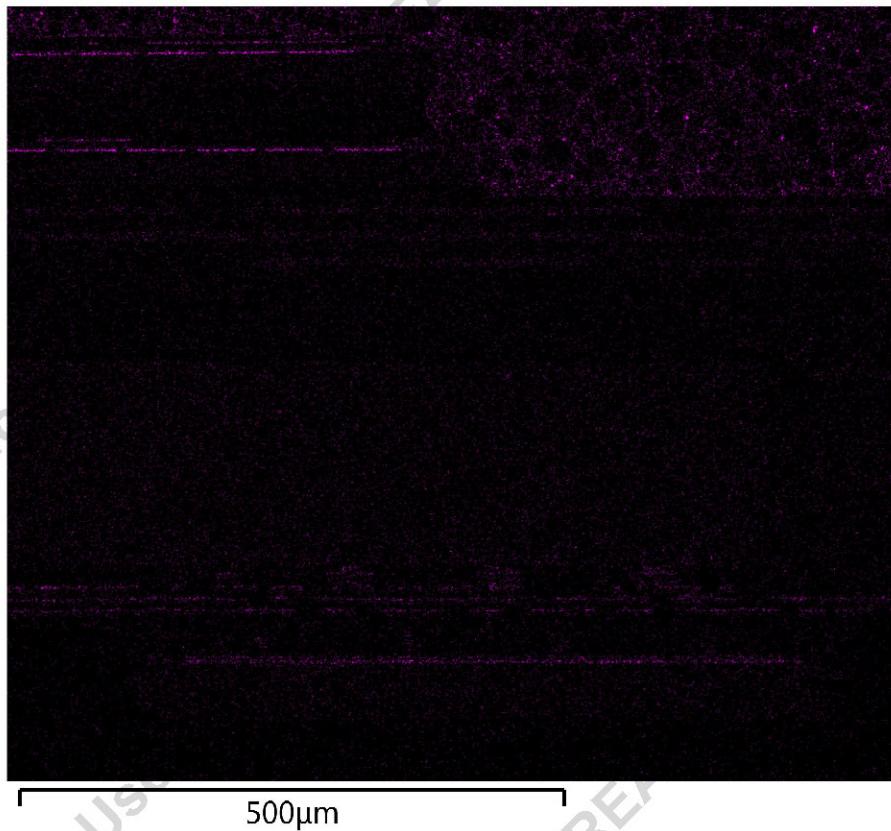


Figure 82. Titanium EDX map layer

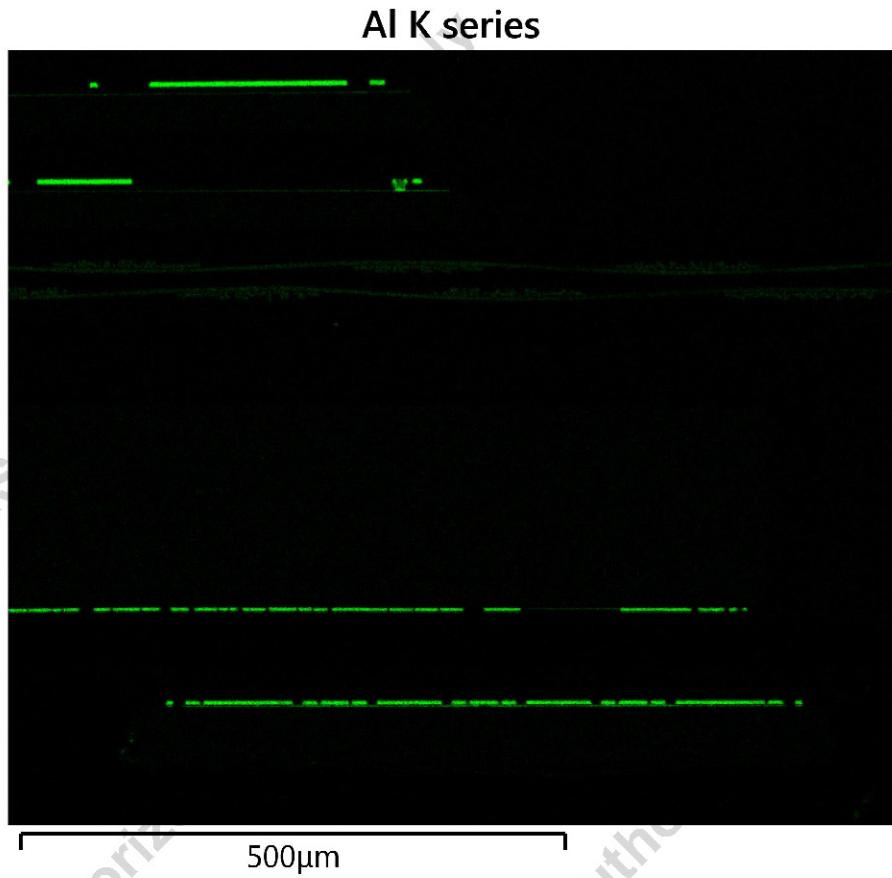


Figure 83. Aluminum EDX map layer

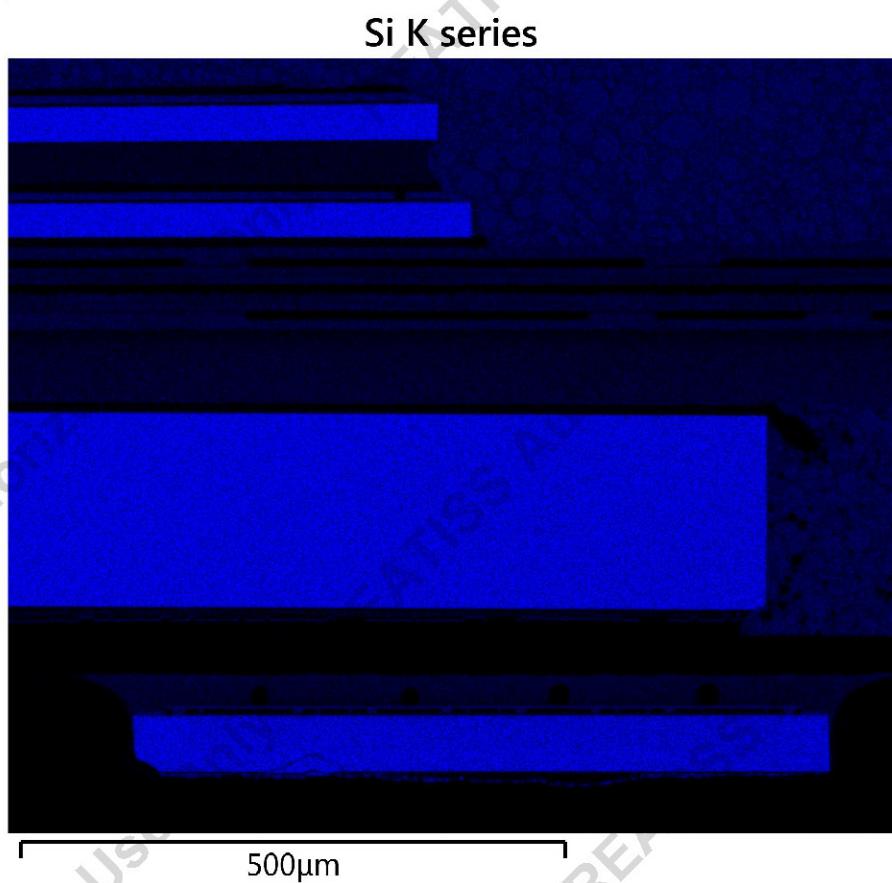


Figure 84. Silicon EDX map layer

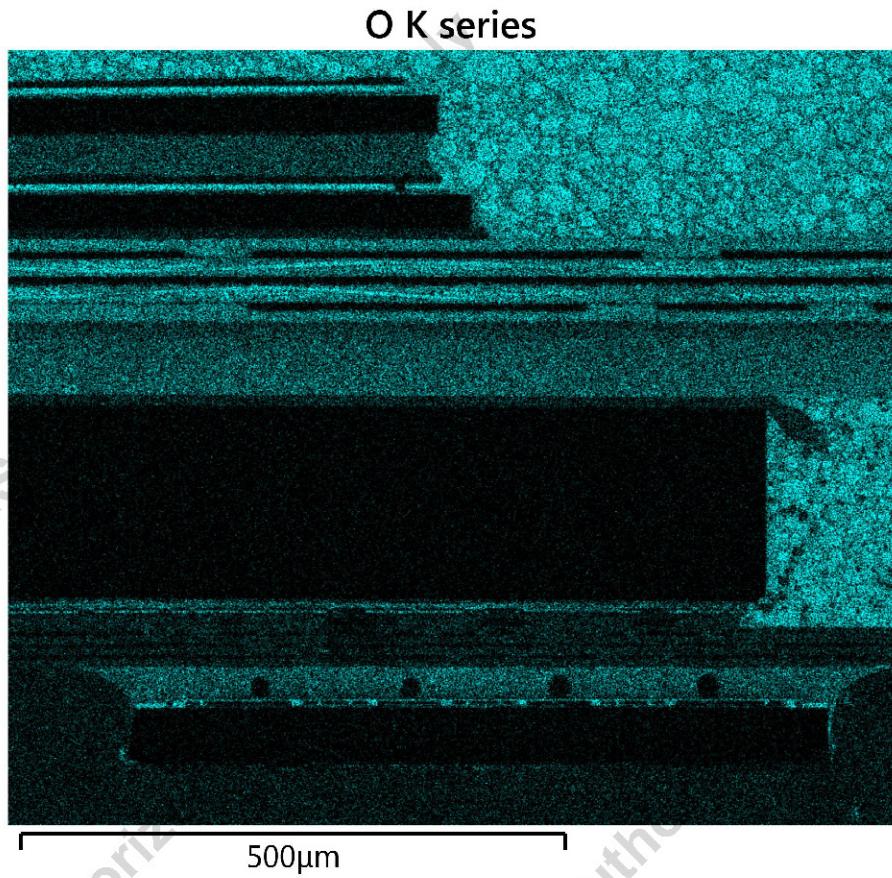


Figure 85. Oxygen EDX map layer

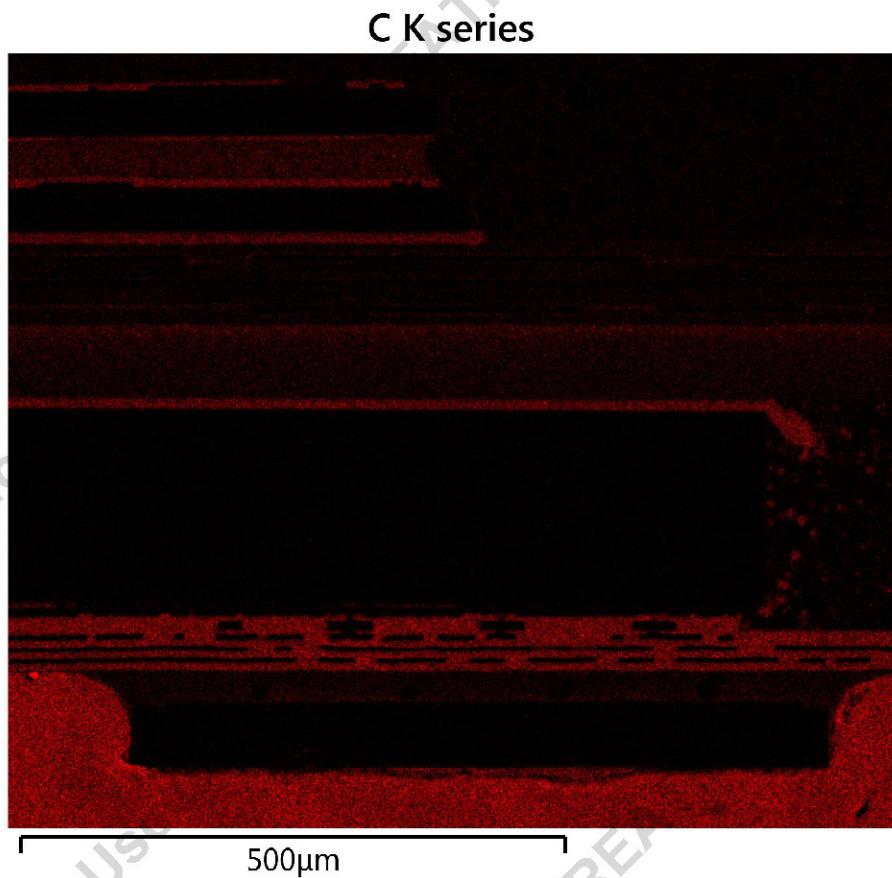


Figure 86. Carbon EDX map layer

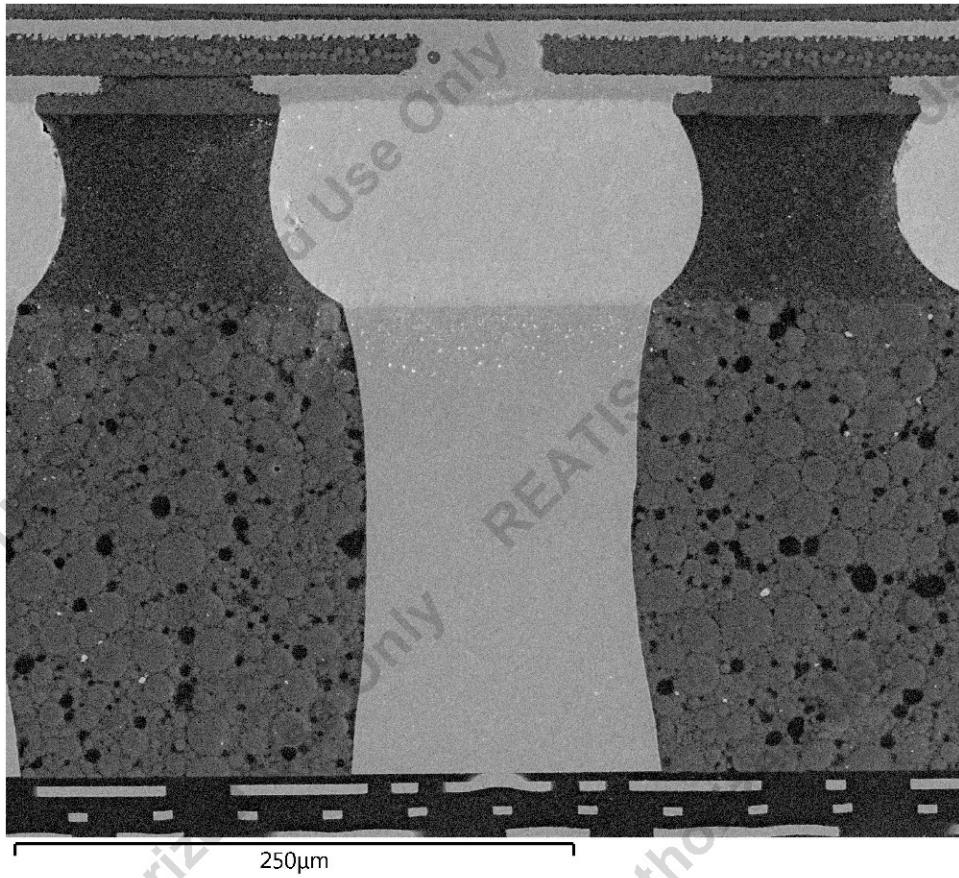


Figure 87. Memory package PCB to through InFO via connection

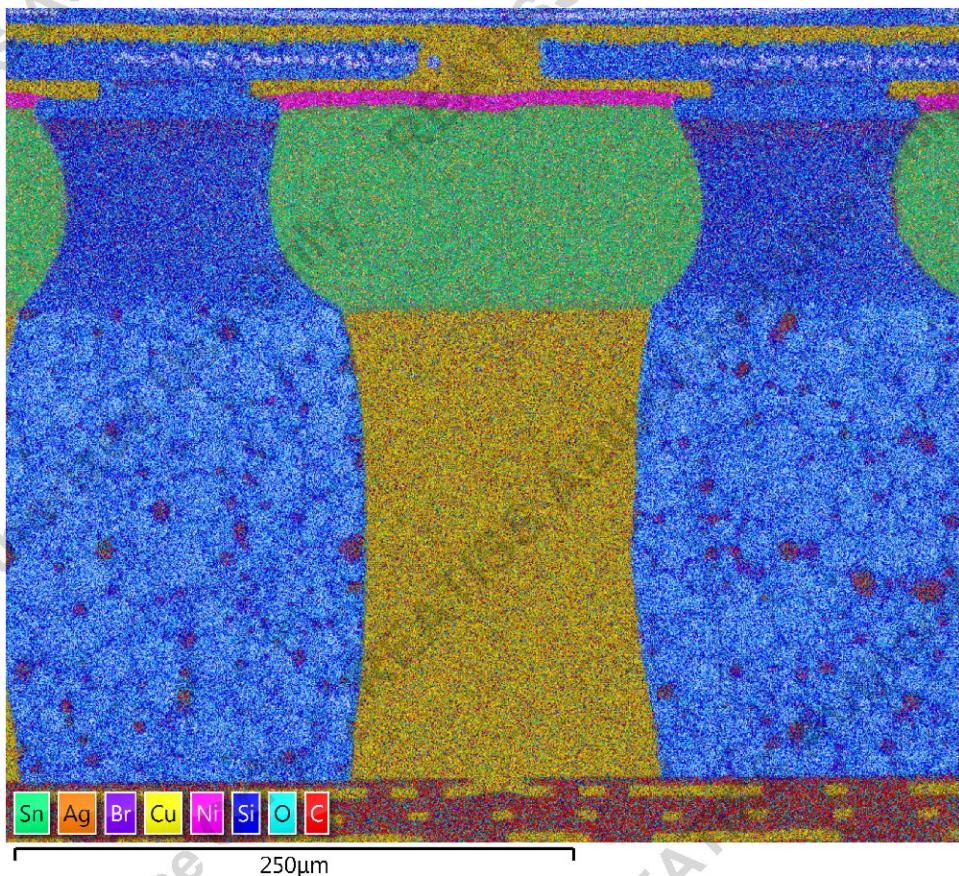


Figure 88. Layered EDX map of memory package PCB to through InFO via connection

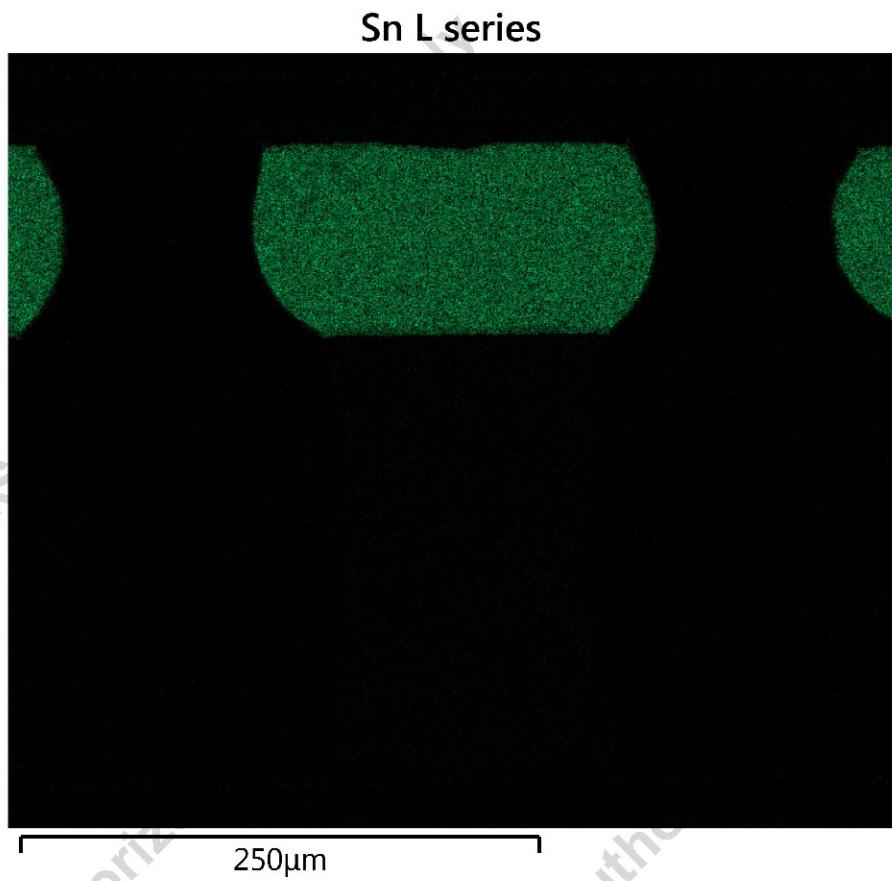


Figure 89. Tin EDX map layer

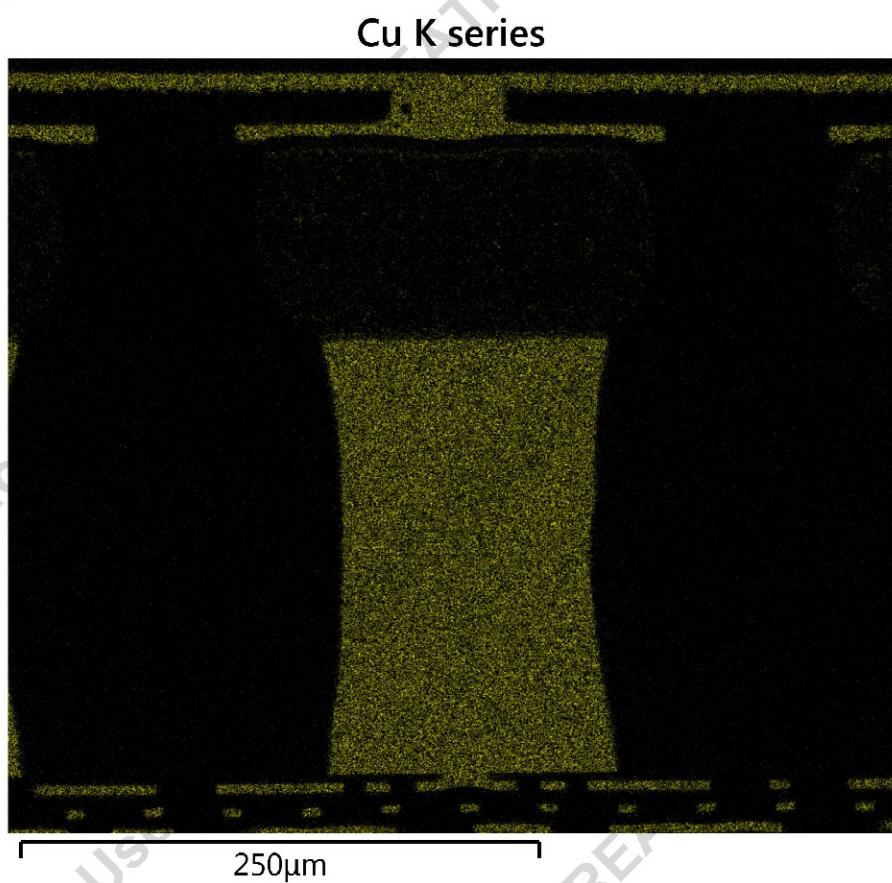


Figure 90. Copper EDX map layer

Ag L series

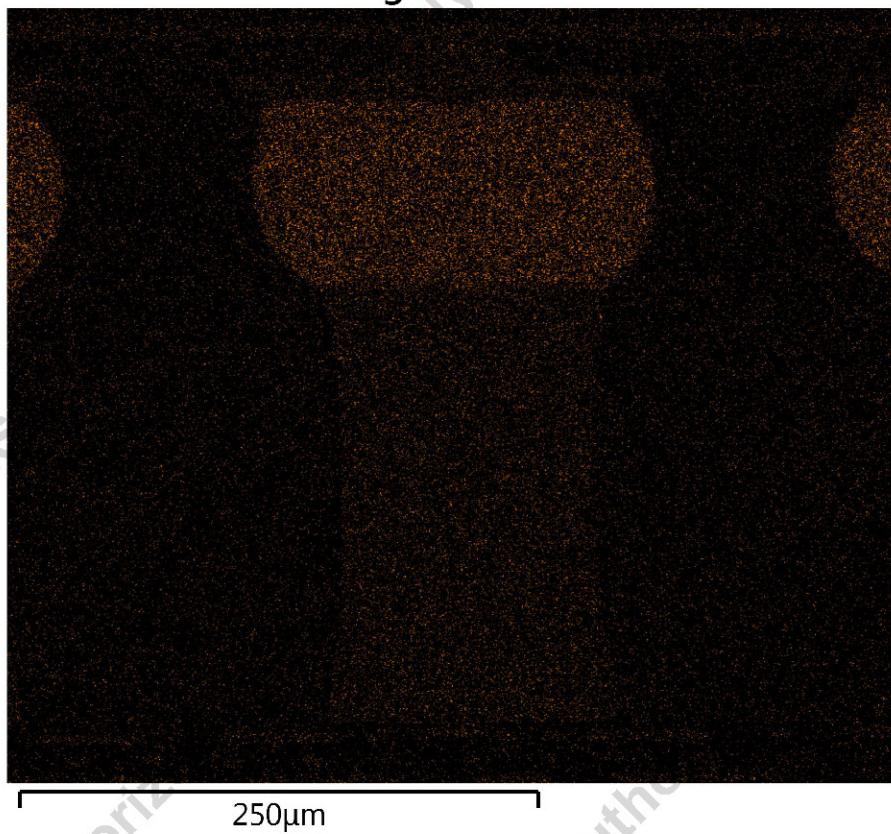


Figure 91. Silver EDX map layer

Ni K series

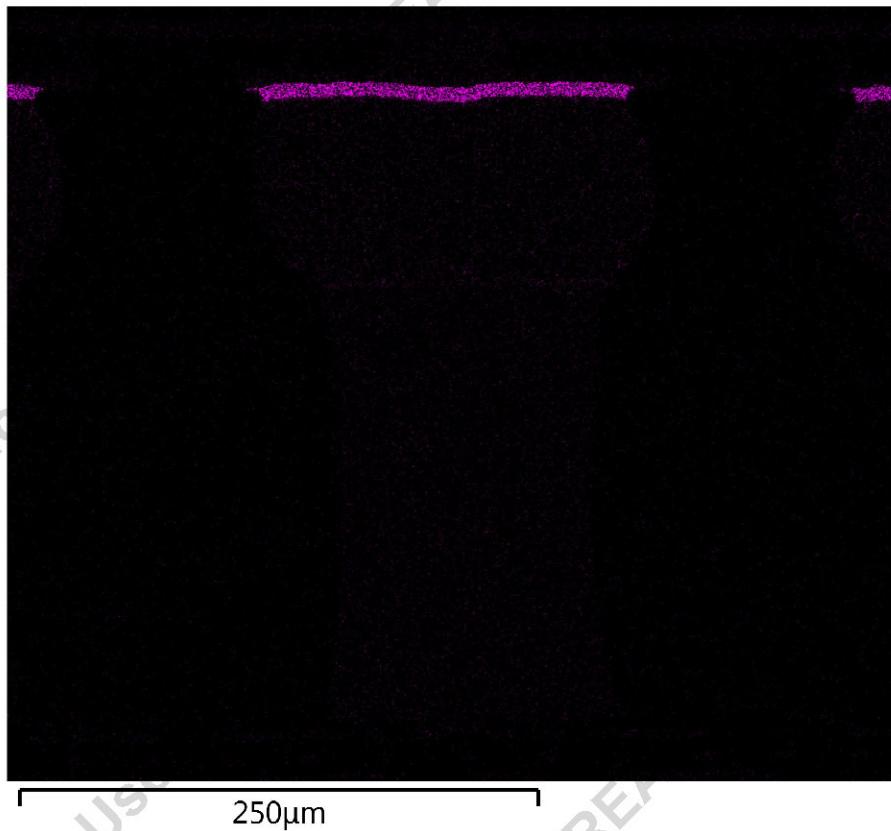


Figure 92. Nickel EDX map layer

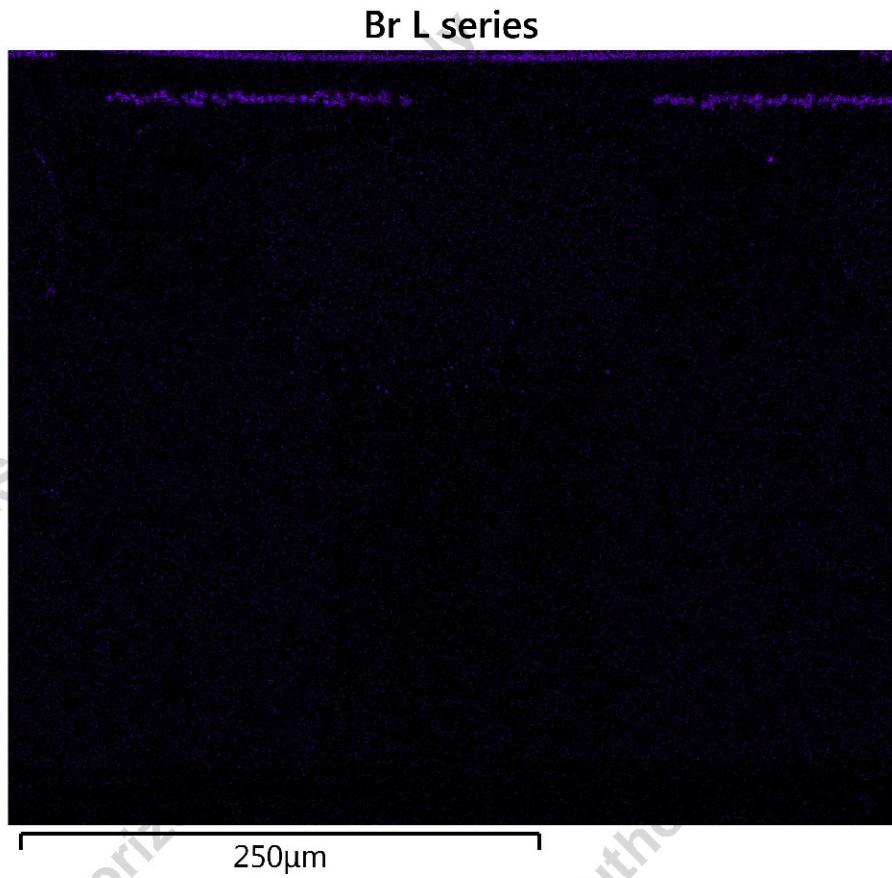


Figure 93. Bromine EDX map layer

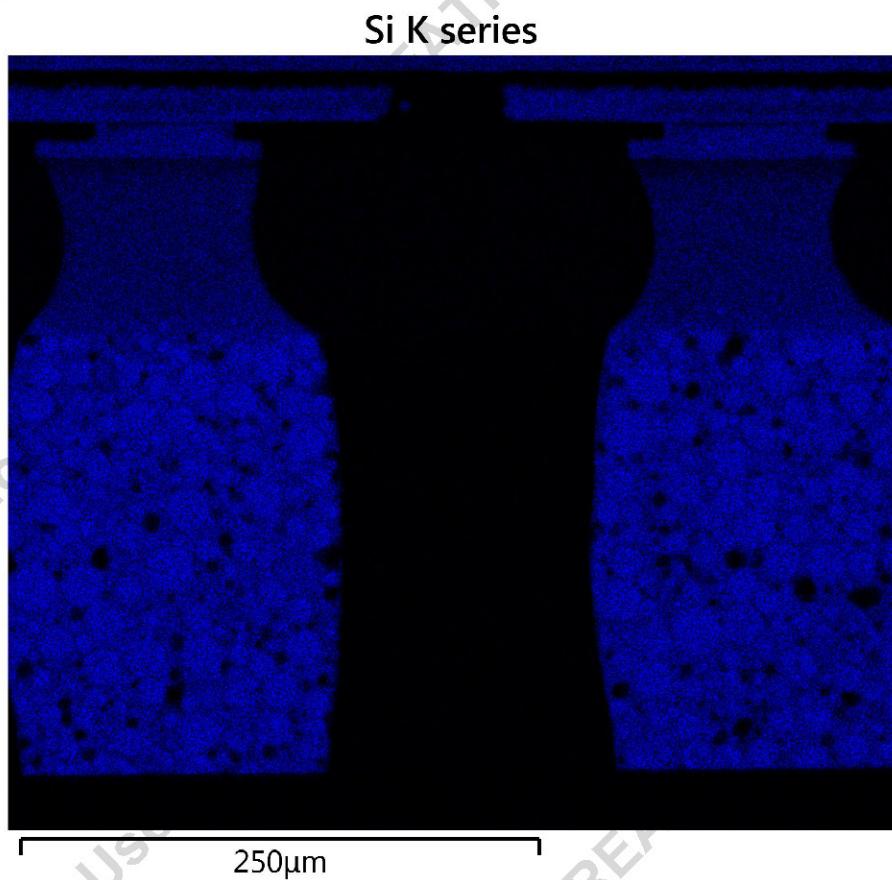


Figure 94. Silicon EDX map layer

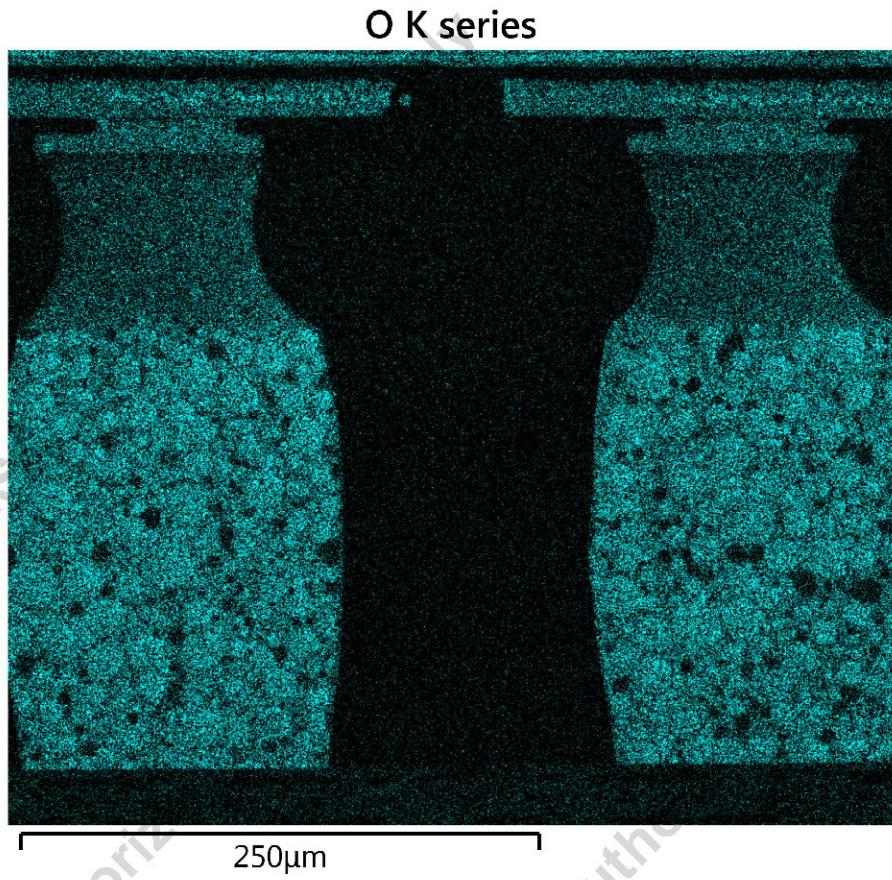


Figure 95. Oxygen EDX map layer

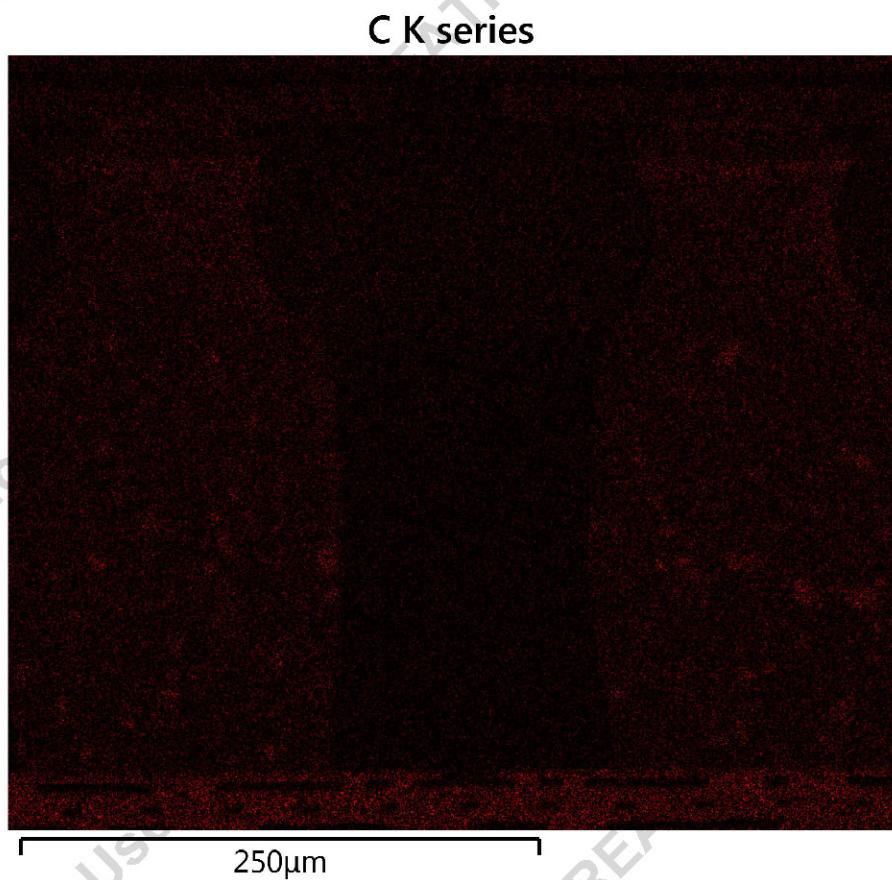


Figure 96. Carbon EDX map layer

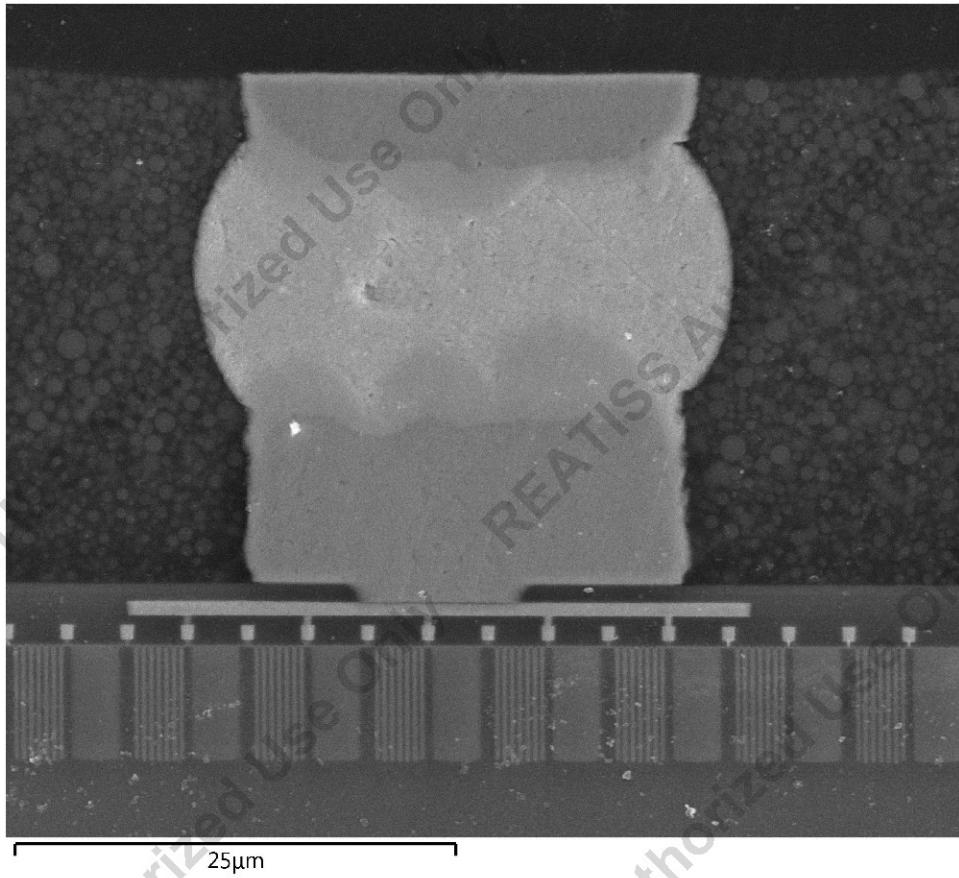


Figure 97. IPD 1 bond pad and copper pillar, connection to RDL

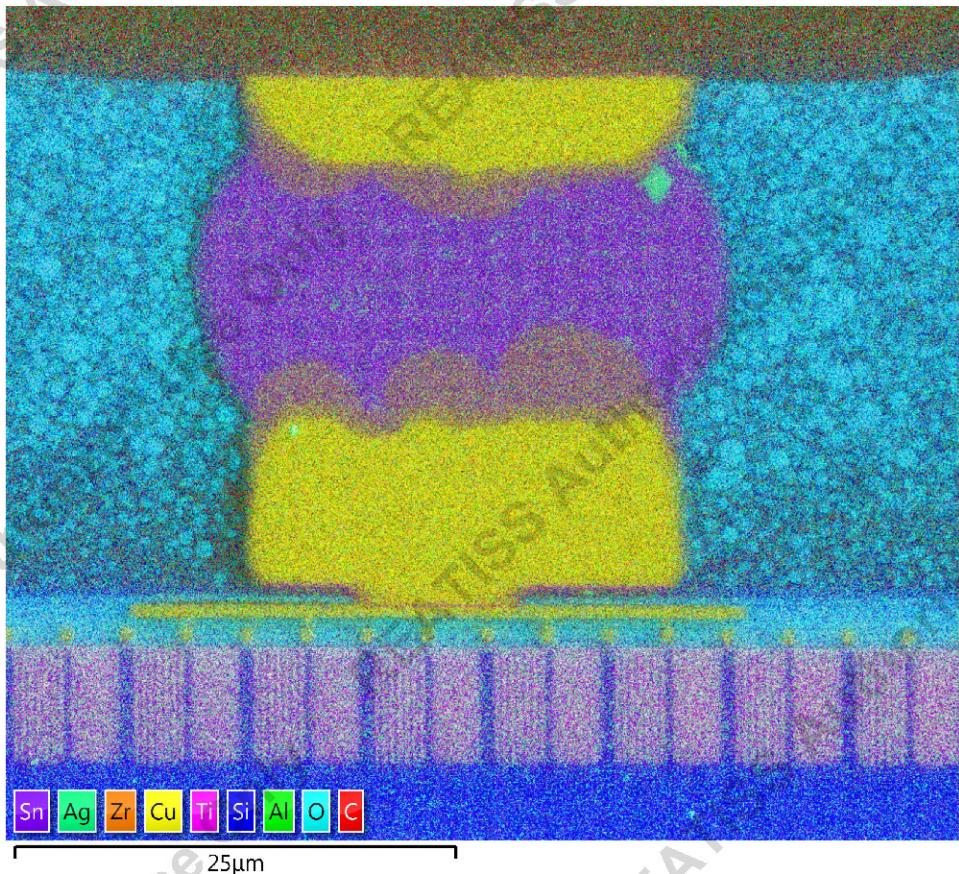


Figure 98. Layered EDX map of IPD 1 bond pad and copper pillar, connection to RDL

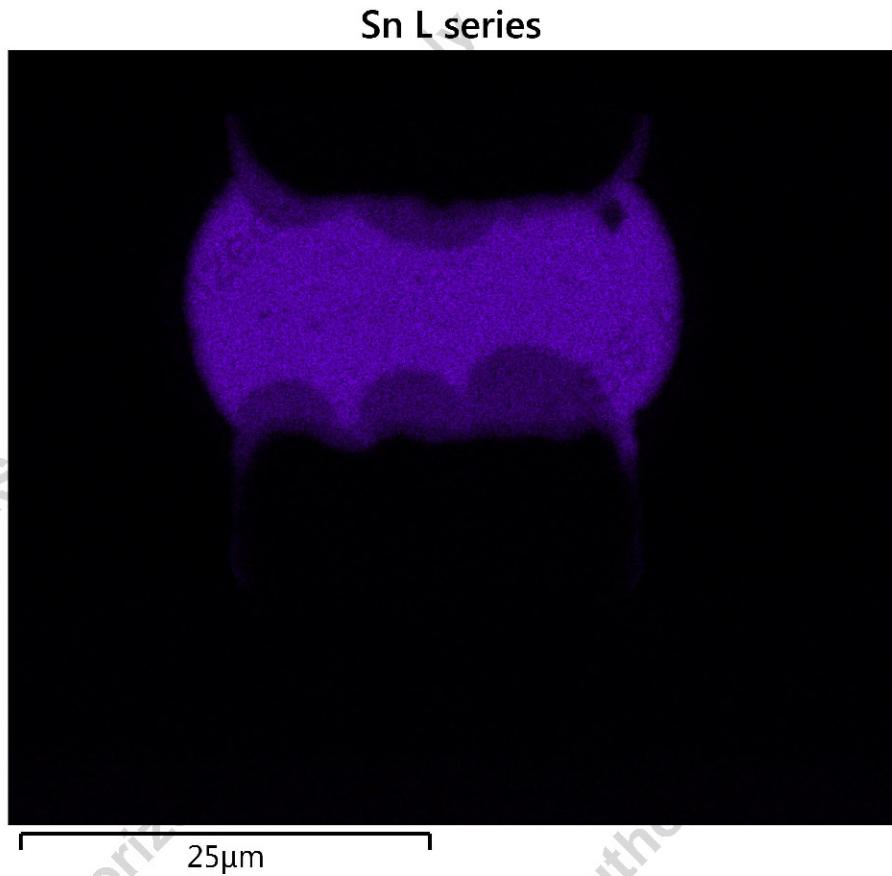


Figure 99. Tin EDX map layer

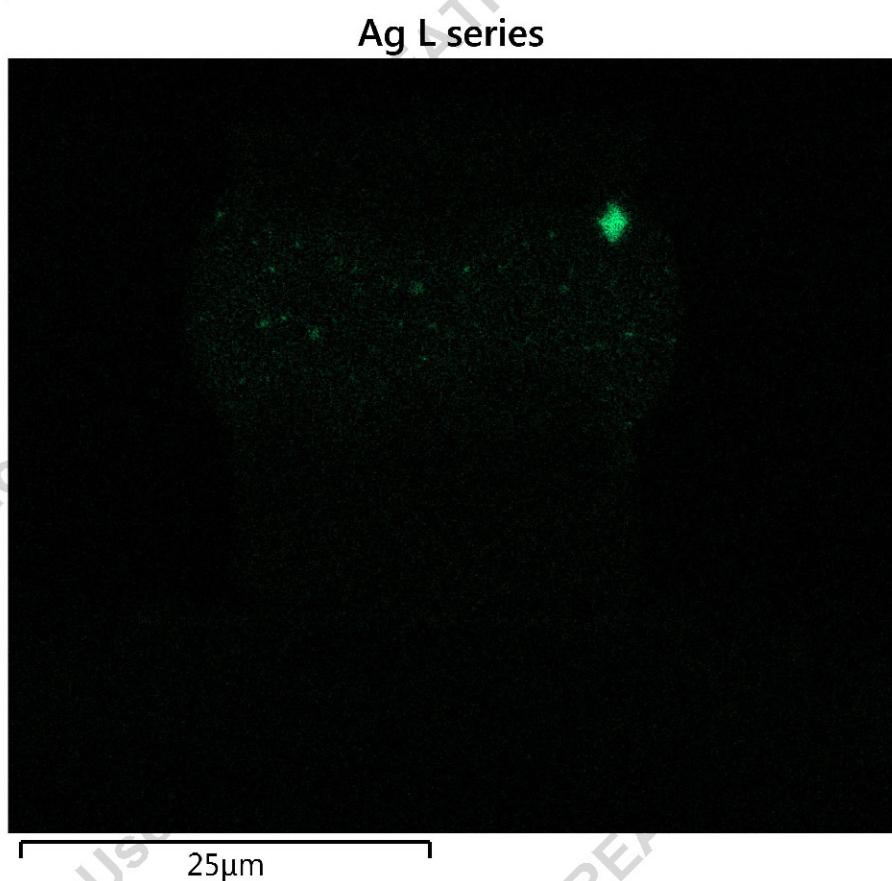


Figure 100. Silver EDX map layer

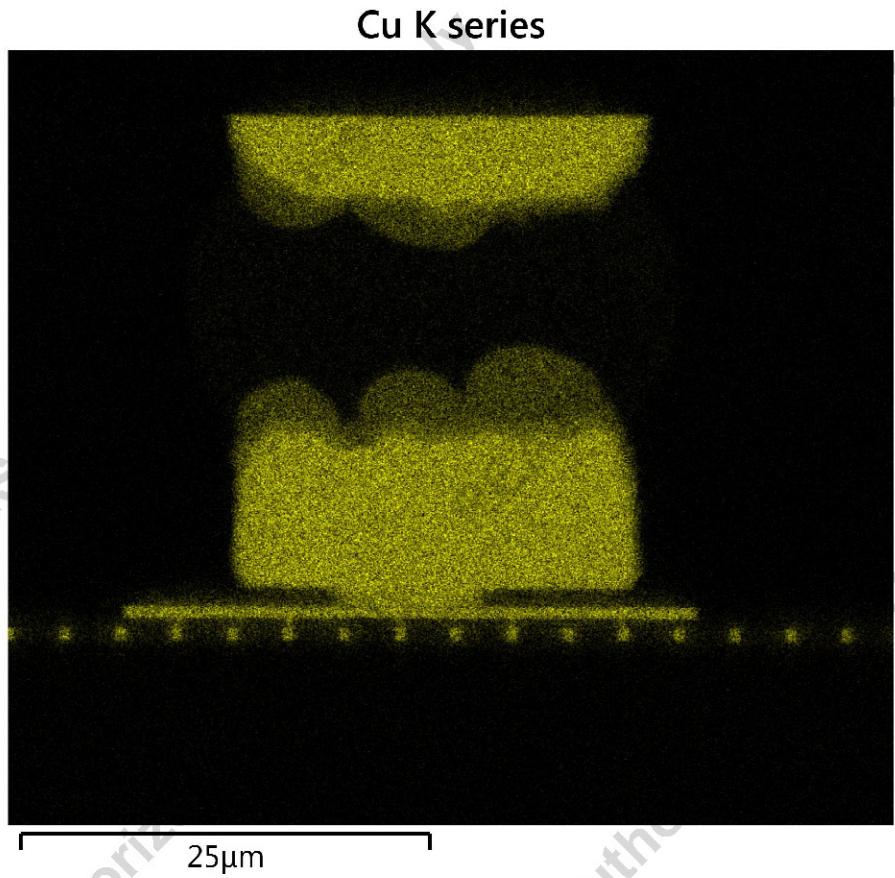


Figure 101. Copper EDX map layer

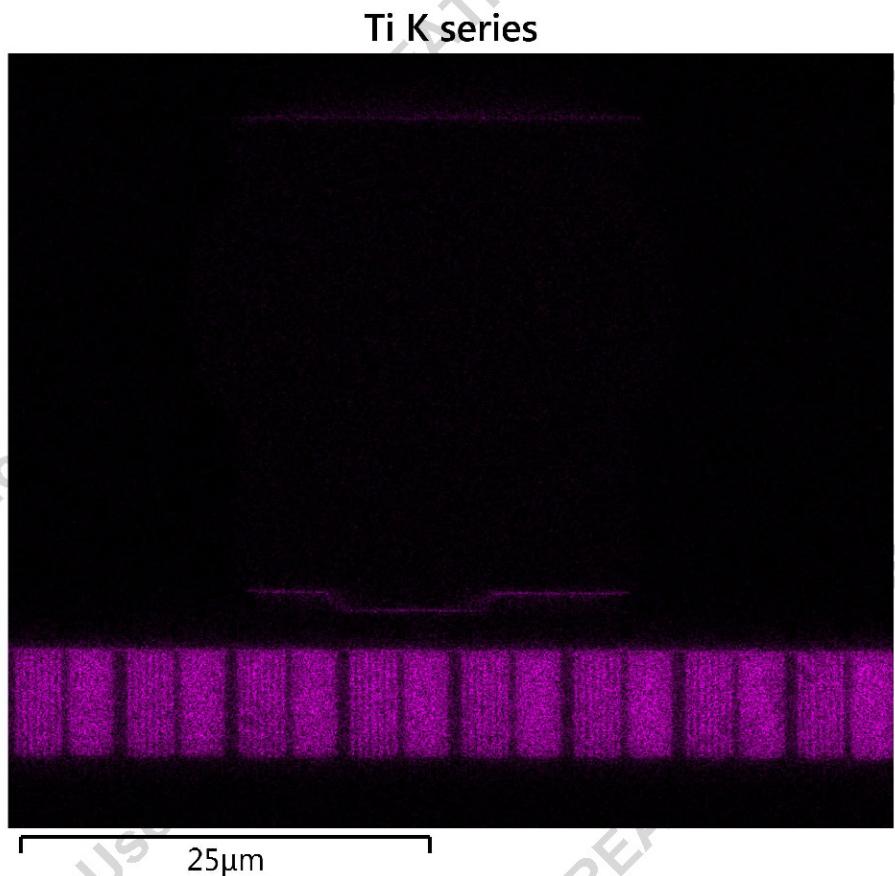


Figure 102. Titanium EDX map layer

Al K series

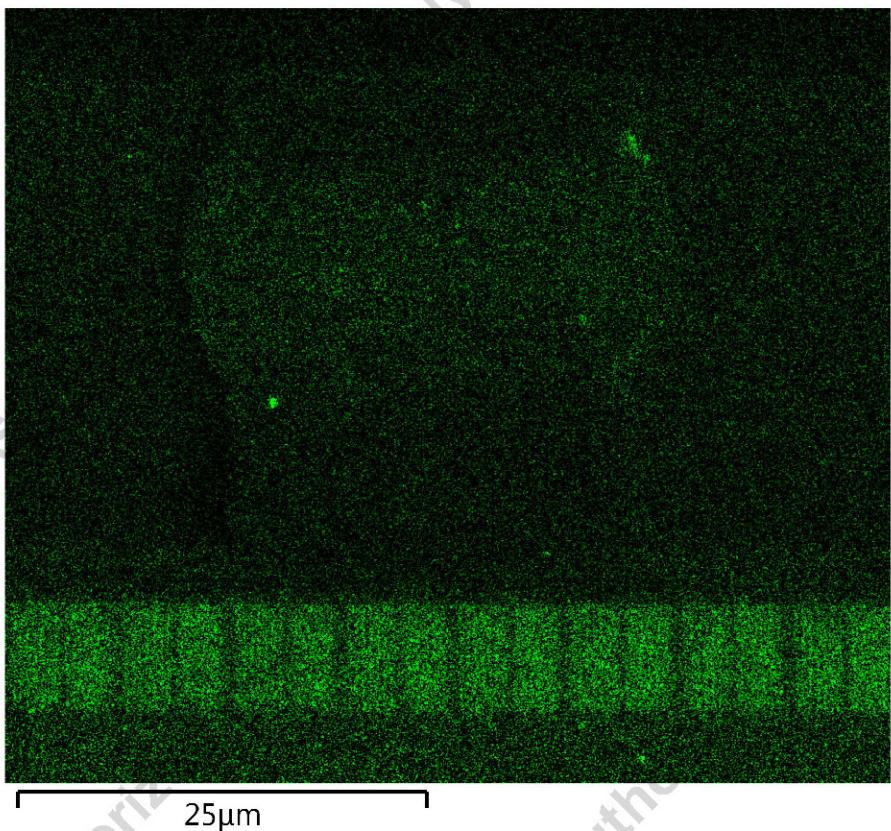


Figure 103. Aluminum EDX map layer

Zr L series

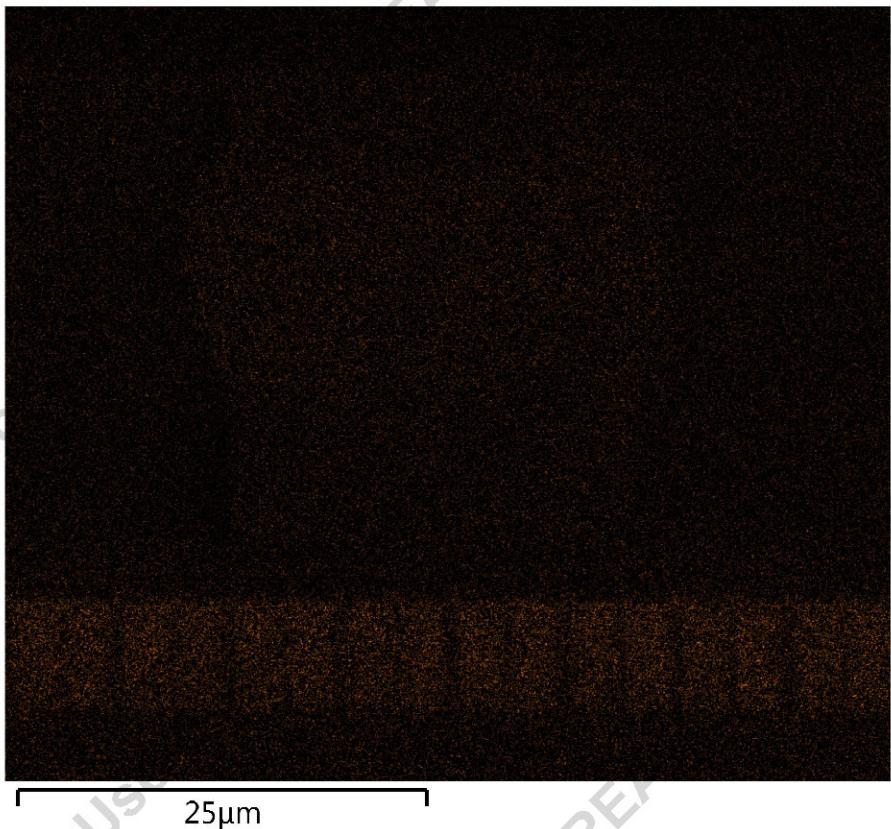


Figure 104. Zirconium EDX map layer

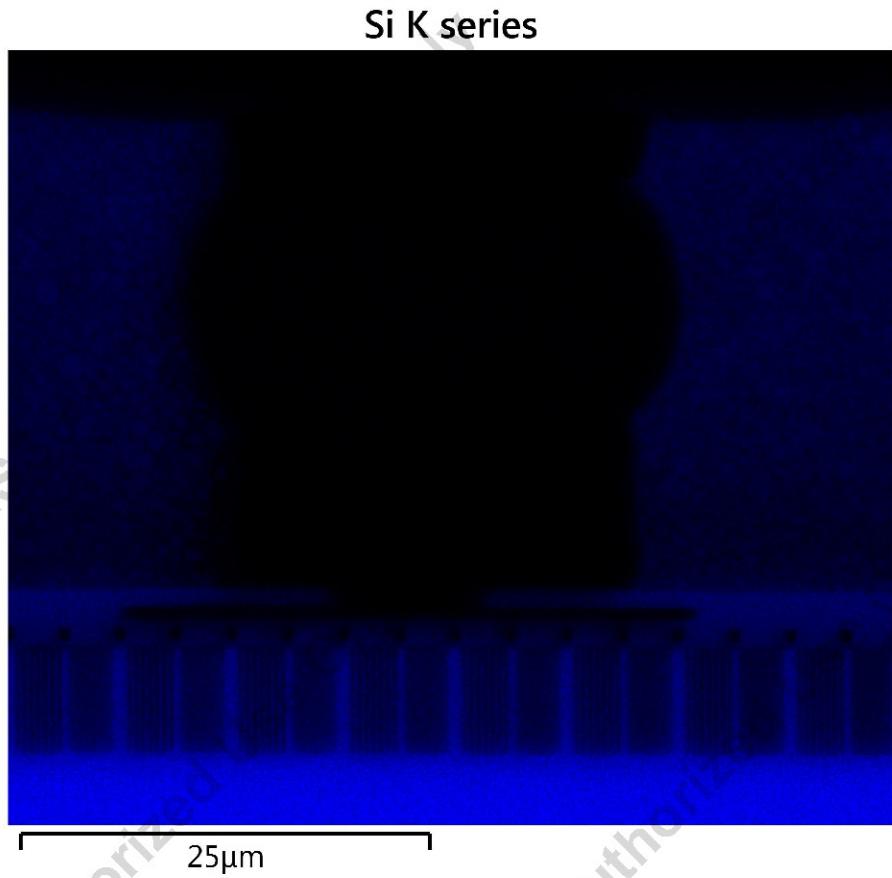


Figure 105. Silicon EDX map layer

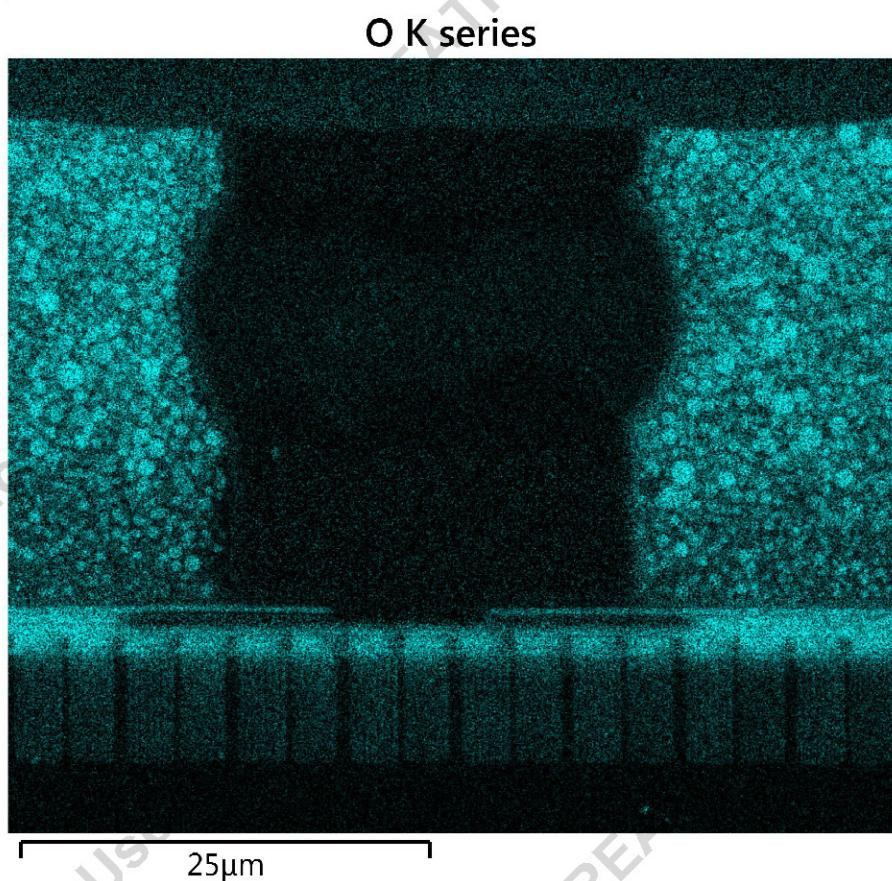


Figure 106. Oxygen EDX map layer

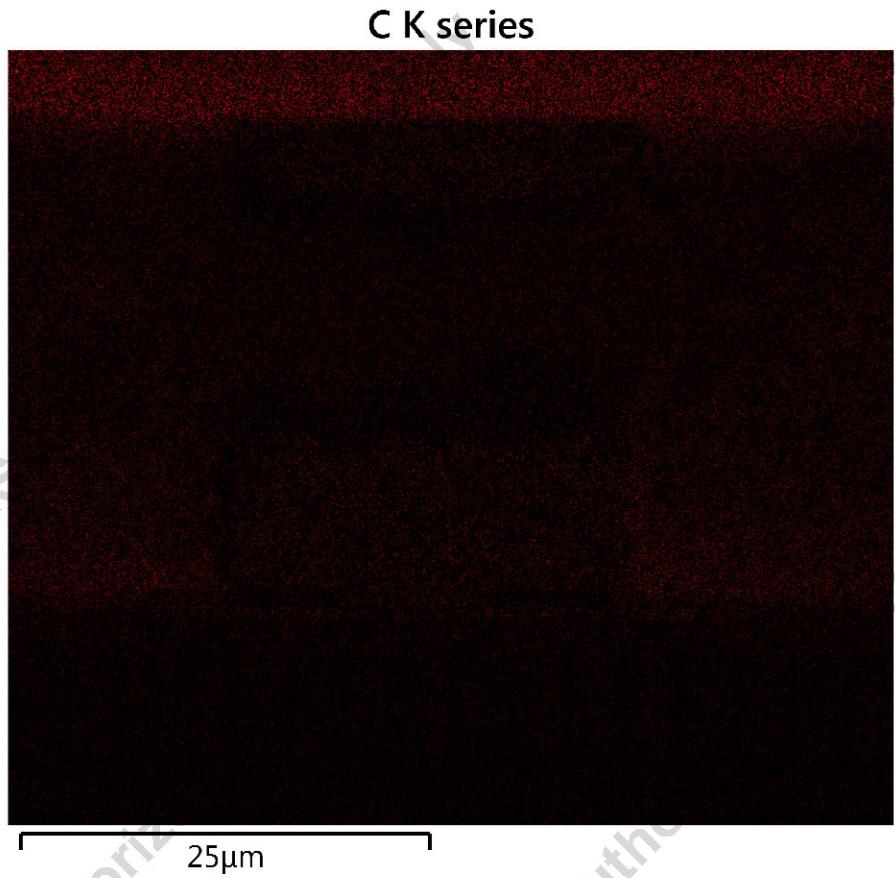


Figure 107. Carbon EDX map layer

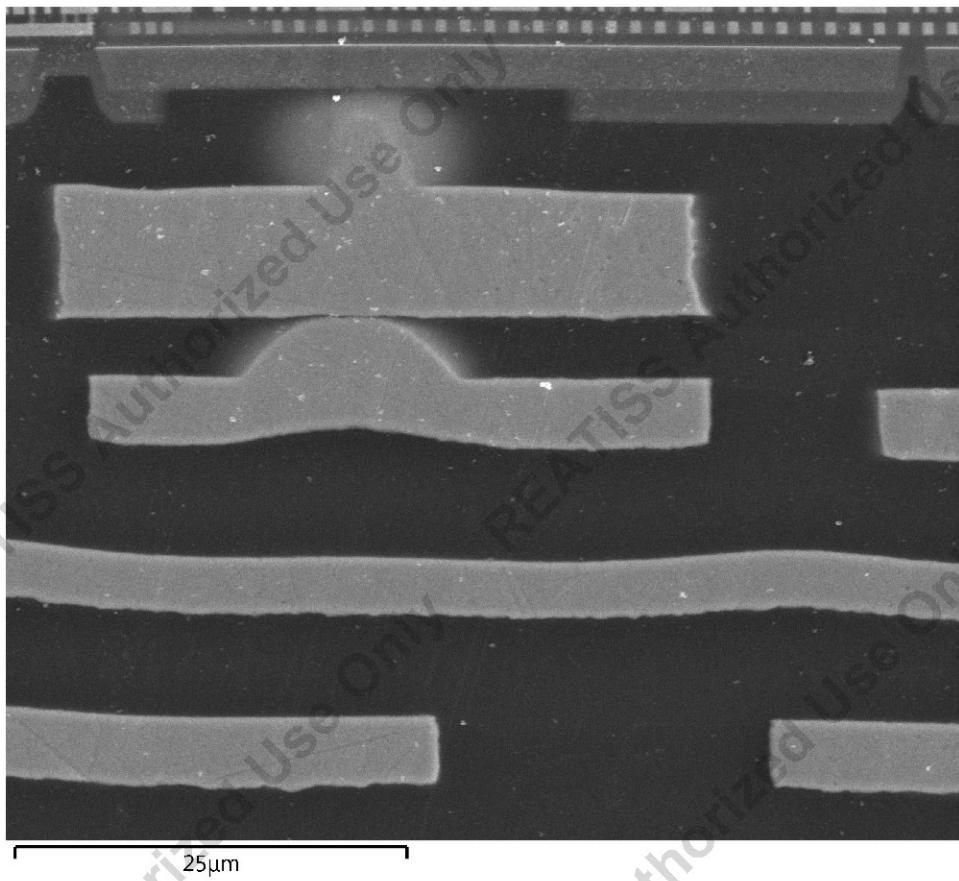


Figure 108. Processor die bond pad, RDL1-RDL4

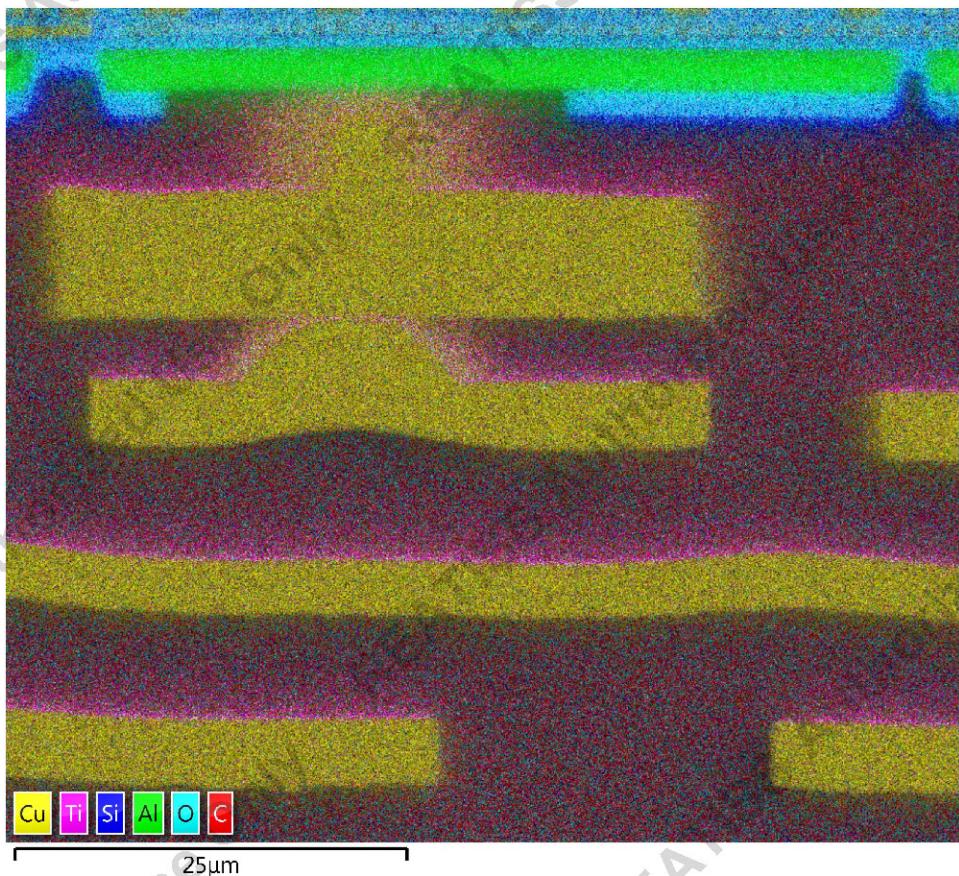


Figure 109. Layered EDX map of processor die bond pad, RDL1-RDL4

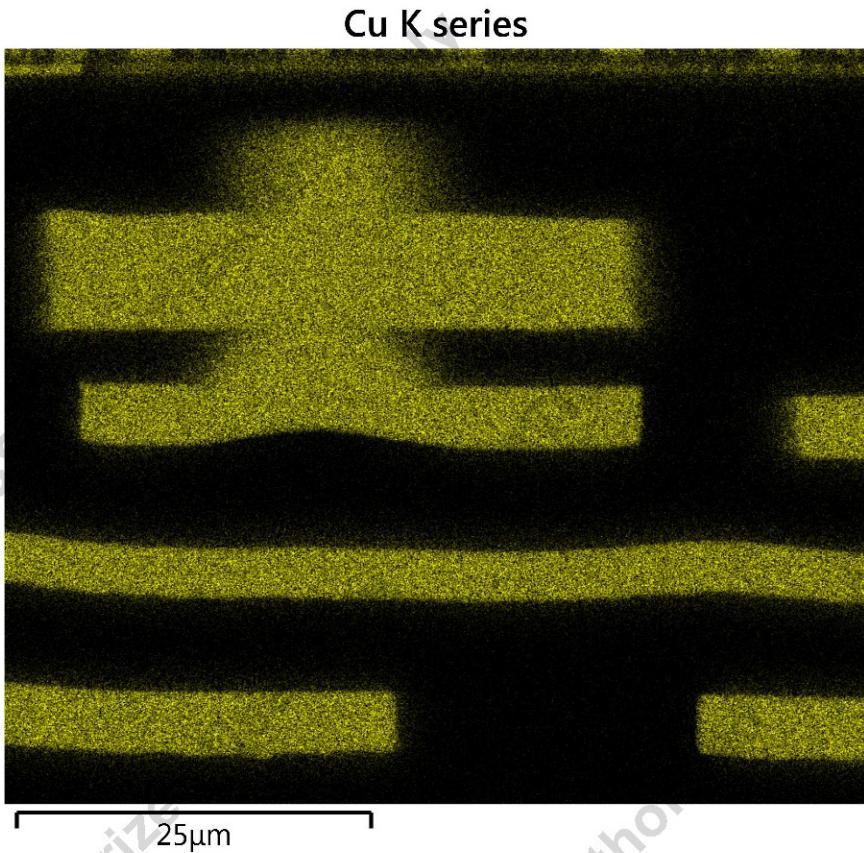


Figure 110. Copper EDX map layer

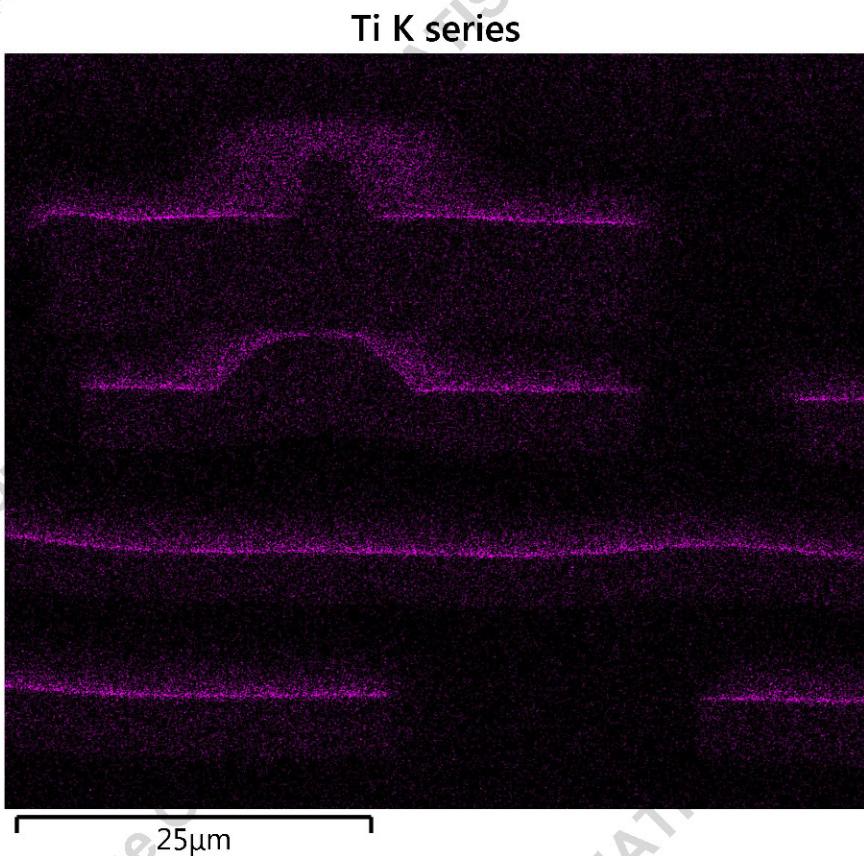


Figure 111. Titanium EDX map layer

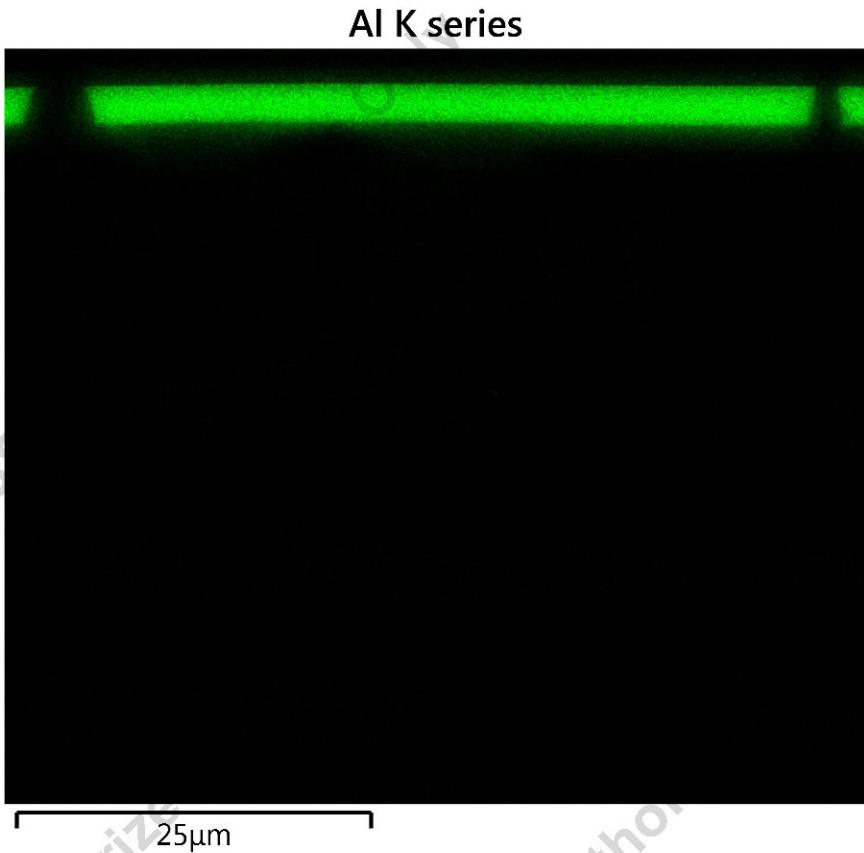


Figure 112. Aluminum EDX map layer

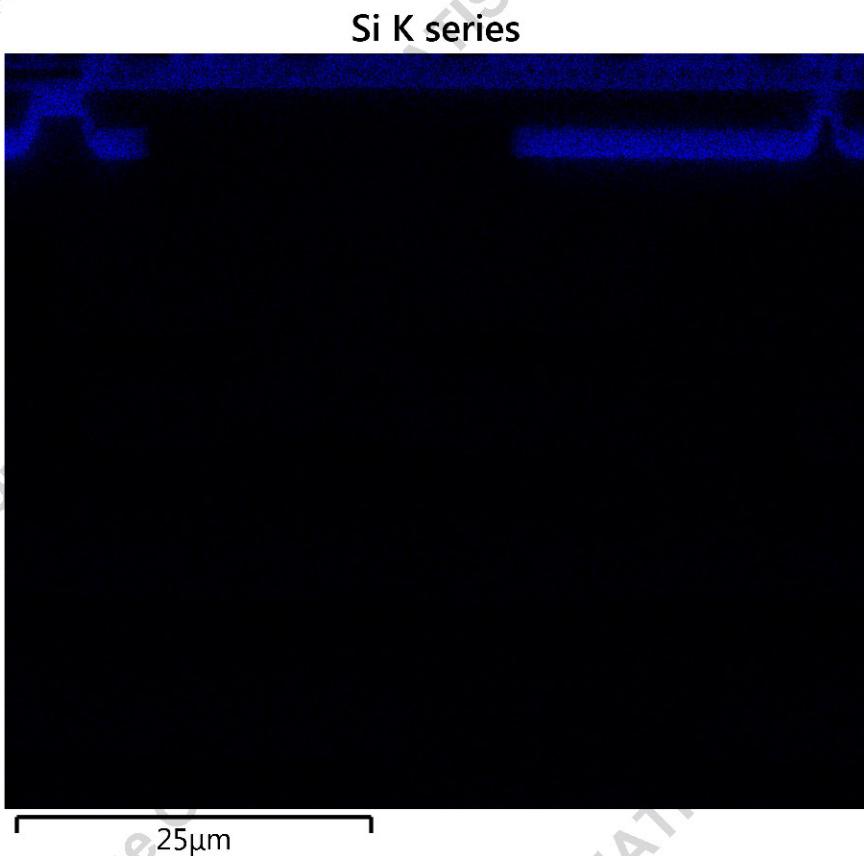


Figure 113. Silicon EDX map layer

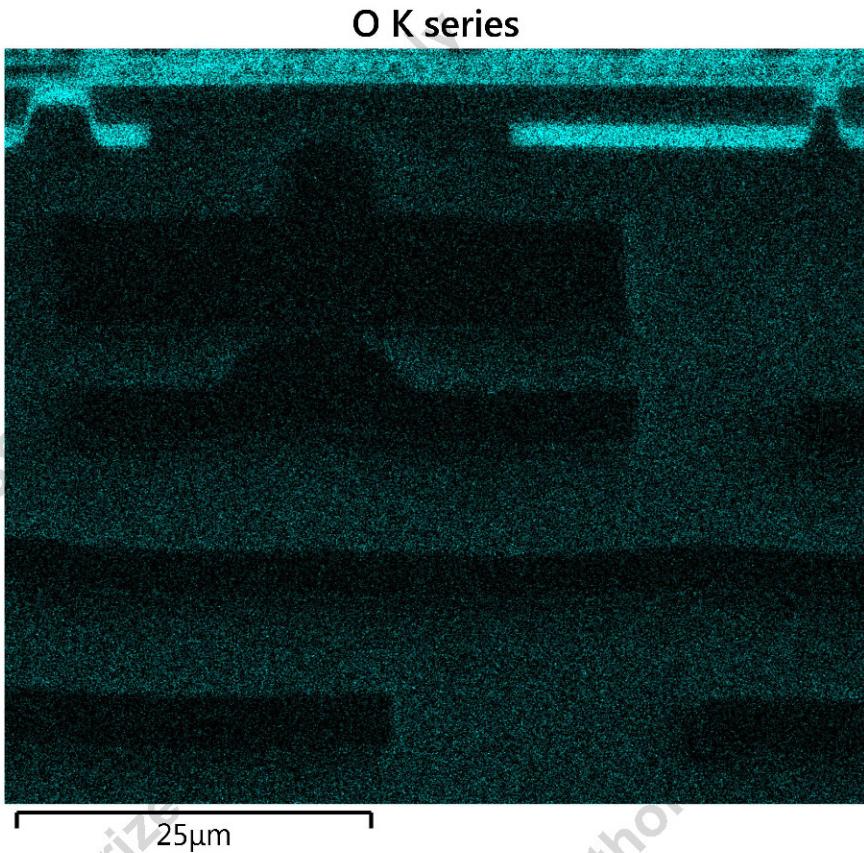


Figure 114. Oxygen EDX map layer

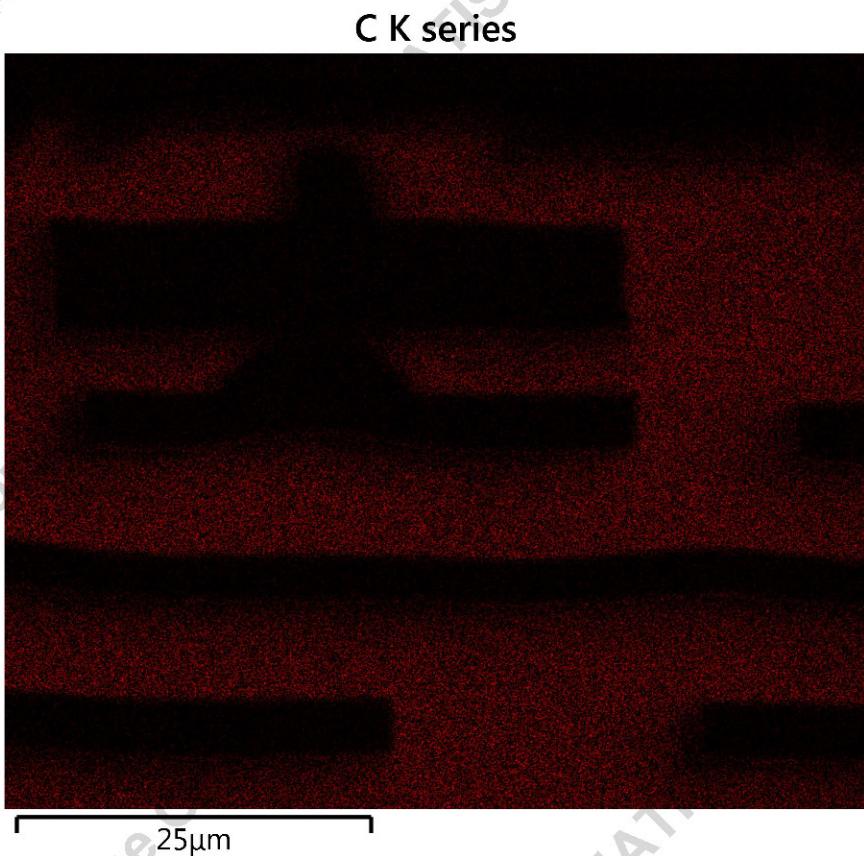


Figure 115. Carbon EDX map layer

Process Analysis

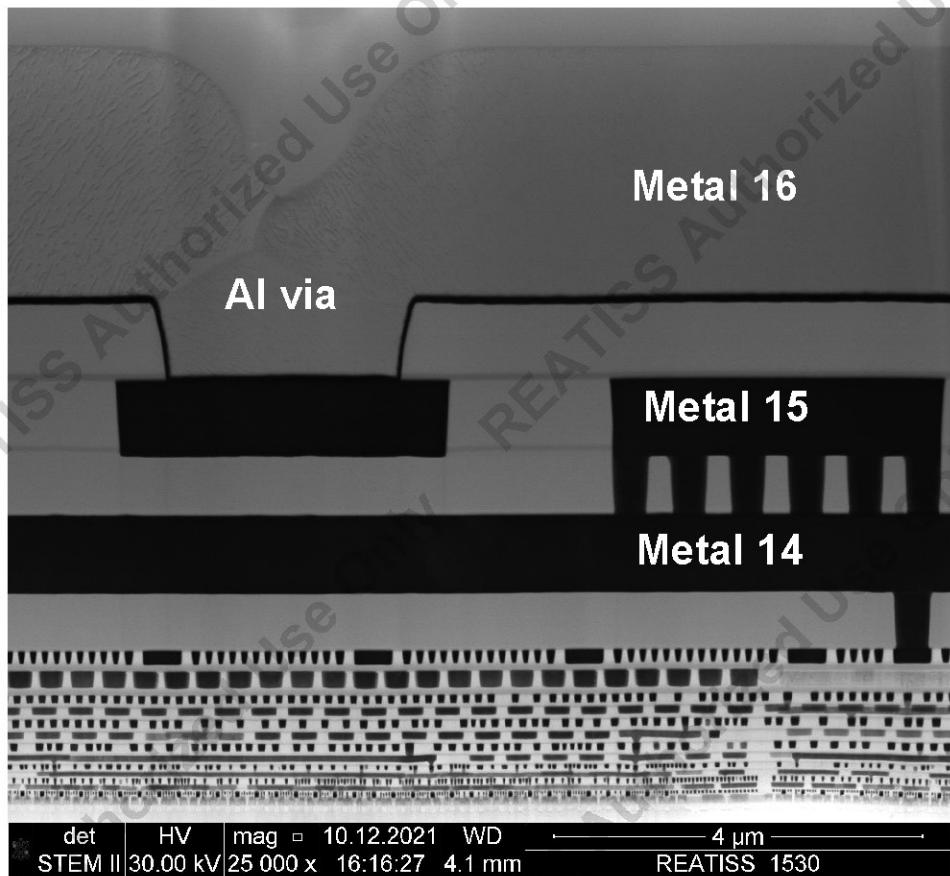


Figure 116. General view

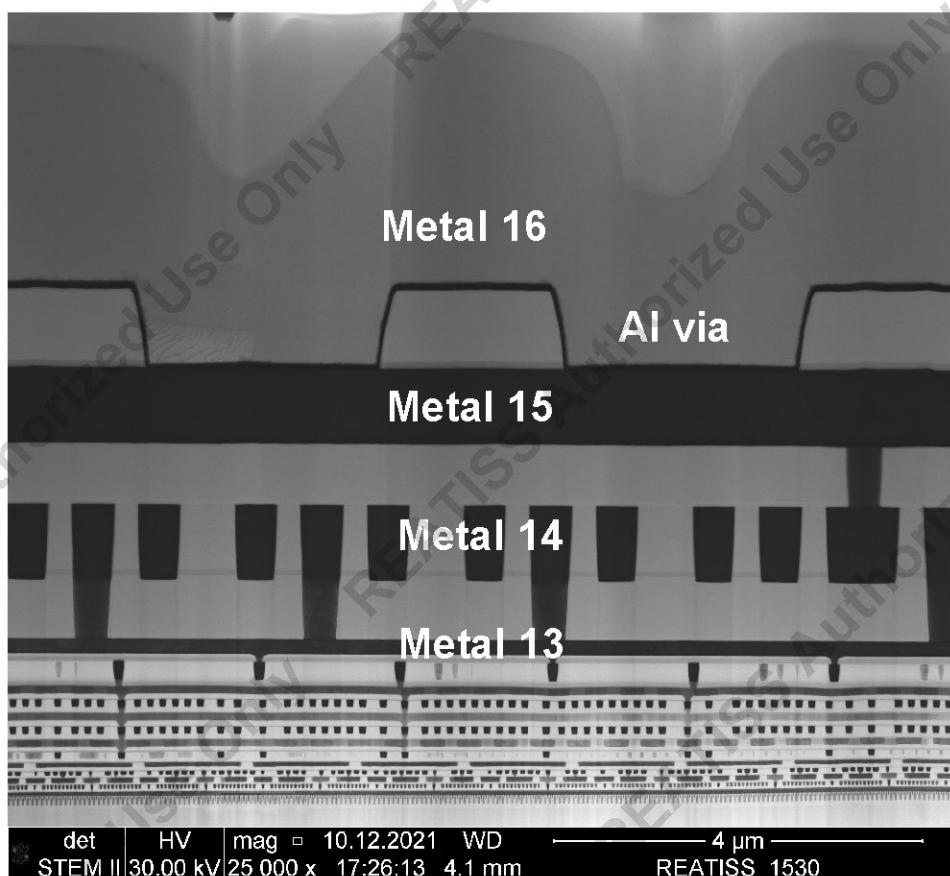


Figure 117. General view

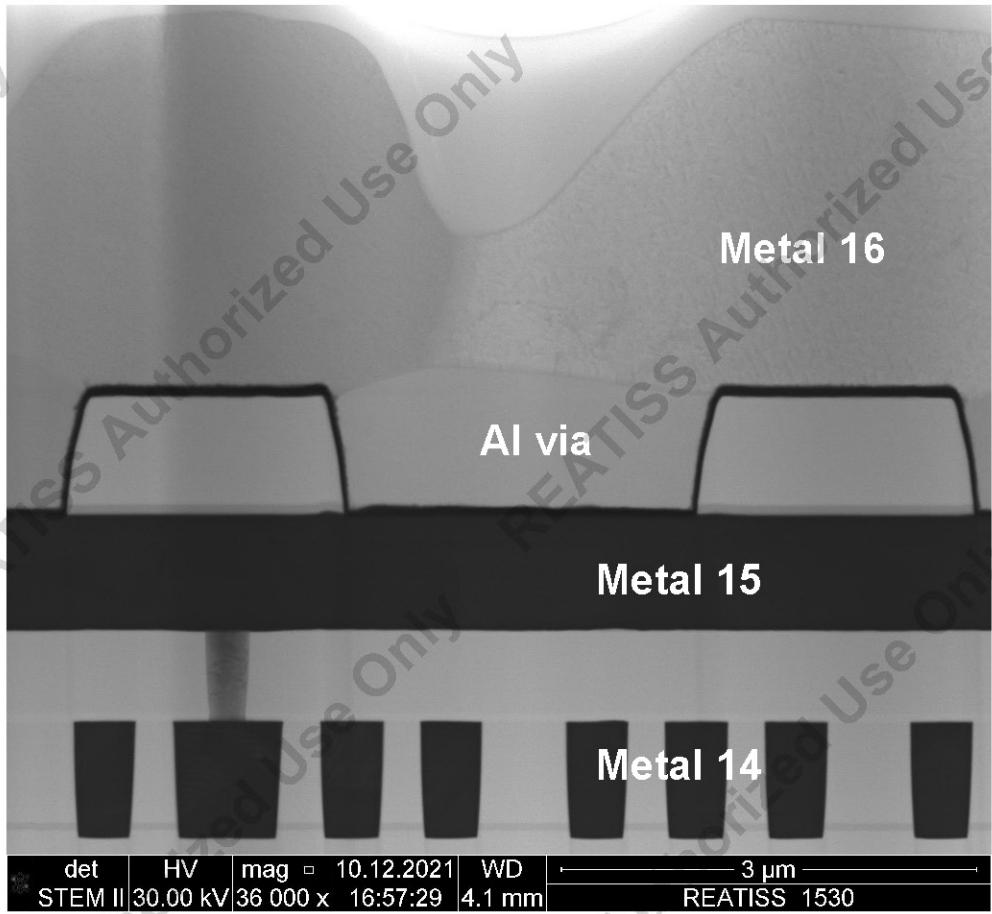


Figure 118. Al M16, Cu M14, M15 lines, Al and Cu vias

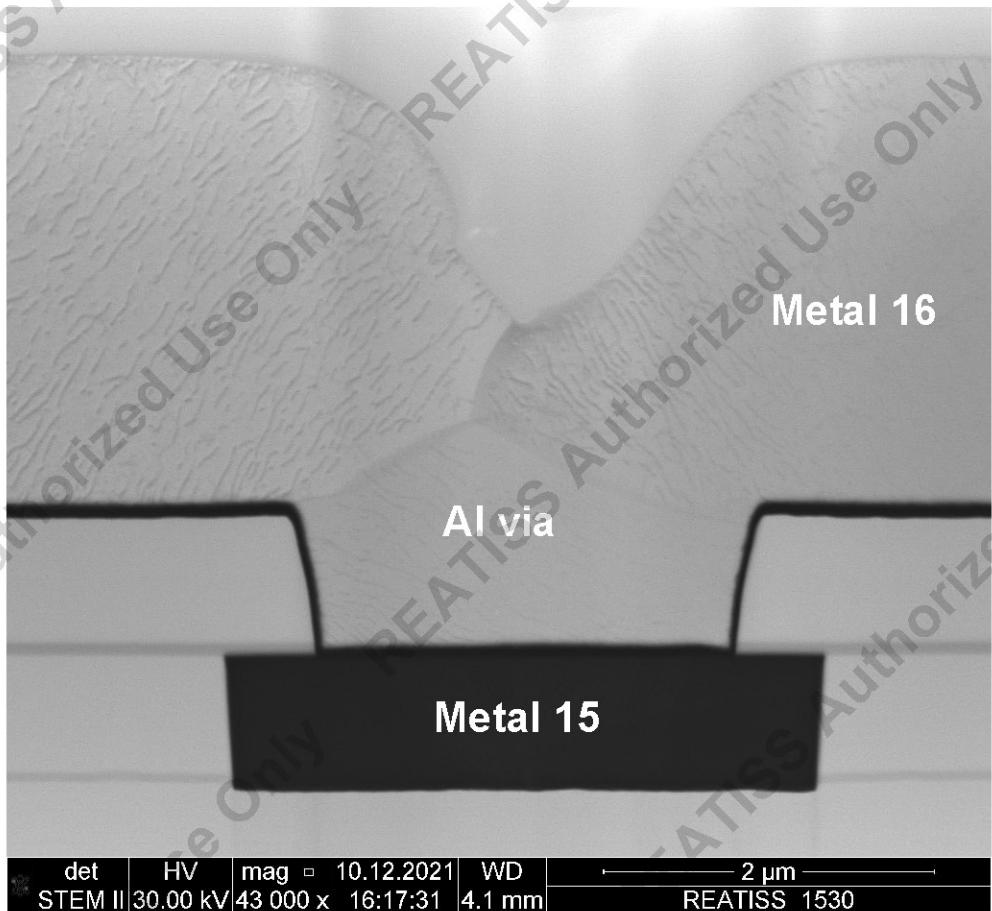


Figure 119. Al M16, Cu M15 lines, Al via

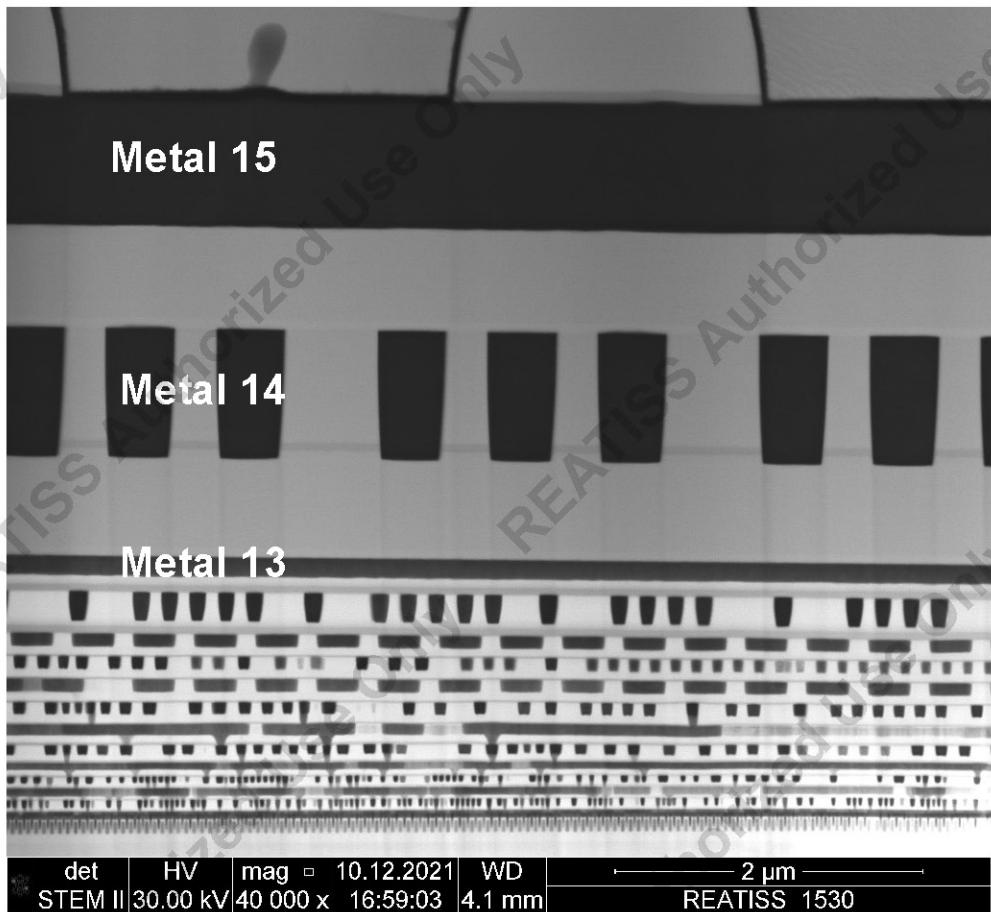


Figure 120. Co Li1, W Li2, Cu M1-M15 lines, Cu vias

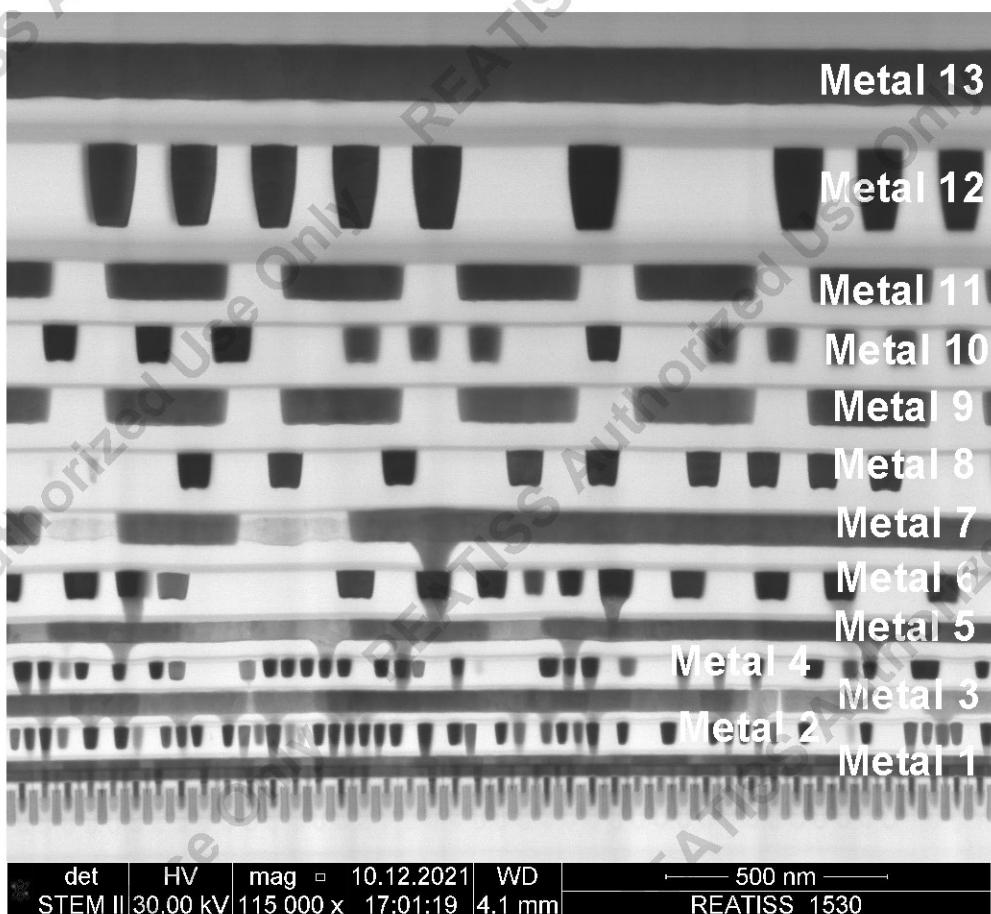


Figure 121. Co Li1, W Li2, Cu M1-M13 lines, Cu vias

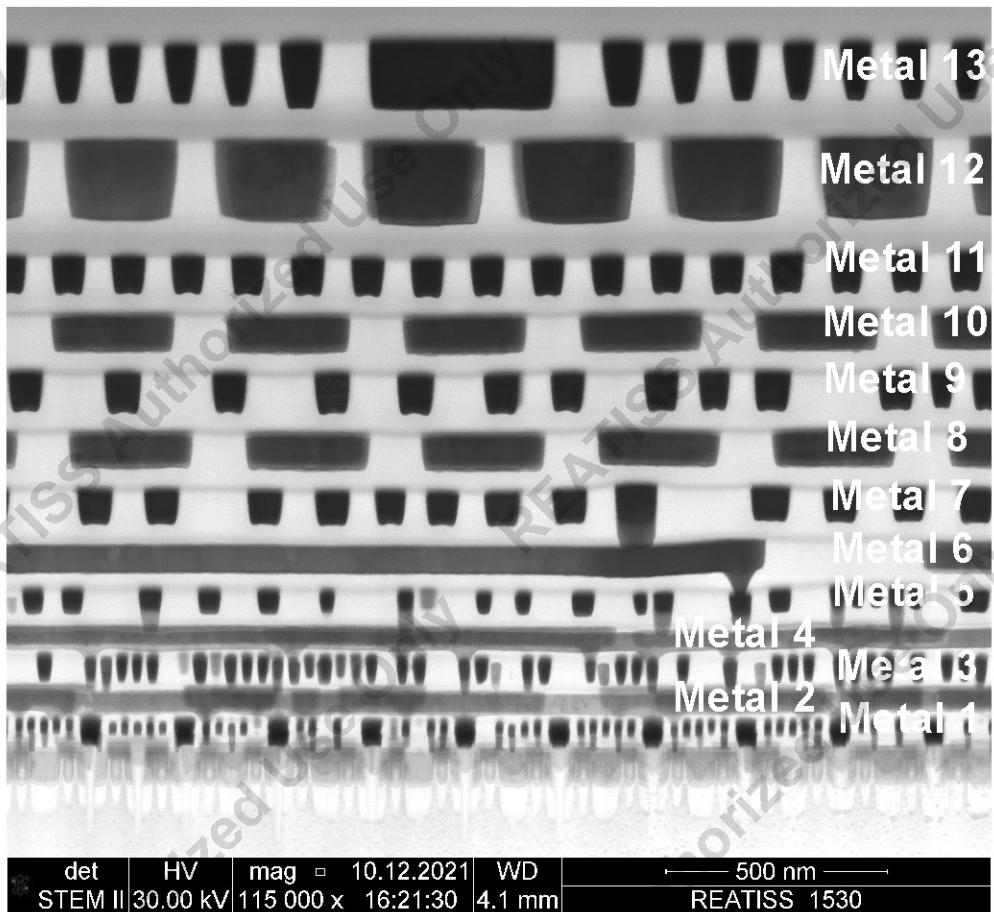


Figure 122. Co Li1, W Li2, Cu M1-M13 lines, Cu vias

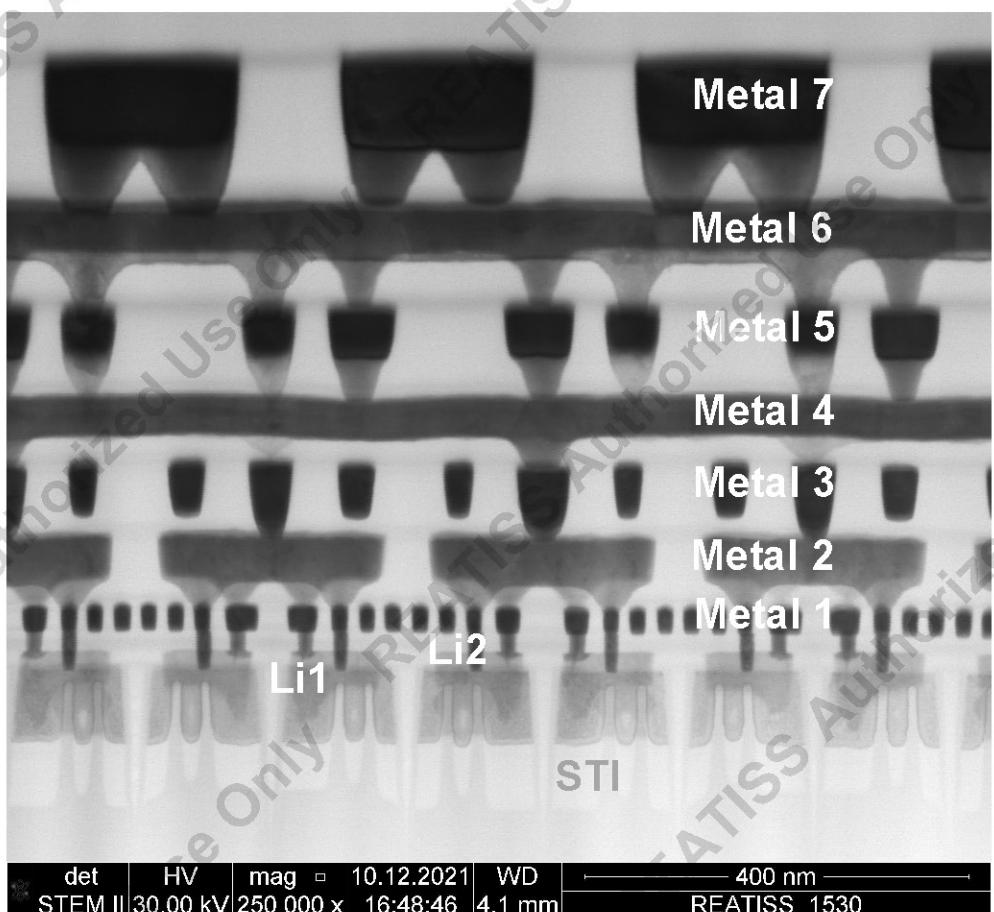


Figure 123. Co Li1, W Li2, Cu M1-M7 lines, Cu vias

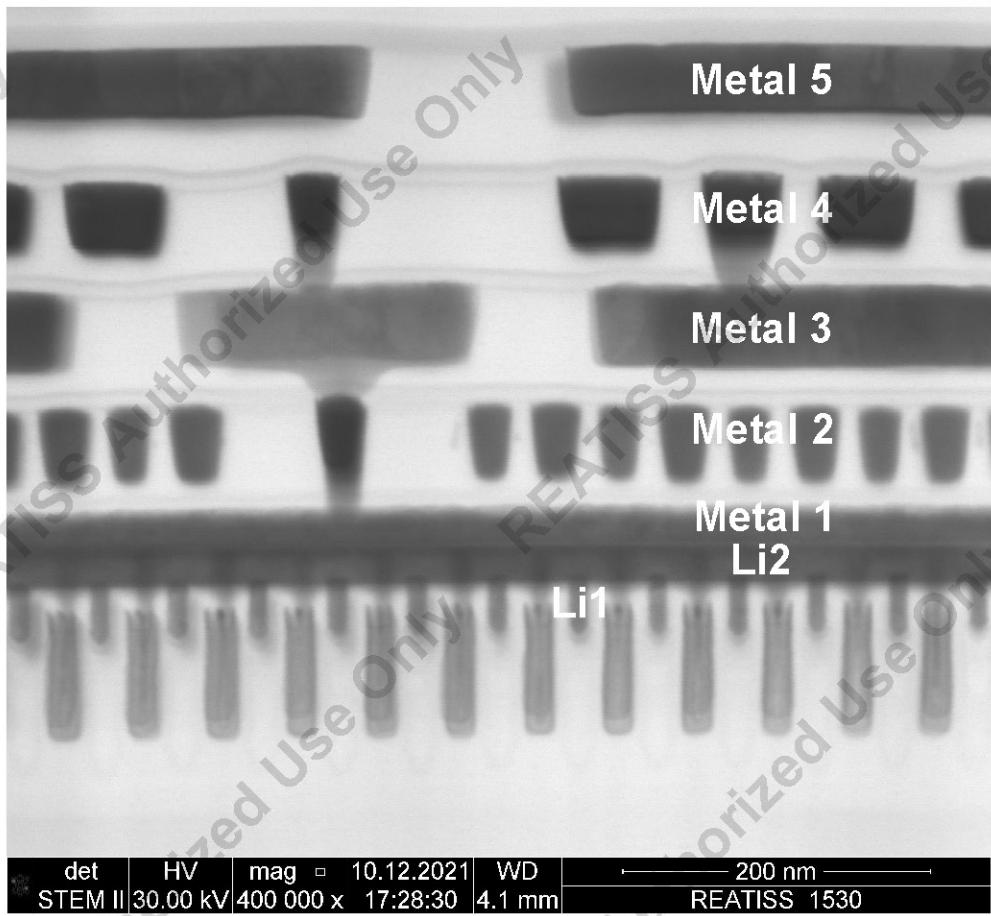


Figure 124. Co Li1, W Li2, Cu M1-M5 lines, Cu vias, FinFETs along fins

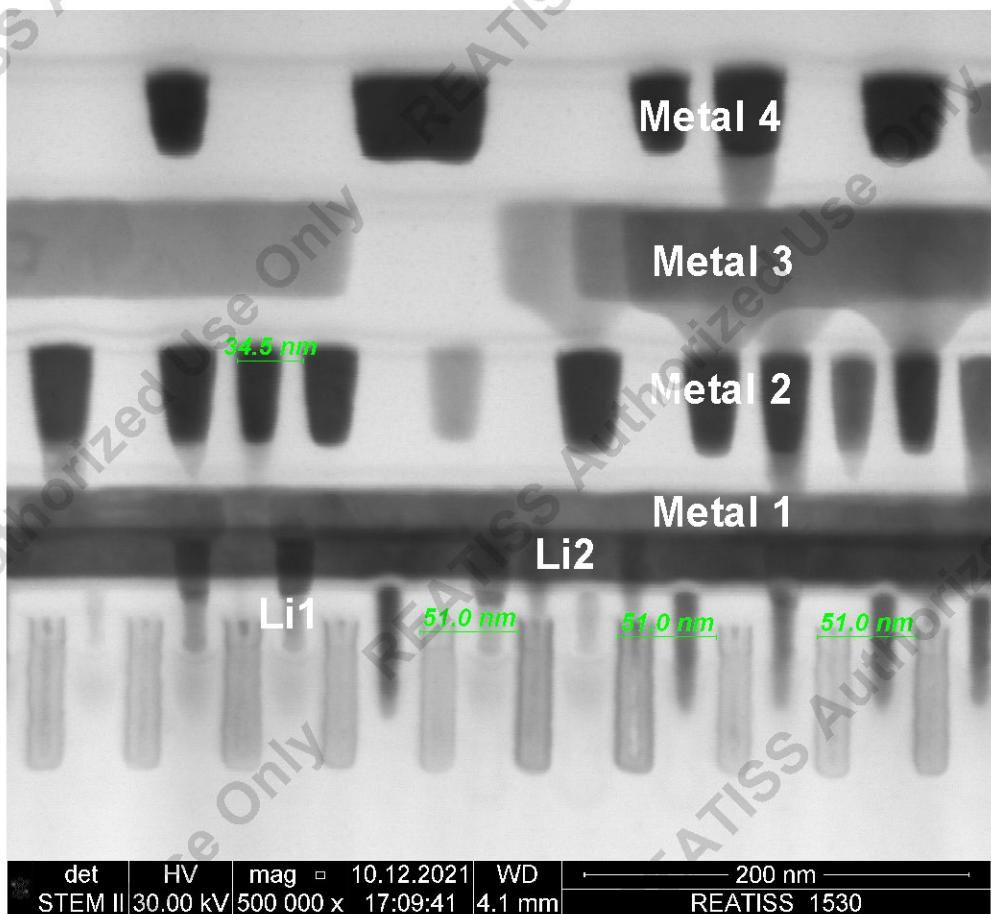


Figure 125. Co Li1, W Li2, Cu M1-M4 lines, Cu vias, FinFETs along fins

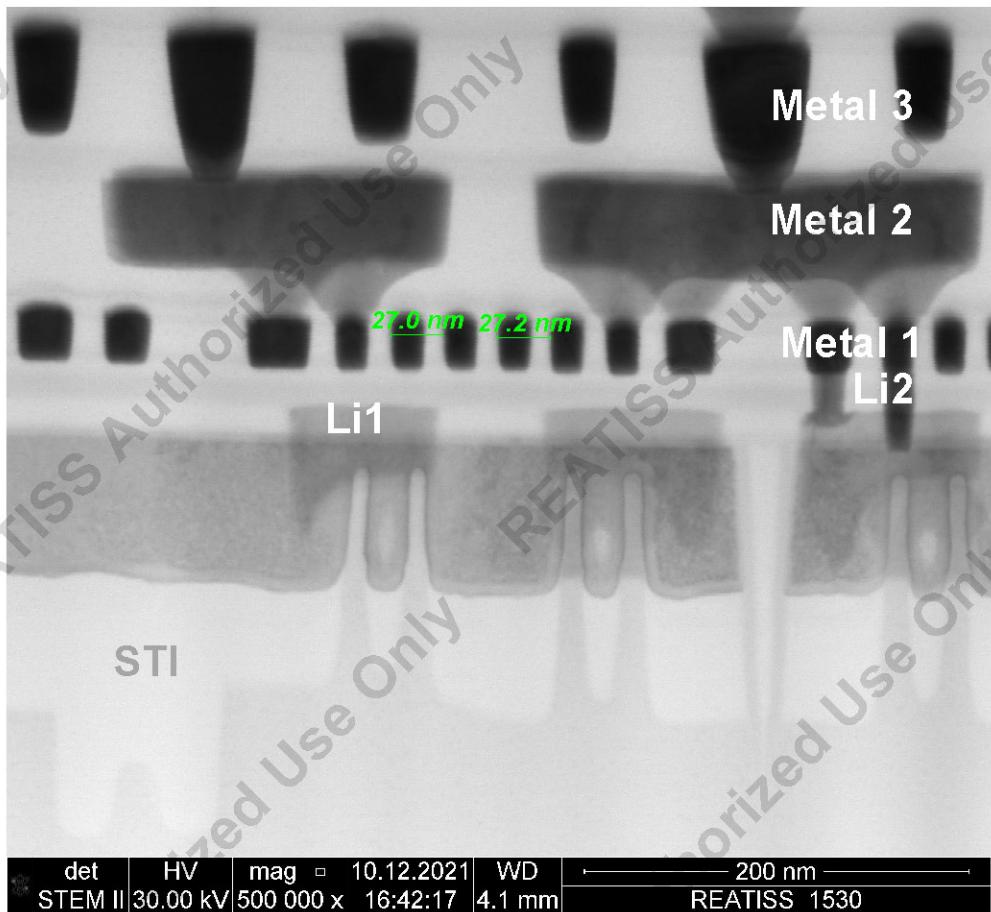


Figure 126. Co Li1, W Li2, Cu M1-M3 lines, Cu vias, FinFETs across fins, STI

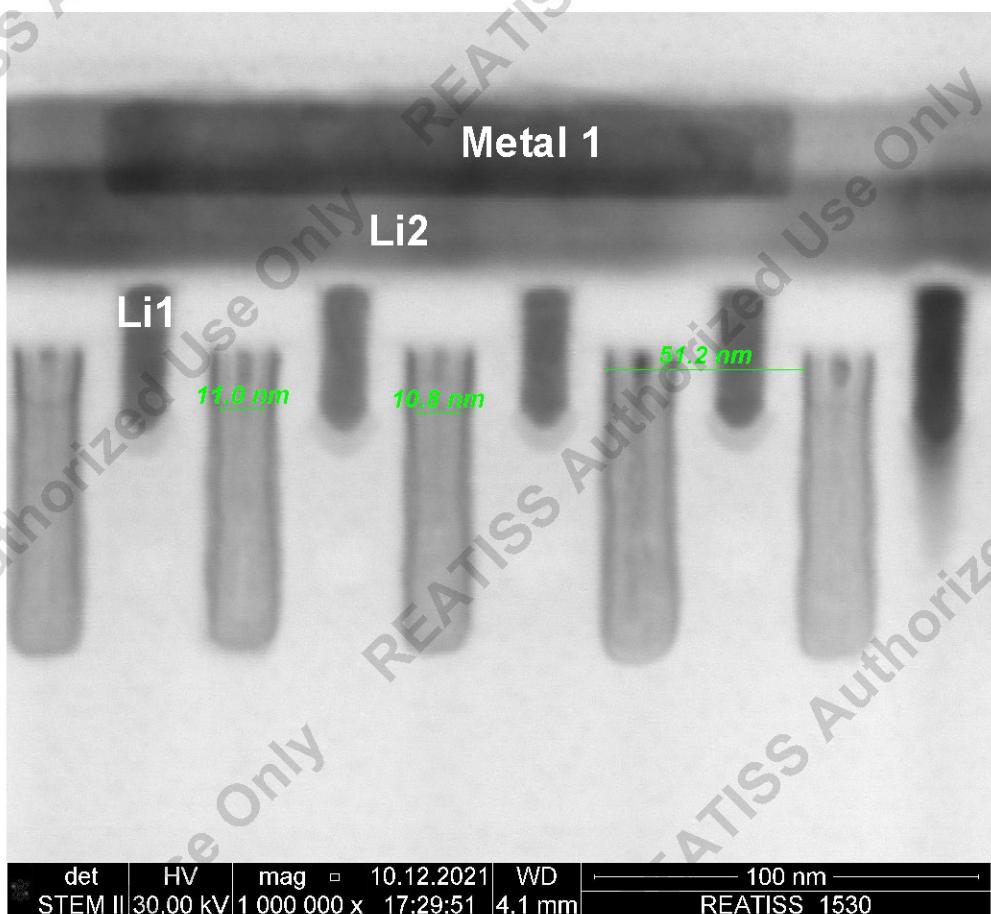


Figure 127. Co Li1, W Li2, Cu M1 line, FinFETs along fins

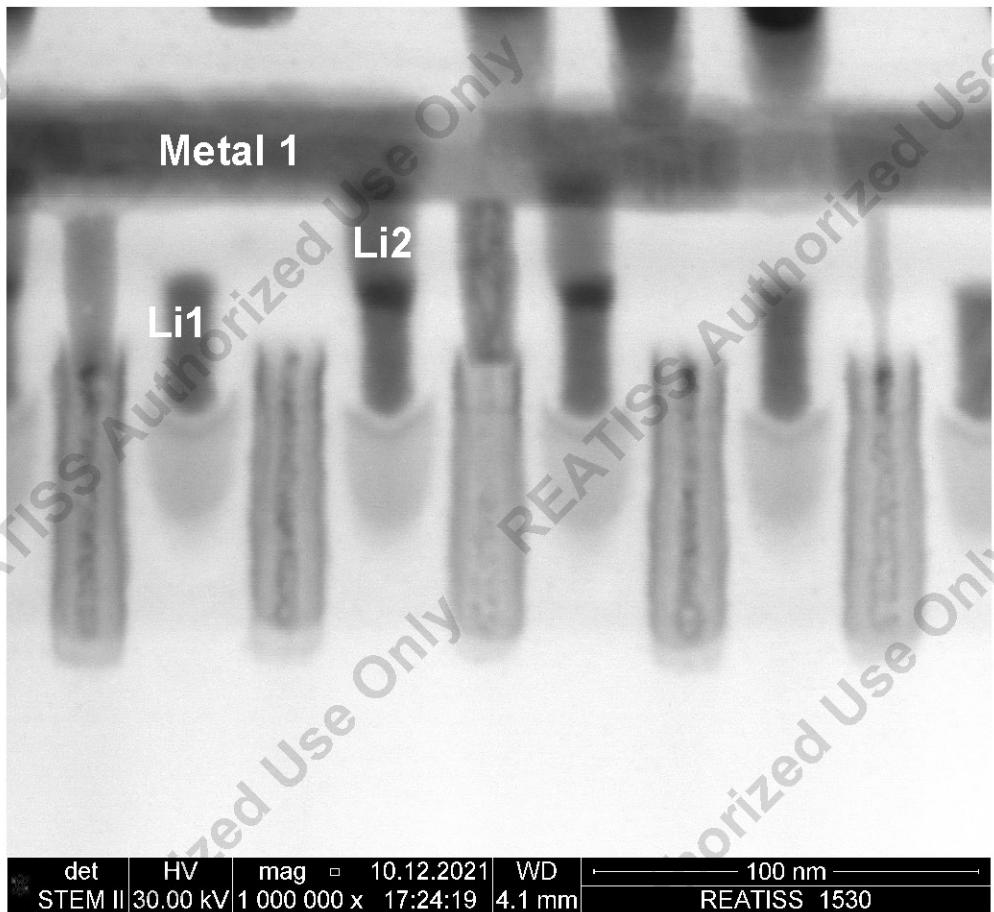


Figure 128. Co Li1, W Li2, Cu M1 line, FinFETs along fins

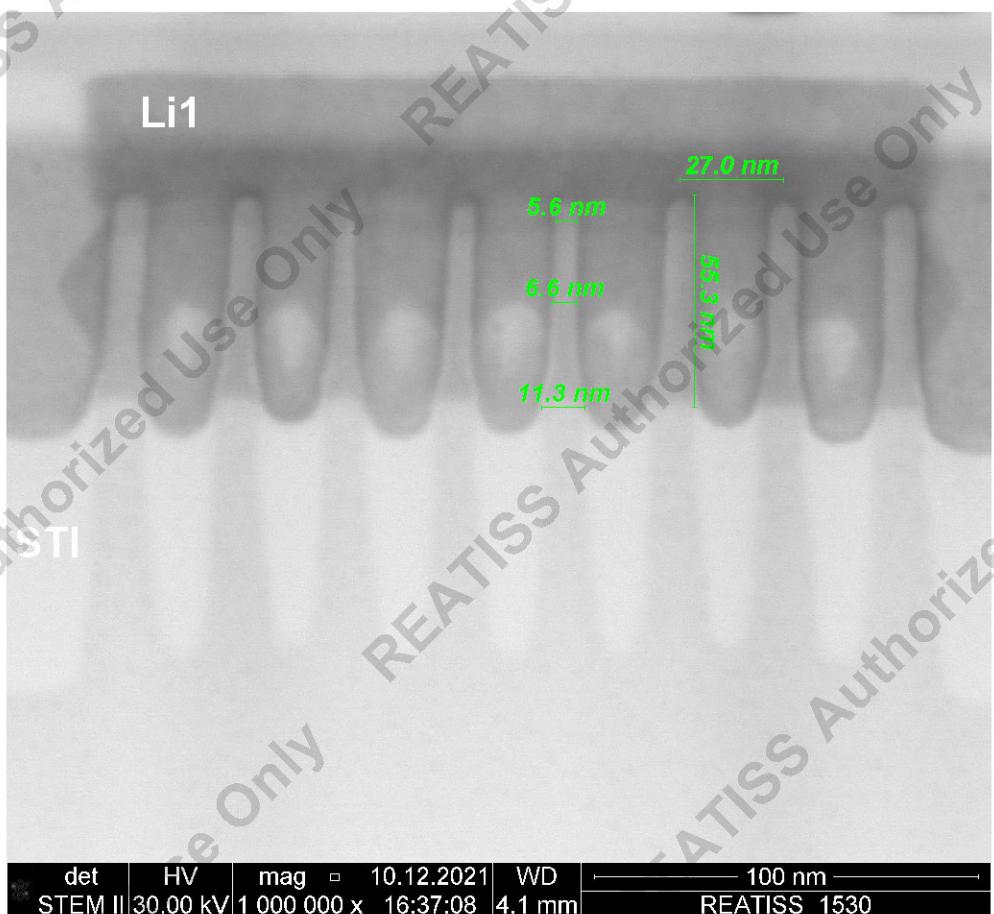


Figure 129. Co Li1, FinFETs across fins, STI

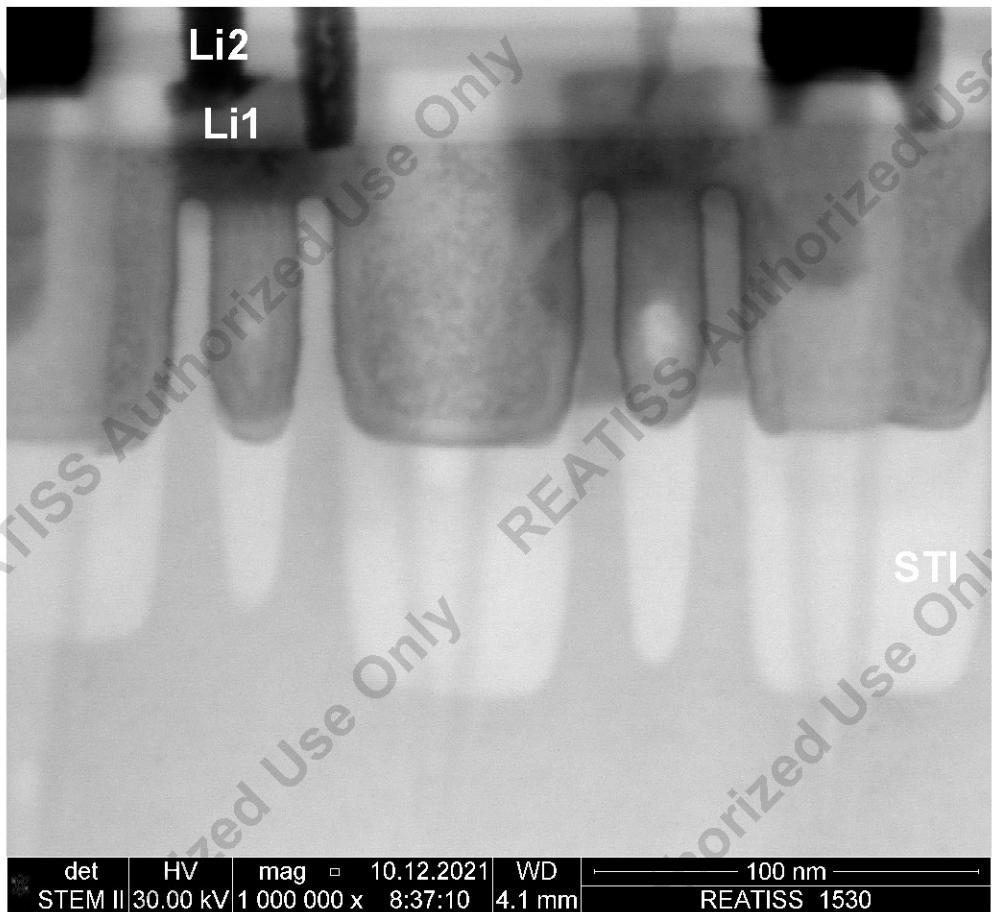


Figure 130. Co Li1, W Li2, FinFETs across fins, STI

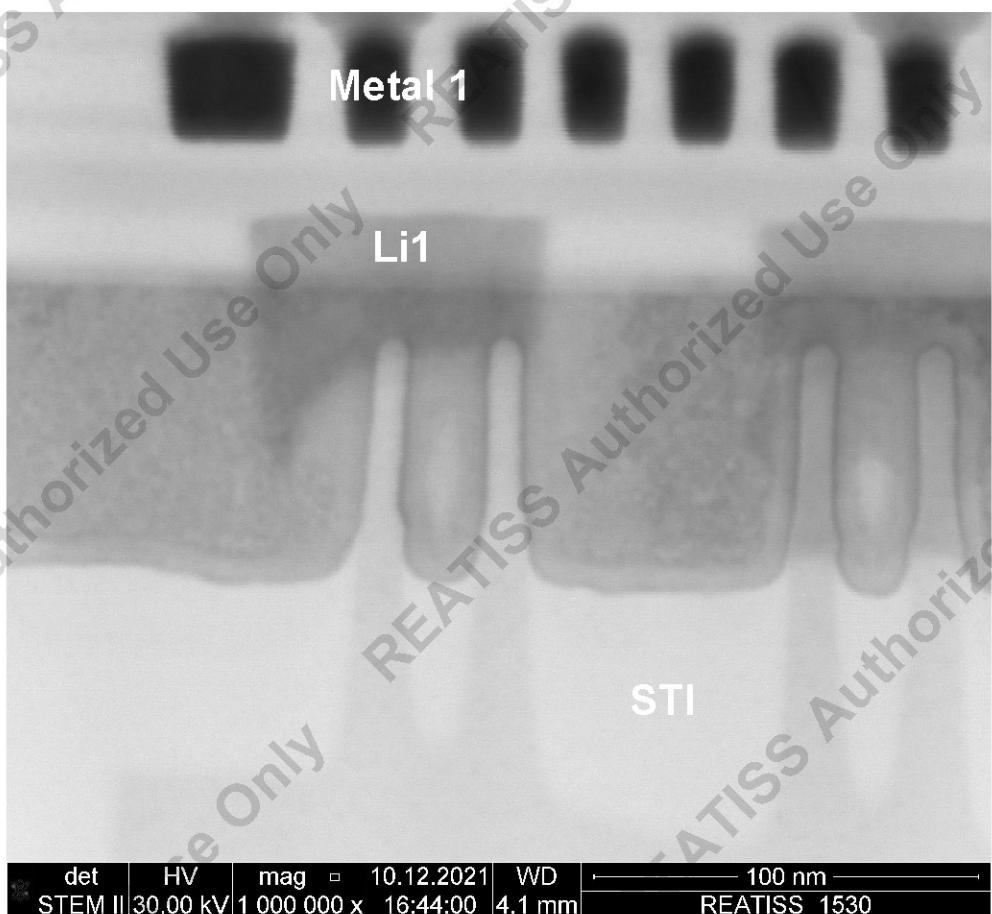


Figure 131. Co Li1, Cu M1 lines, FinFETs across fins, STI

Material Analysis

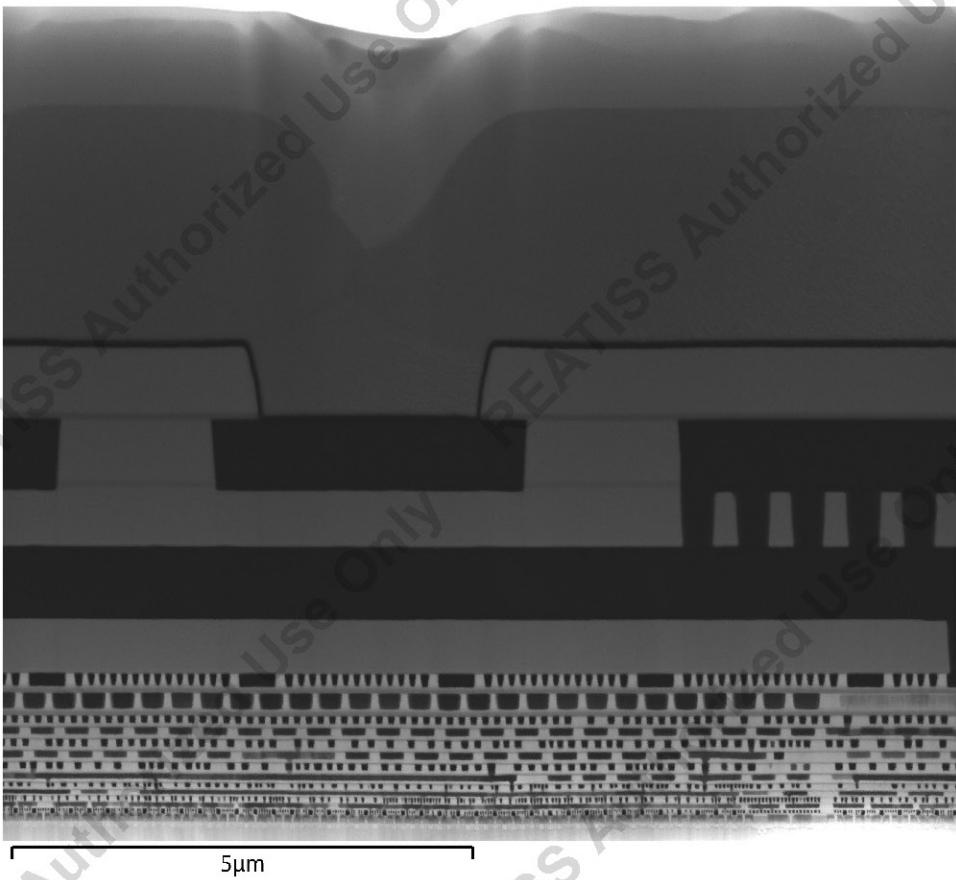


Figure 132. General view



Figure 133. Layered EDX map of general view

Al K series

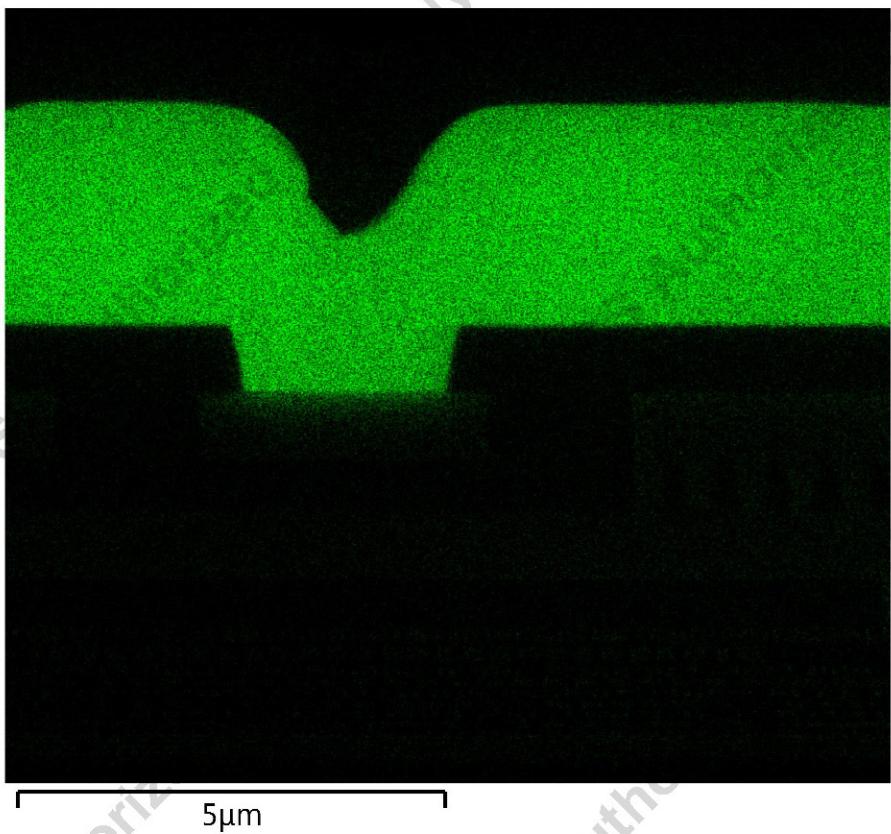


Figure 134. Aluminum EDX map layer

Cu K series

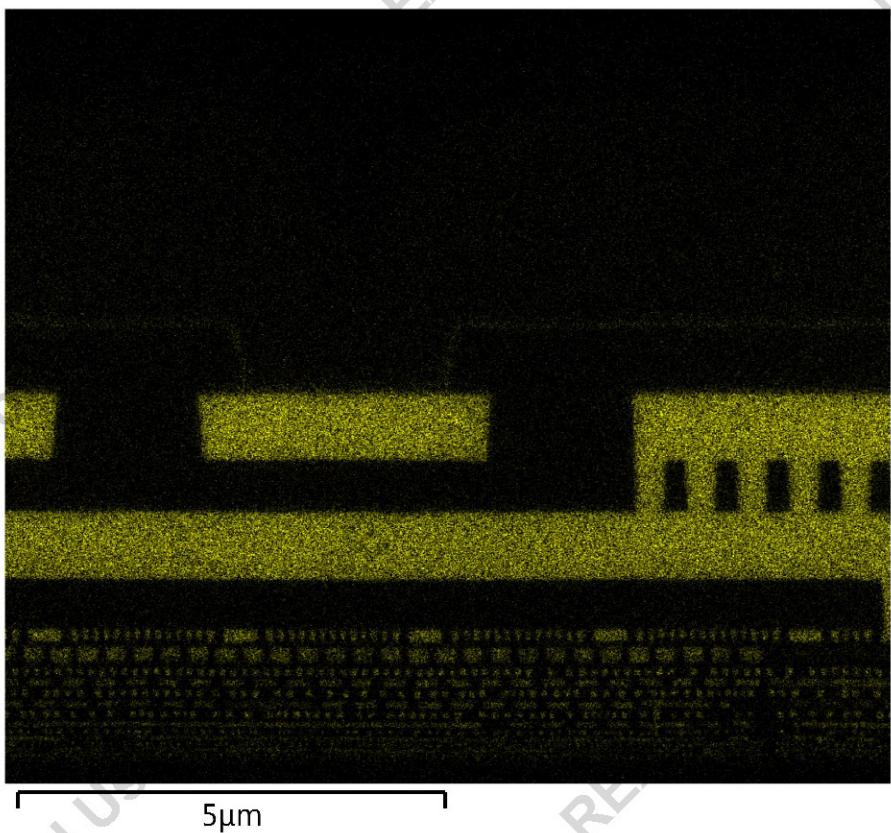


Figure 135. Copper EDX map layer

Ta L series

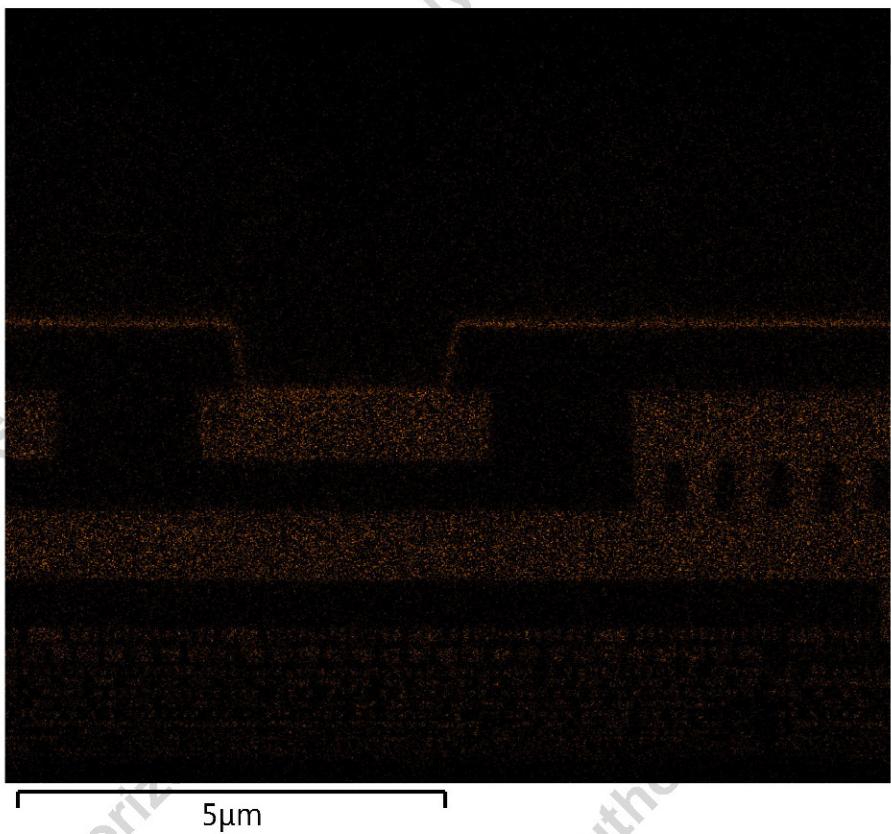


Figure 136. Tantalum EDX map layer

Si K series

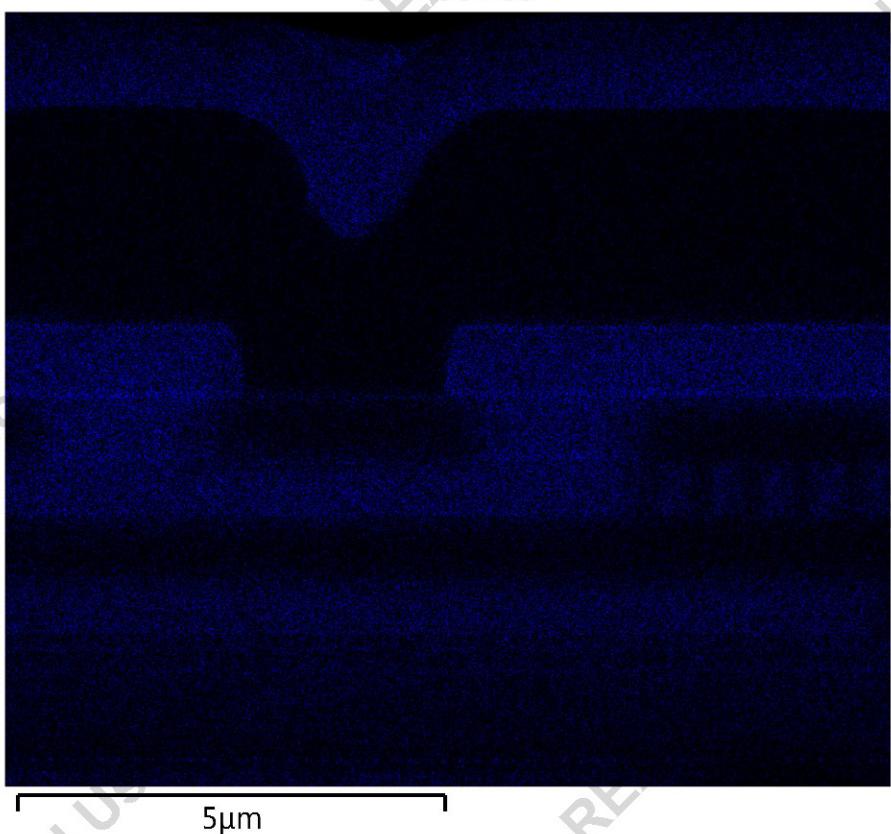


Figure 137. Silicon EDX map layer

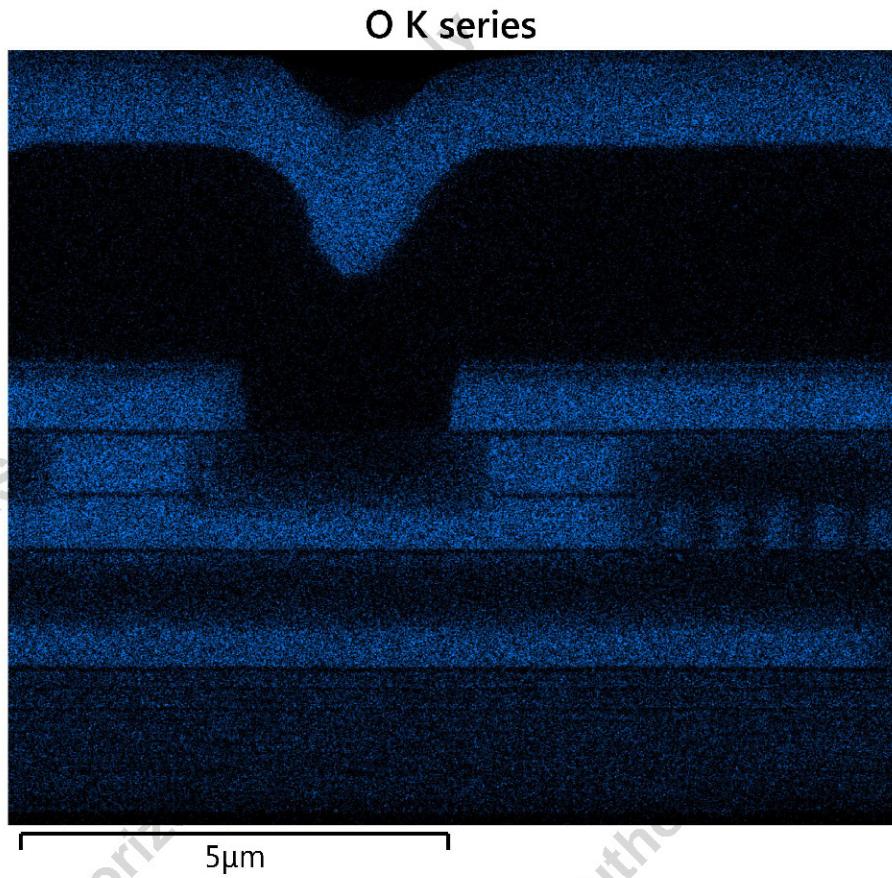


Figure 138. Oxygen EDX map layer

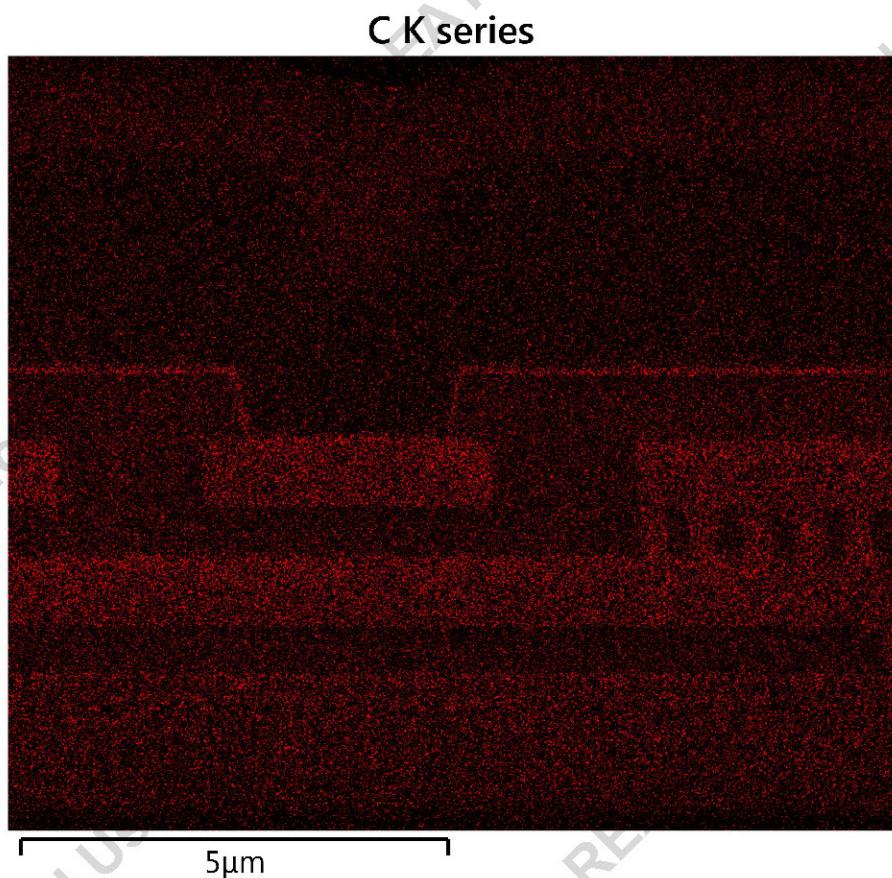


Figure 139. Carbon EDX map layer

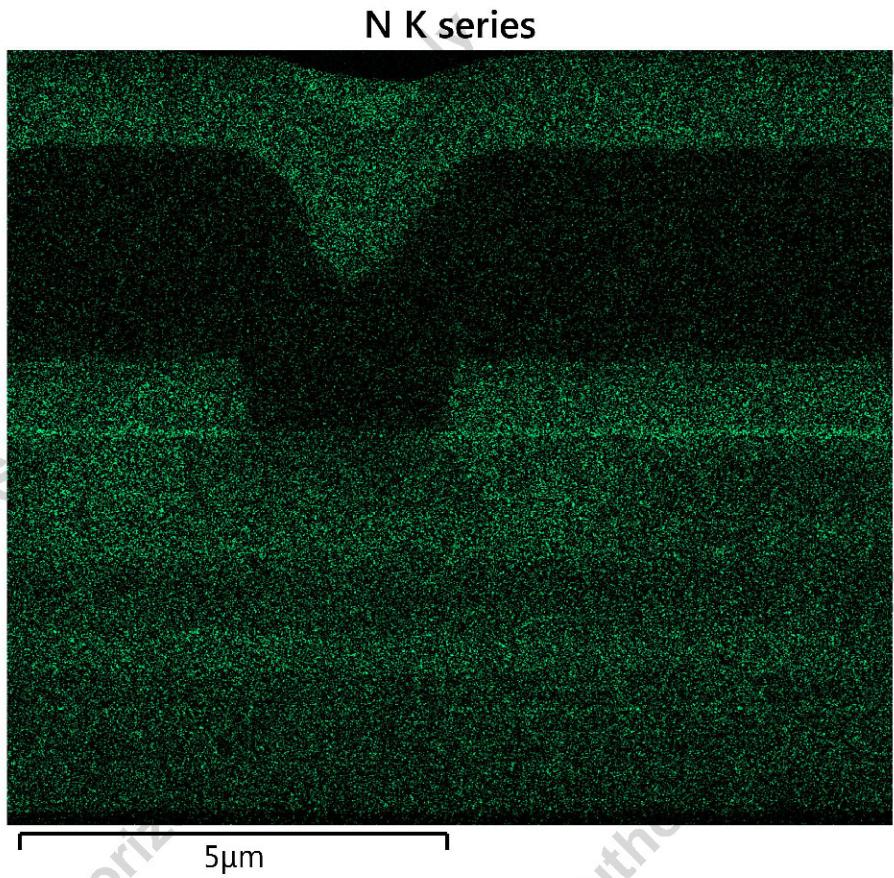


Figure 140. Nitrogen EDX map layer

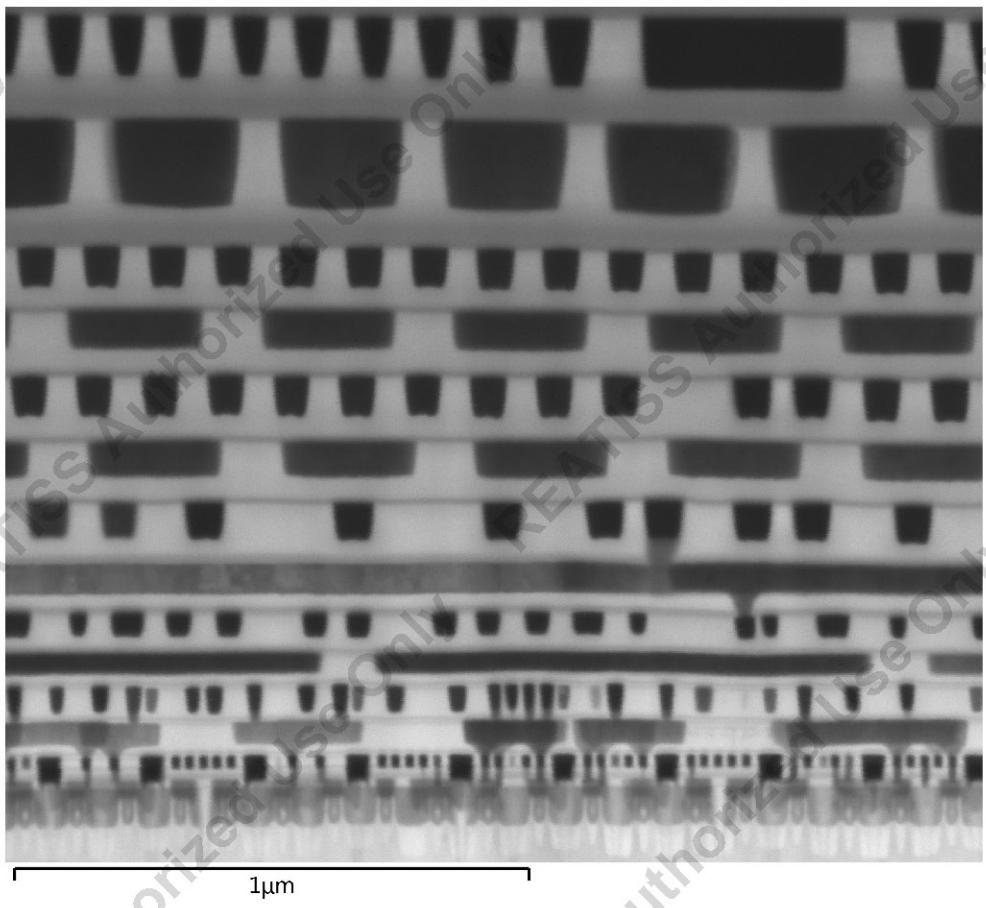


Figure 141. Co Li1, W Li2, Cu M1-M13 lines, Cu vias

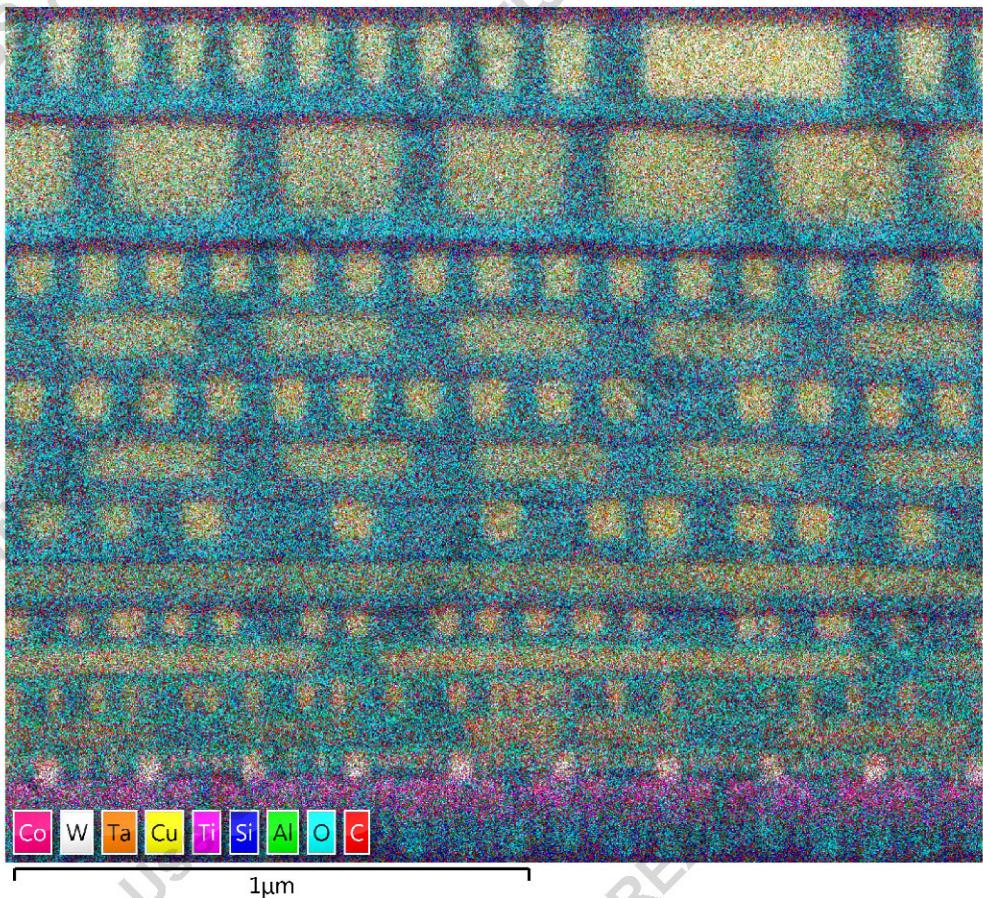


Figure 142. Layered EDX map of Co Li1, W Li2, Cu M1-M13 lines, Cu vias

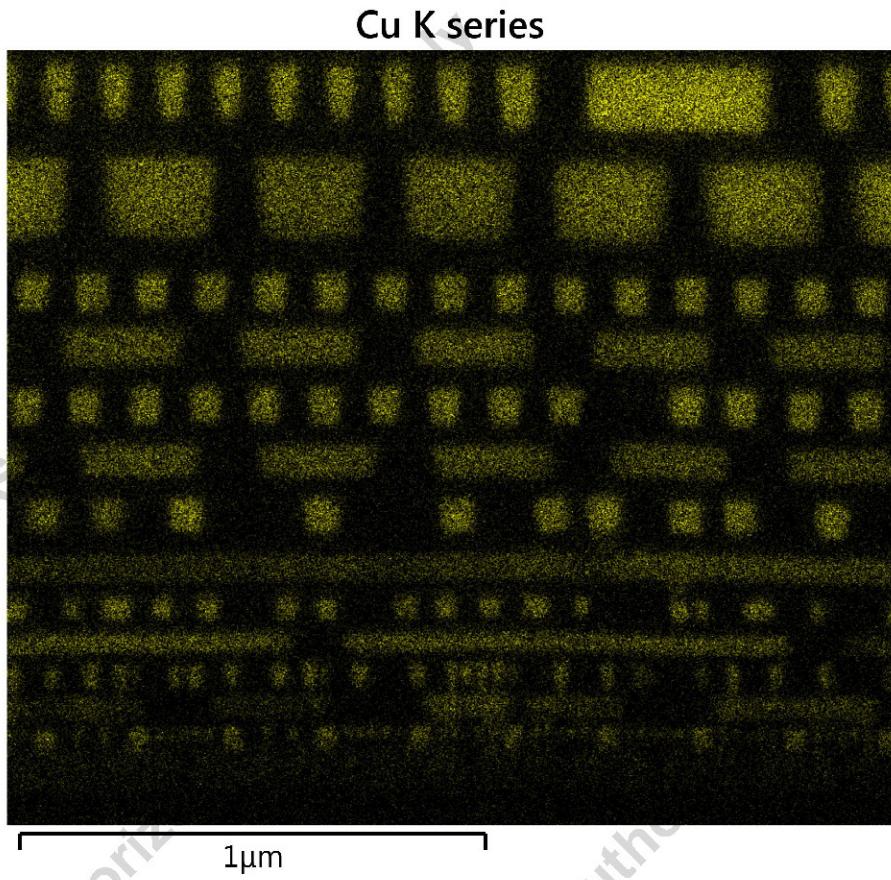


Figure 143. Copper EDX map layer

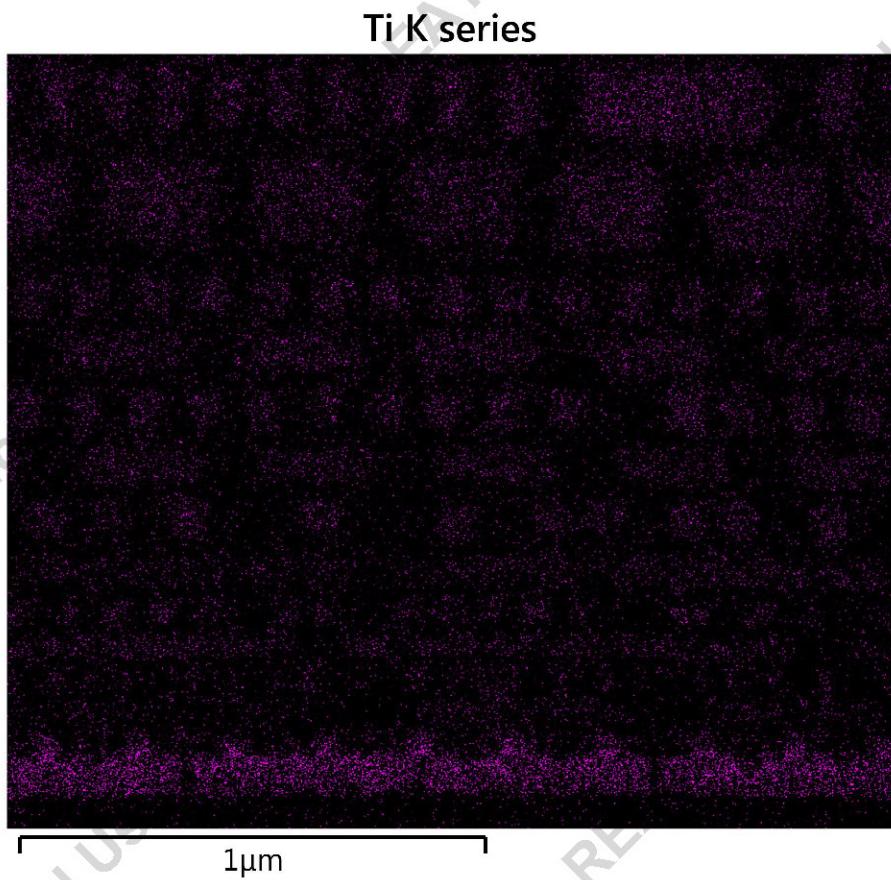


Figure 144. Titanium EDX map layer

Ta L series

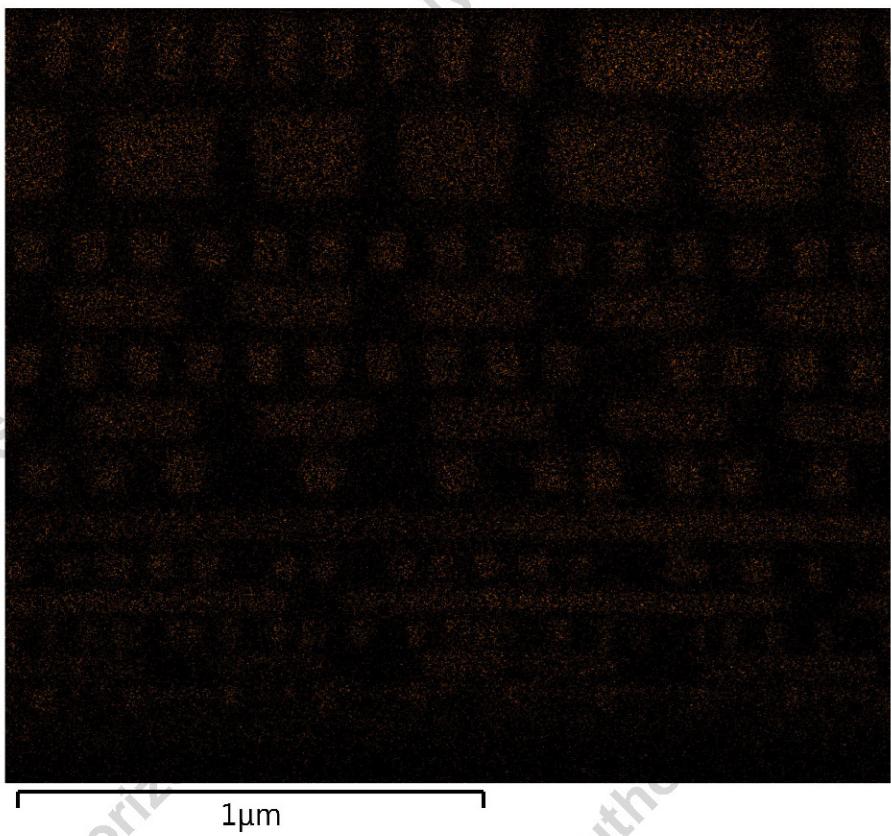


Figure 145. Tantalum EDX map layer

Co K series

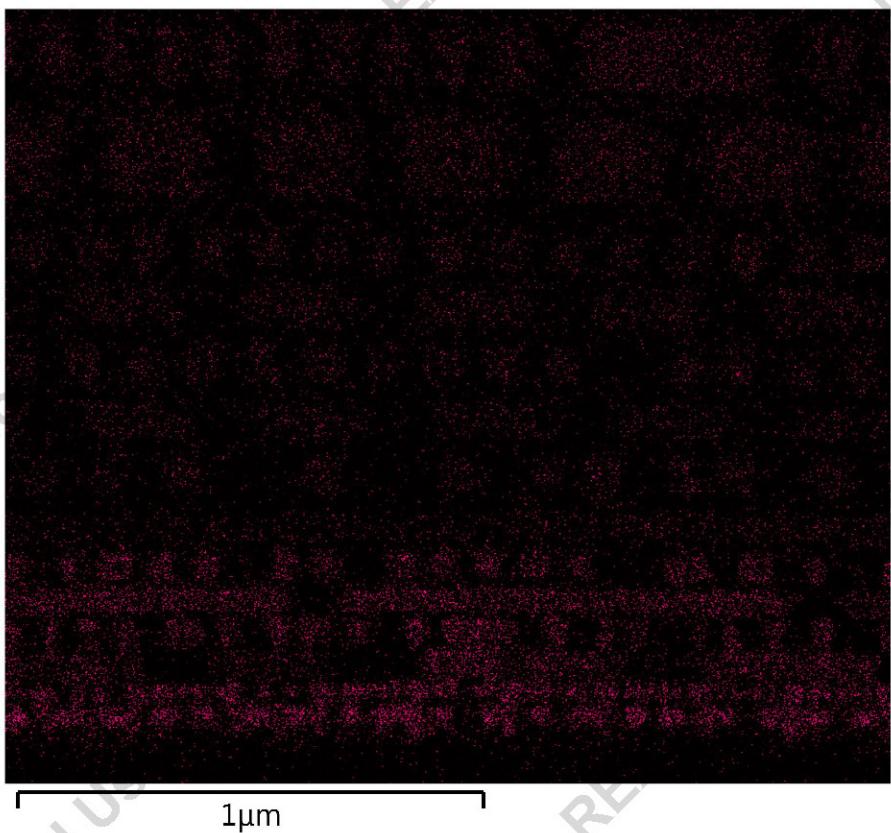


Figure 146. Cobalt EDX map layer

W L series

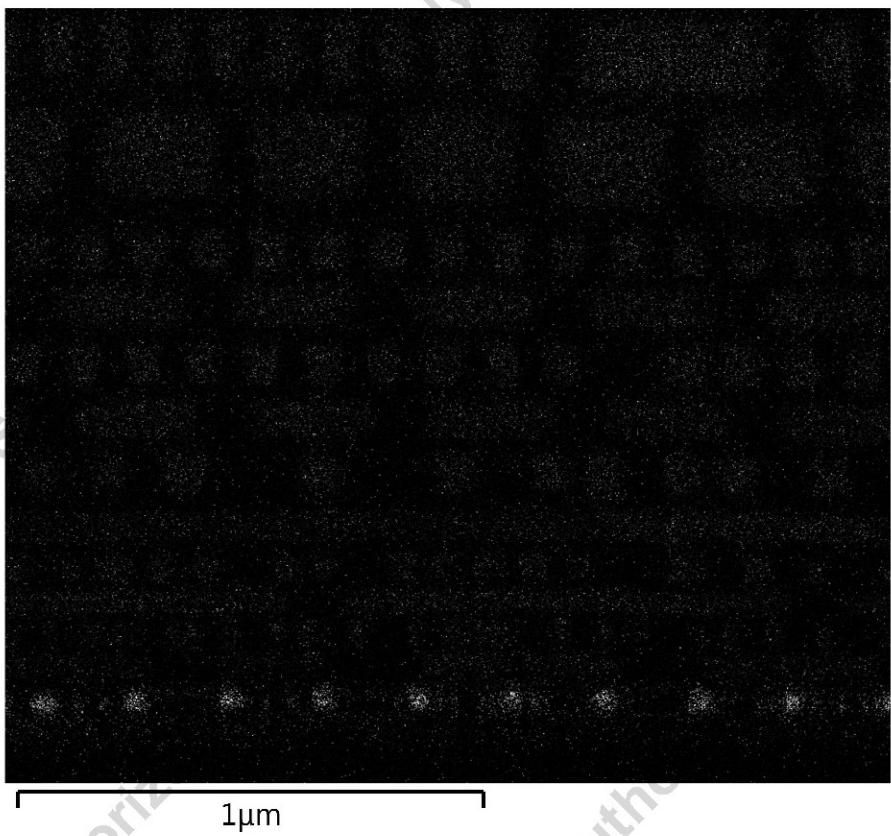


Figure 147. Tungsten EDX map layer

Al K series

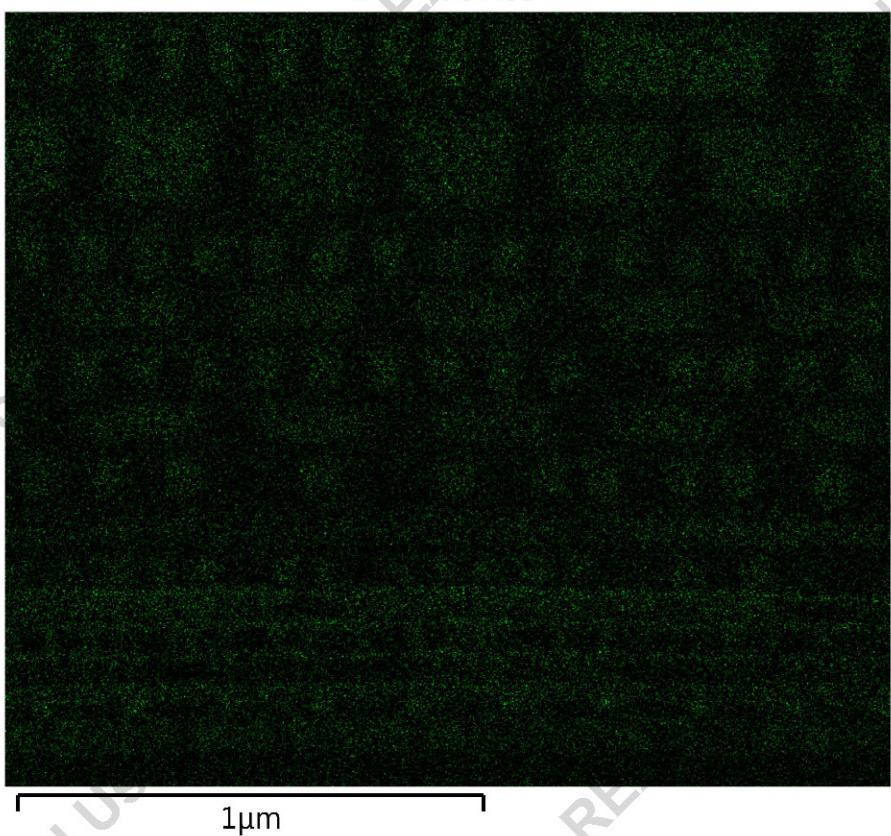


Figure 148. Aluminum EDX map layer

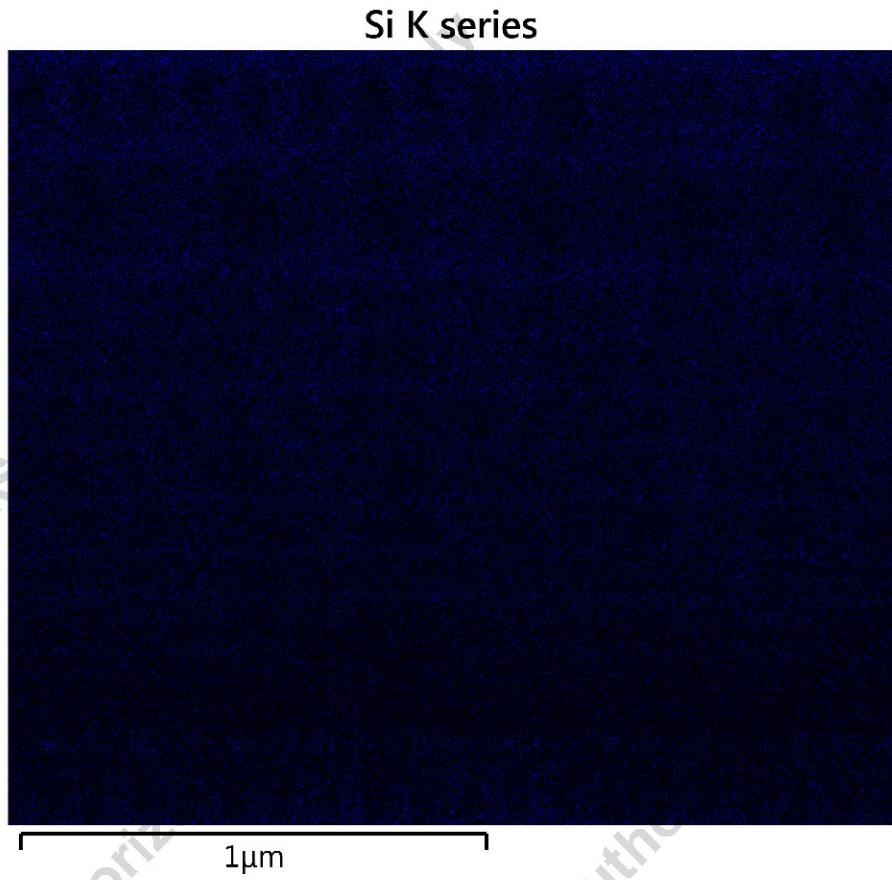


Figure 149. Silicon EDX map layer

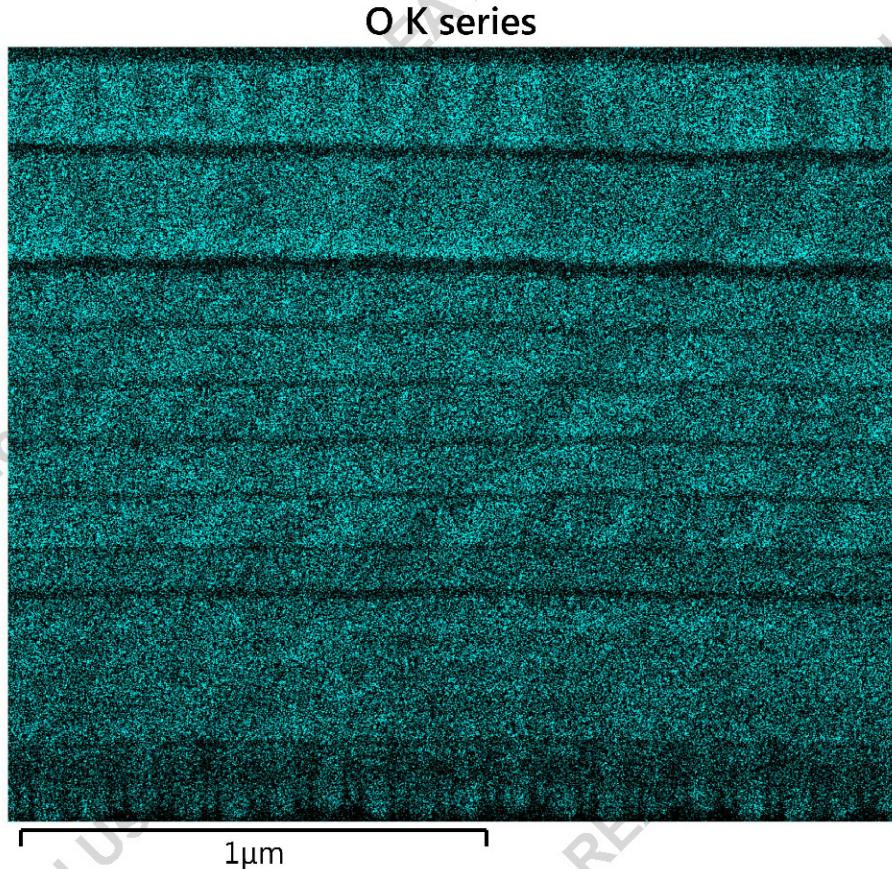


Figure 150. Oxygen EDX map layer

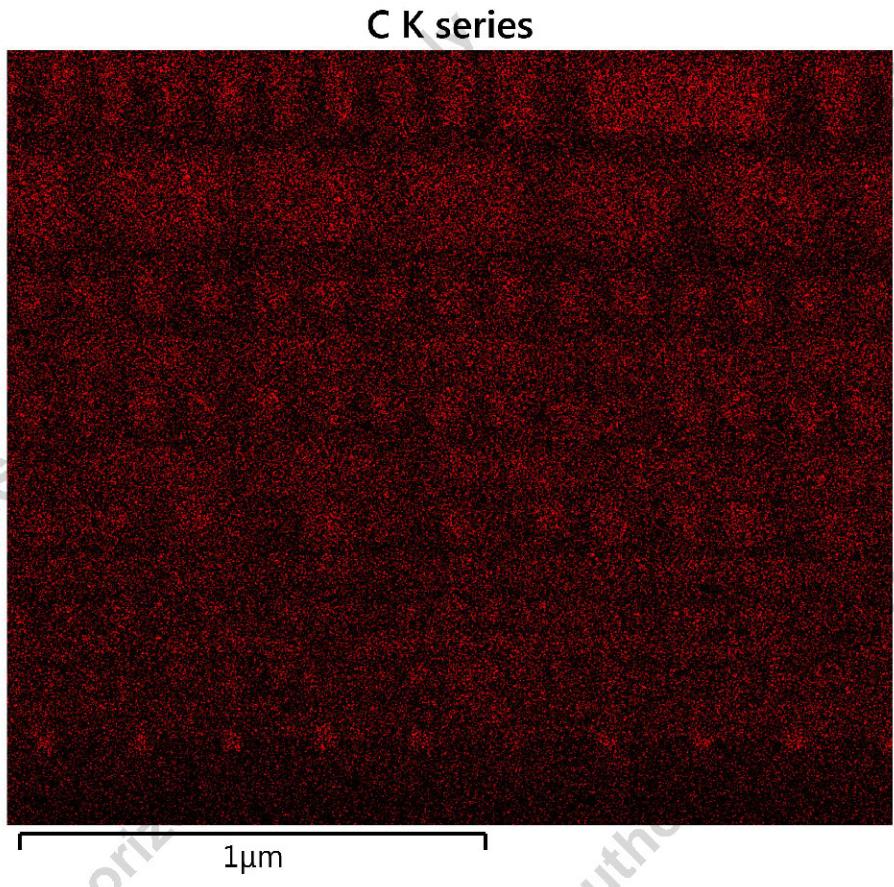


Figure 151. Carbon EDX map layer



Figure 152. Co Li1, W Li2, Cu M1-M8 lines, FinFETs across fins

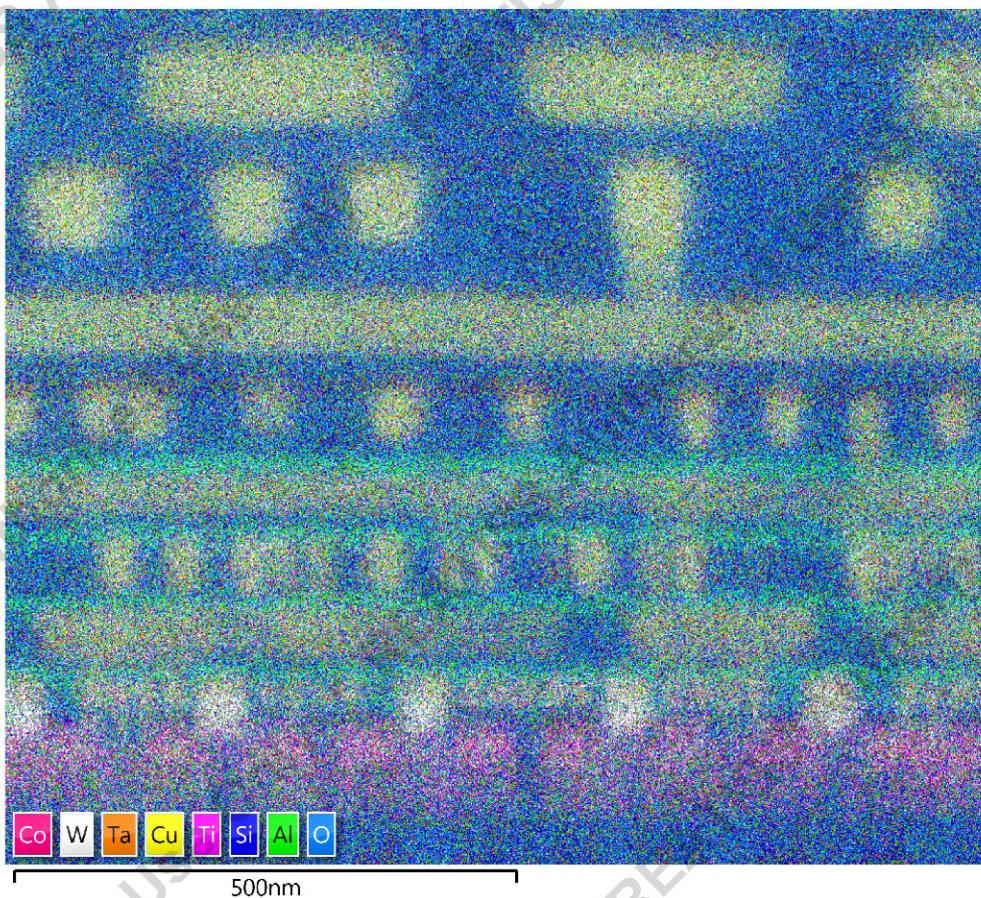


Figure 153. Layered EDX map of Co Li1, W Li2, Cu M1-M8 lines, FinFETs across fins

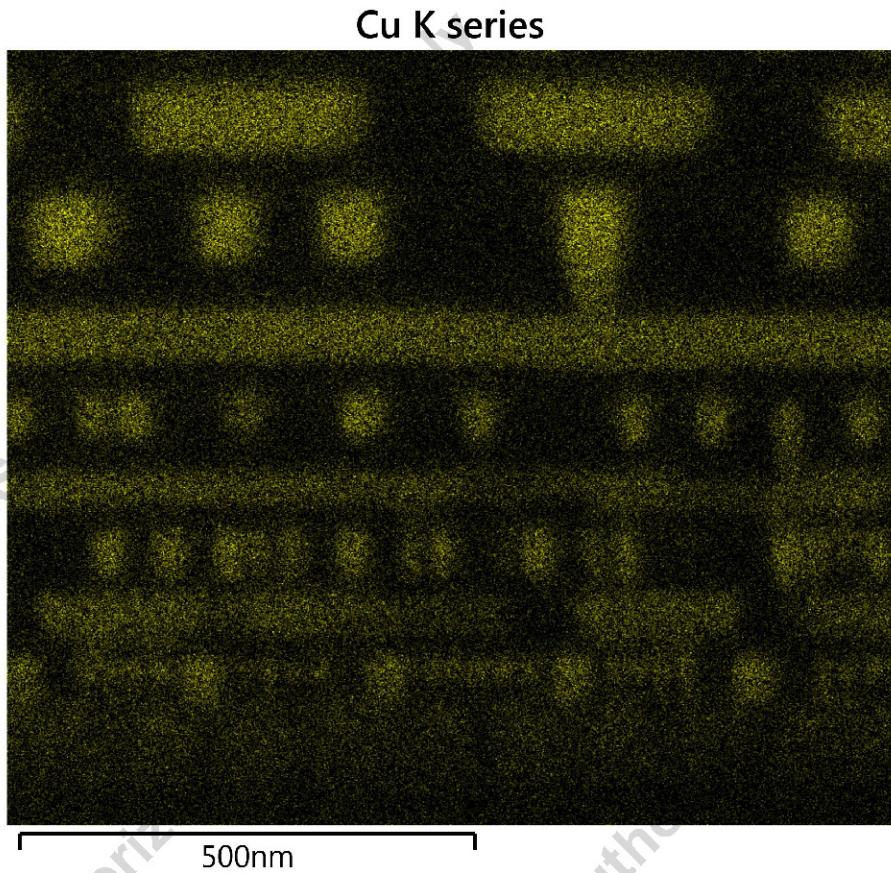


Figure 154. Copper EDX map layer

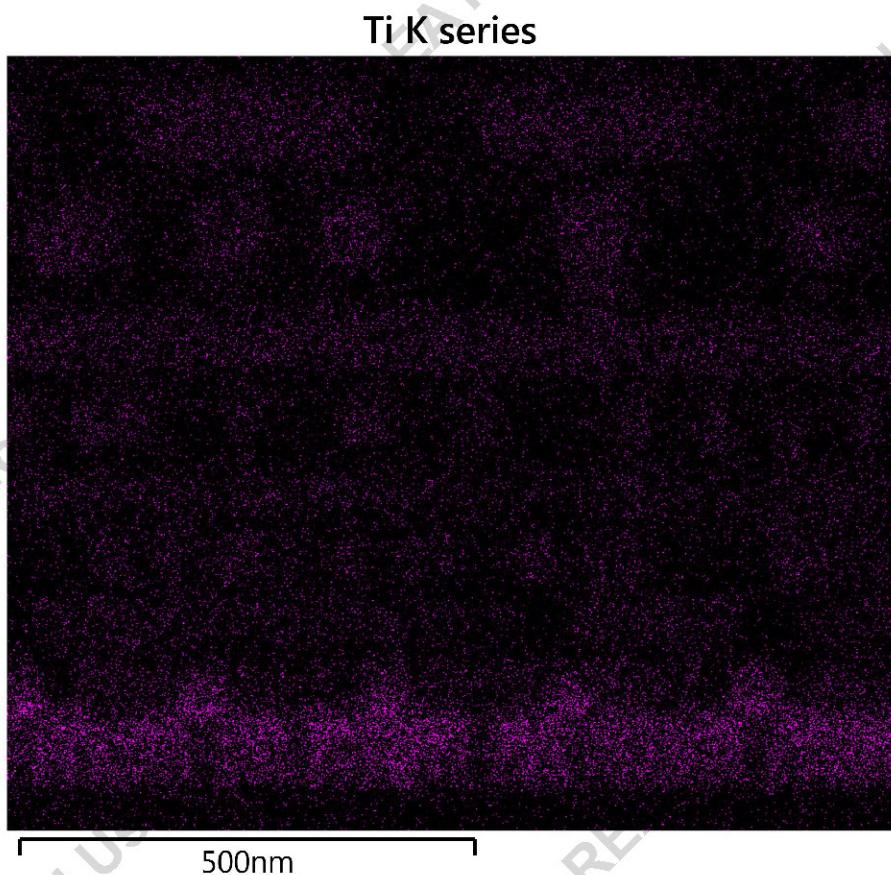


Figure 155. Titanium EDX map layer

Ta L series

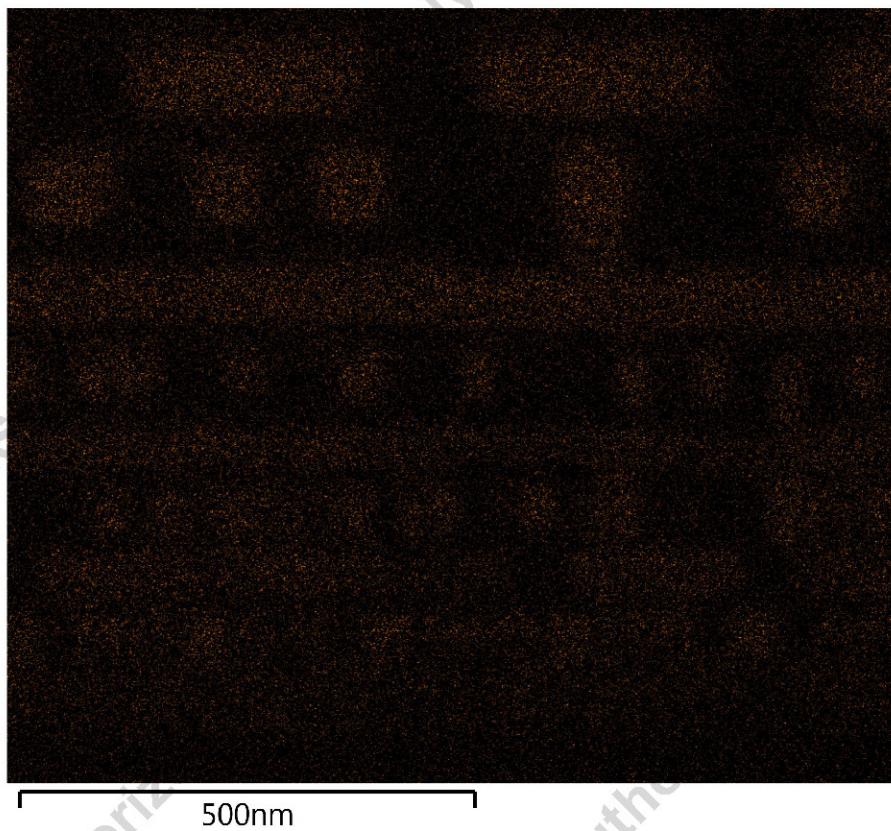


Figure 156. Tantalum EDX map layer

Co K series

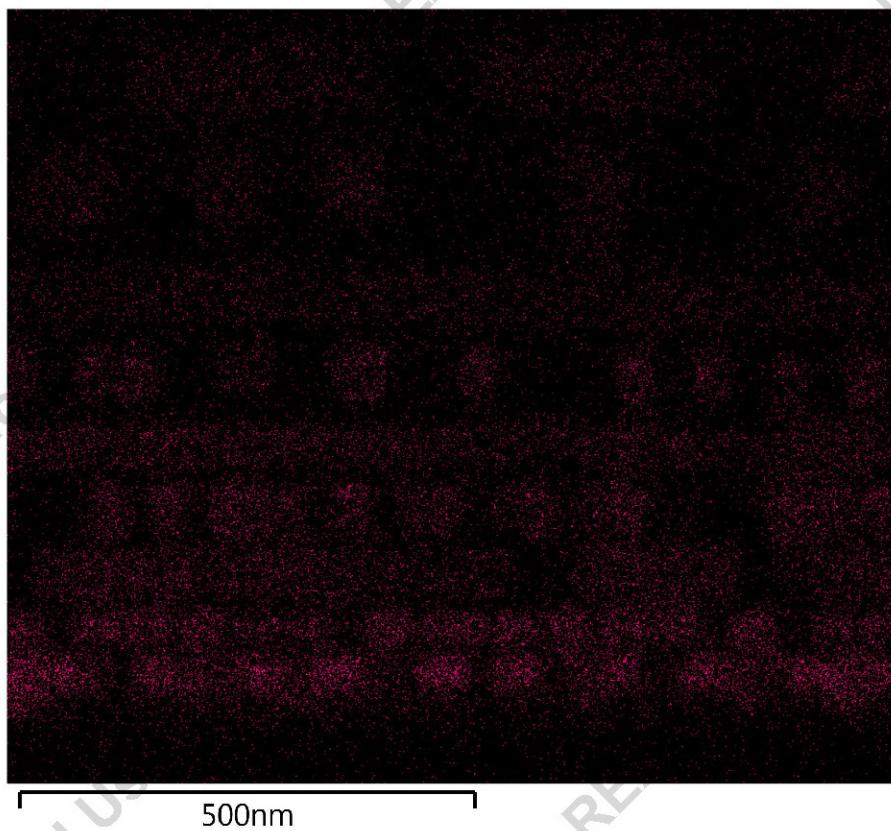


Figure 157. Cobalt EDX map layer

W L series

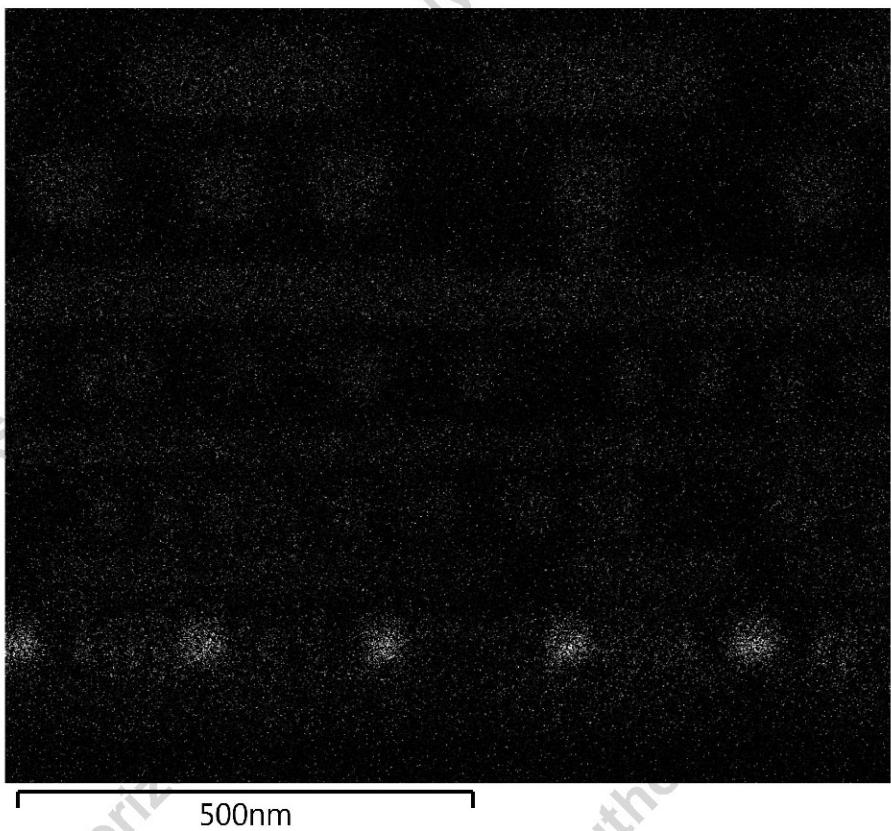


Figure 158. Tungsten EDX map layer

Al K series

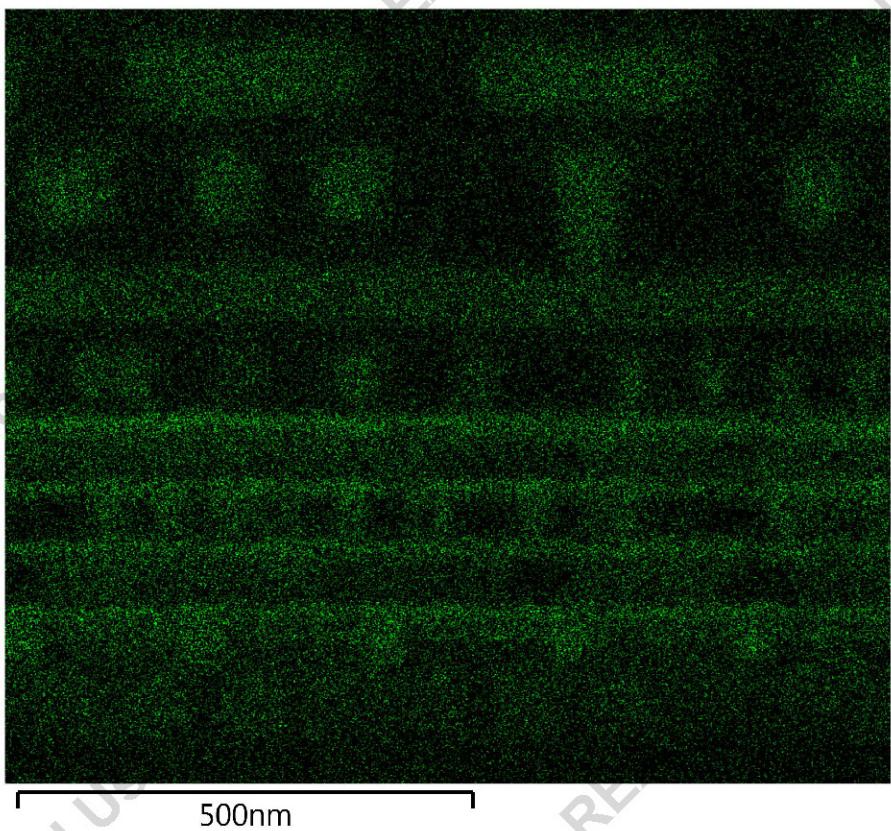


Figure 159. Aluminum EDX map layer

Si K series

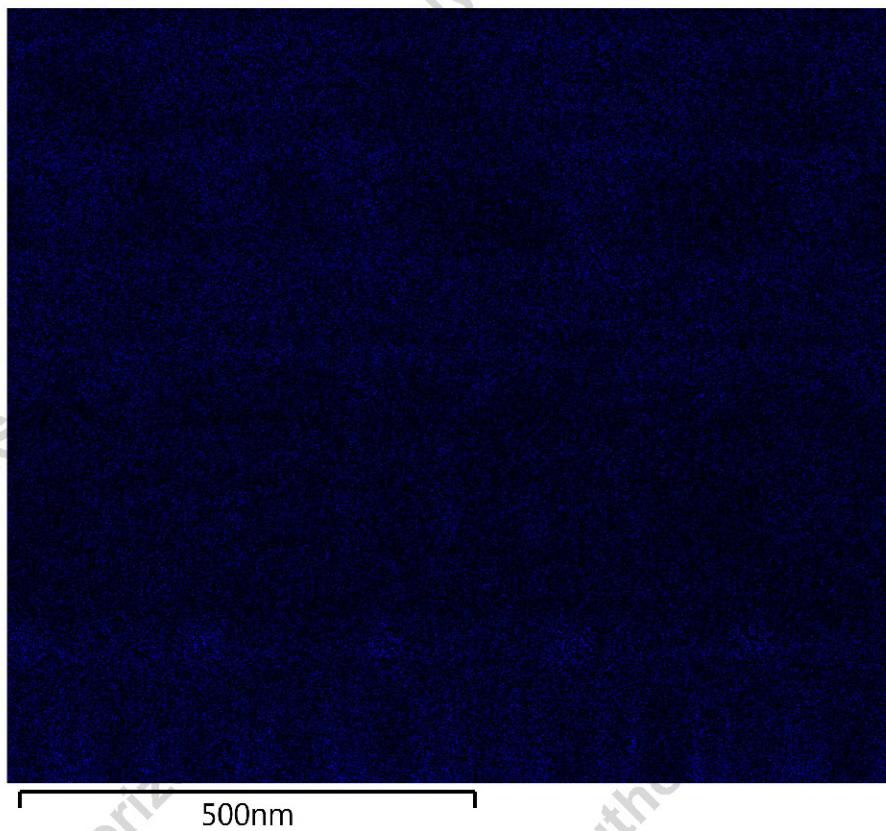


Figure 160. Silicon EDX map layer

O K series

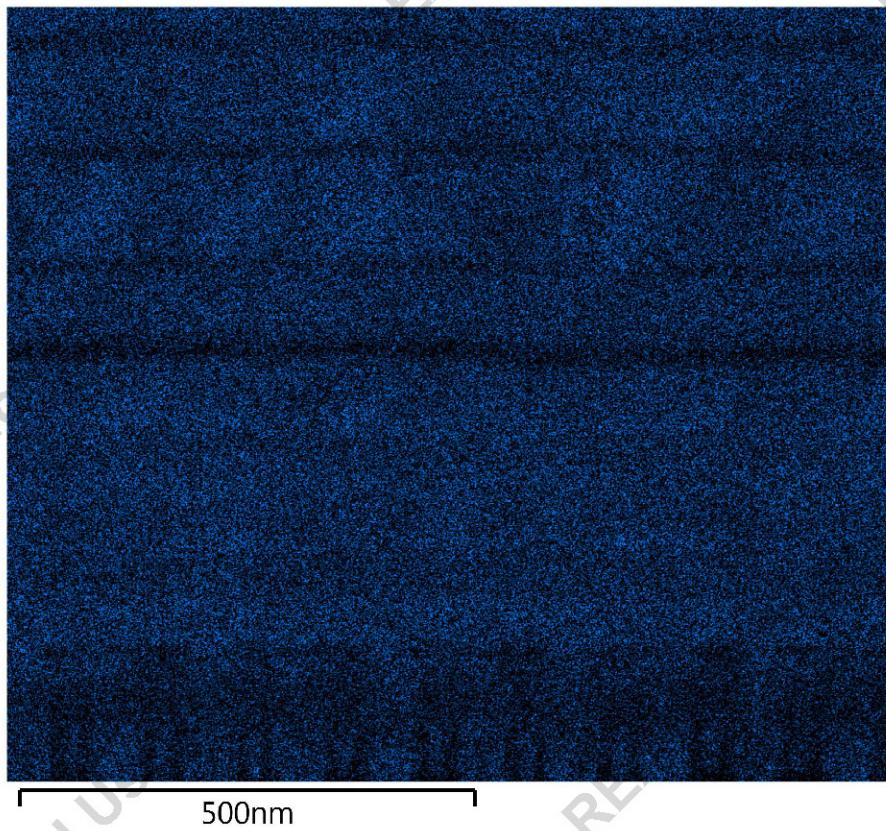


Figure 161. Oxygen EDX map layer

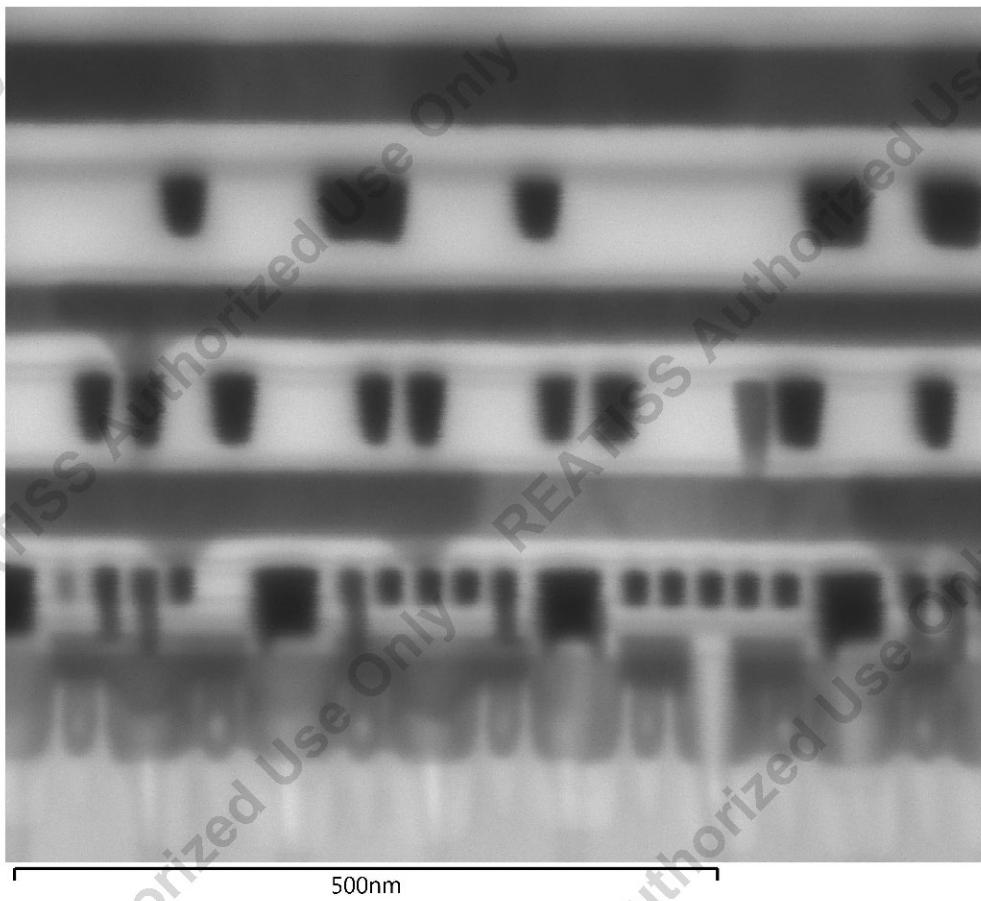


Figure 162. Co Li1, W Li2, Cu M1-M6 lines, FinFETs across fins

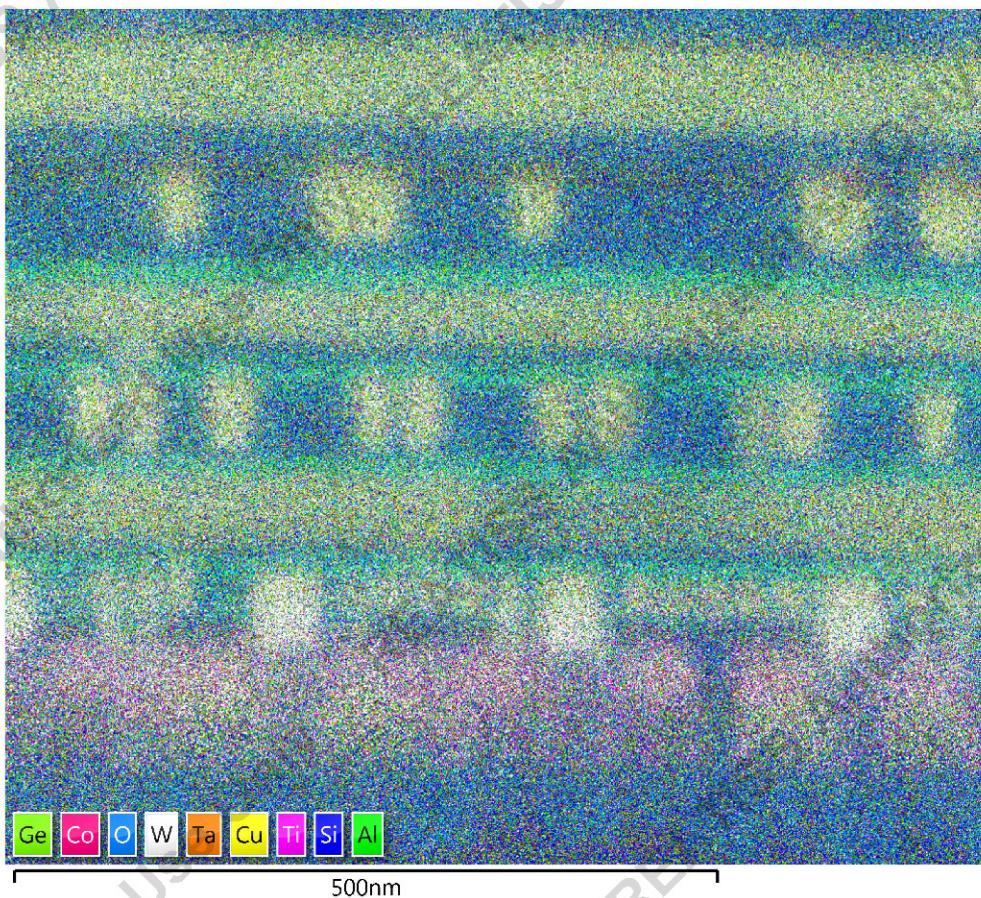


Figure 163. Layered EDX map of Co Li1, W Li2, Cu M1-M6 lines, FinFETs across fins

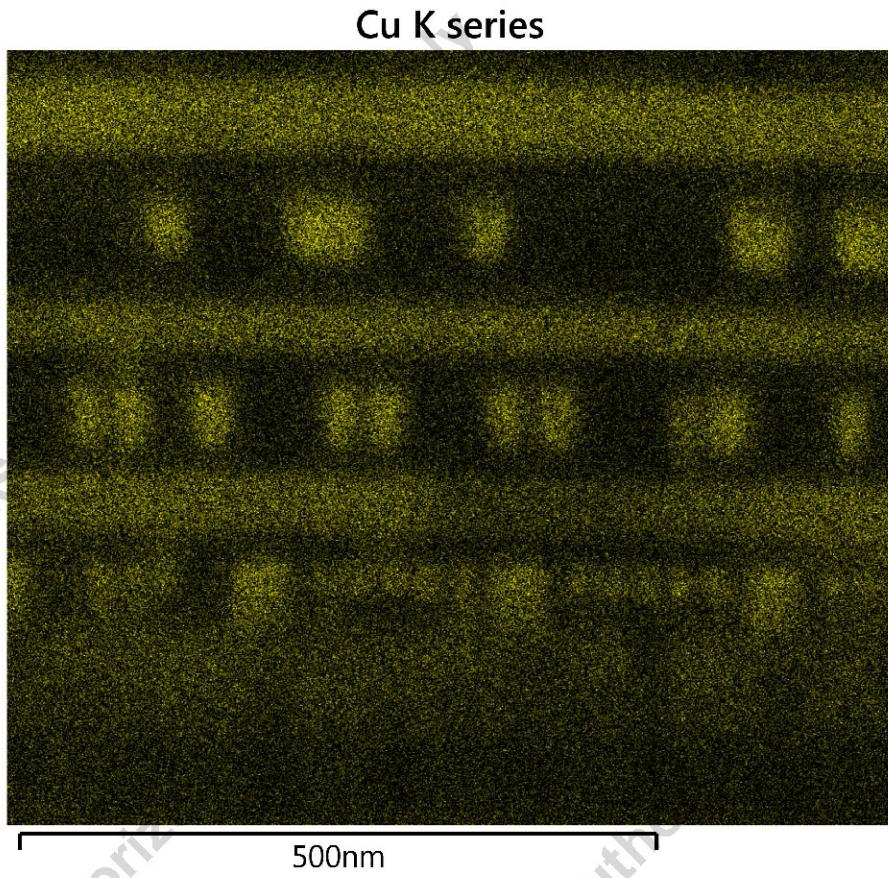


Figure 164. Copper EDX map layer

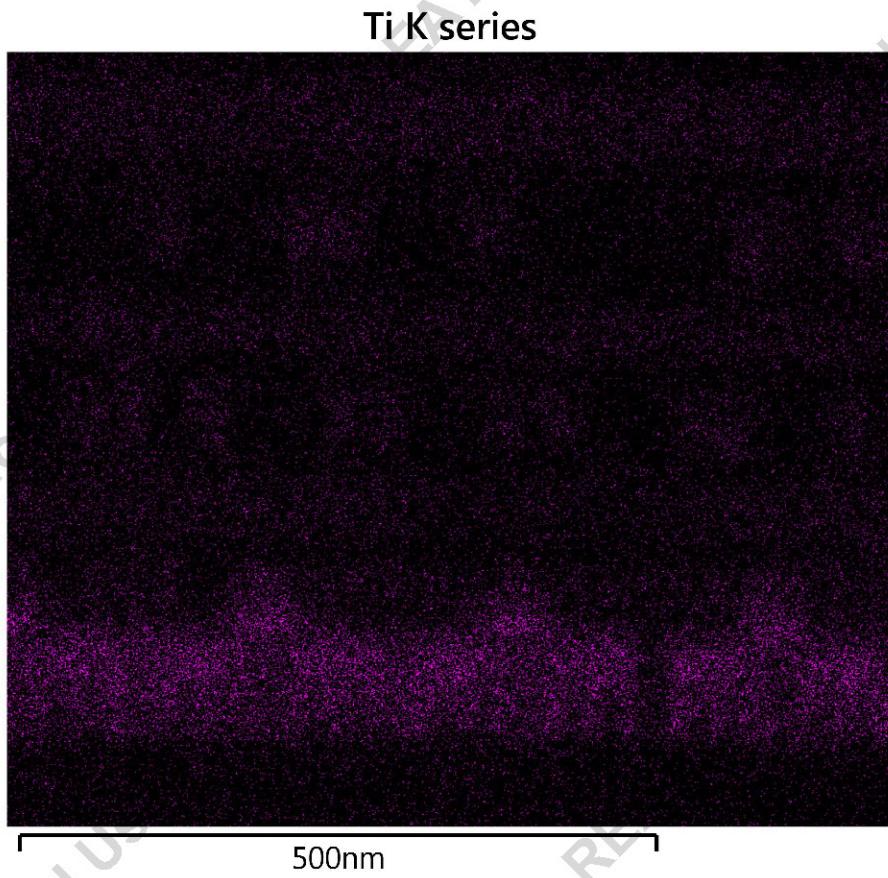


Figure 165. Titanium EDX map layer

Ta L series

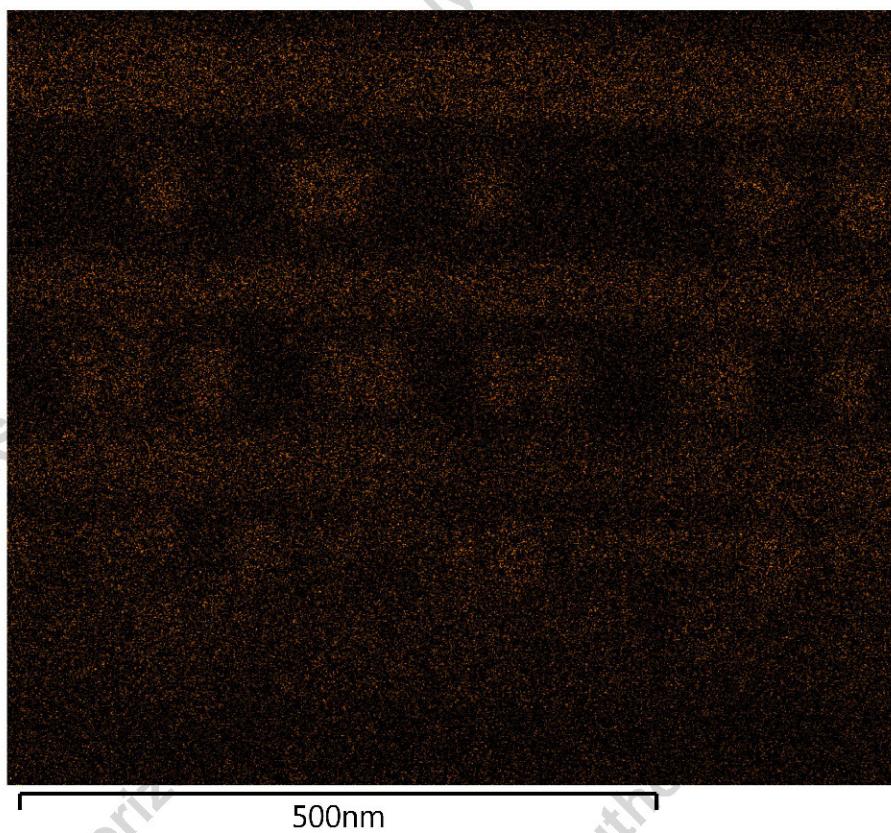


Figure 166. Tantalum EDX map layer

Co K series

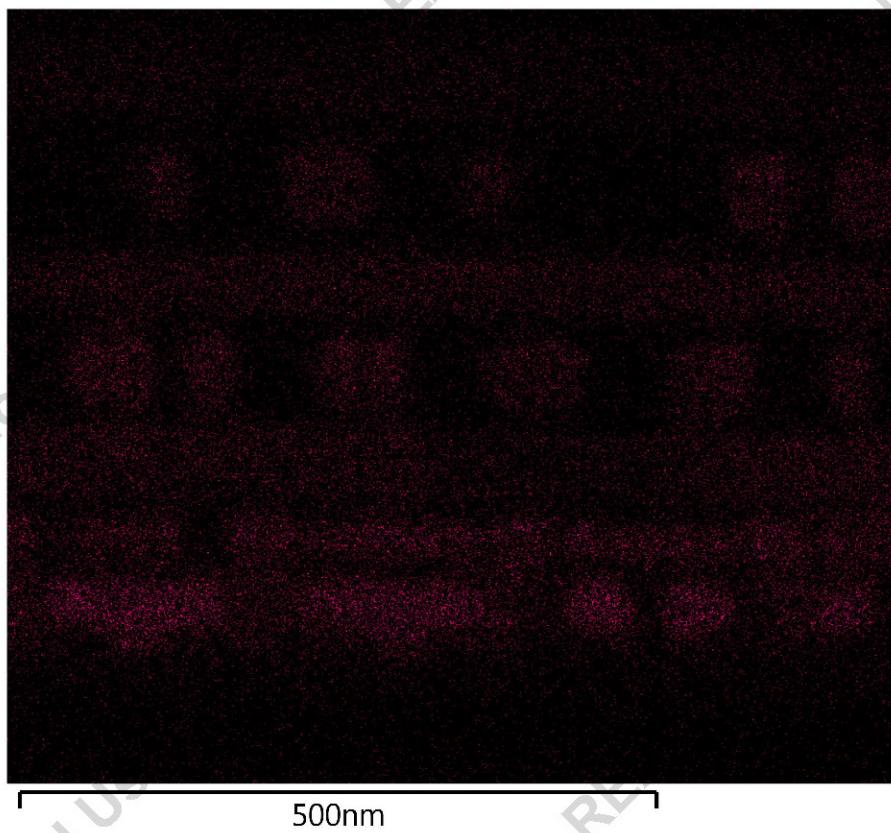


Figure 167. Cobalt EDX map layer

W L series

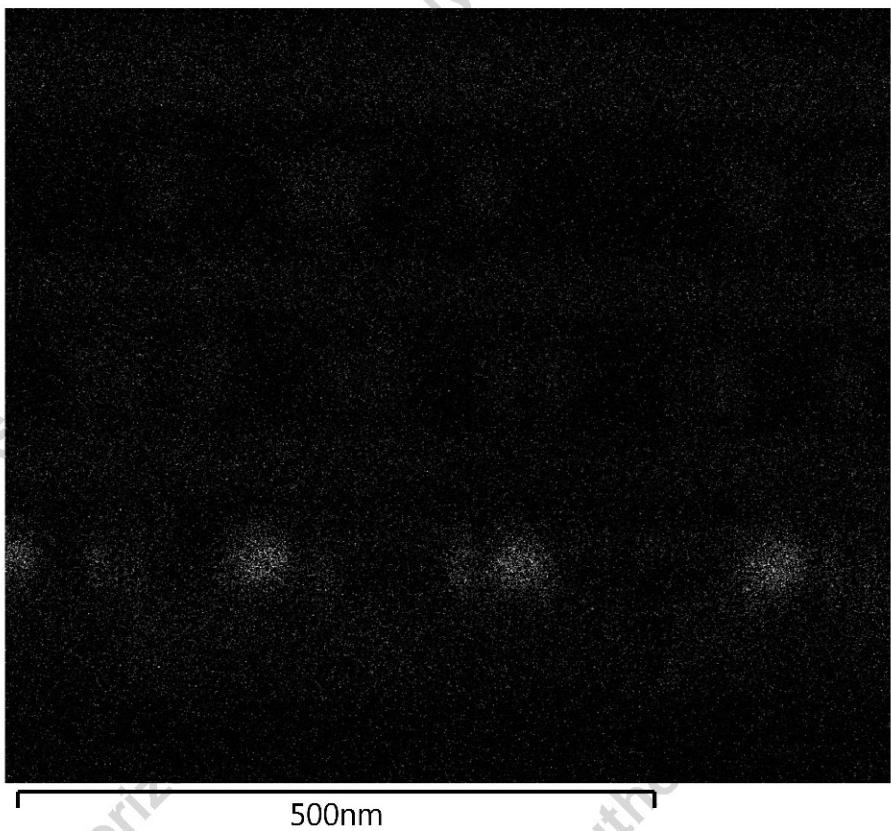


Figure 168. Tungsten EDX map layer

Ge K series

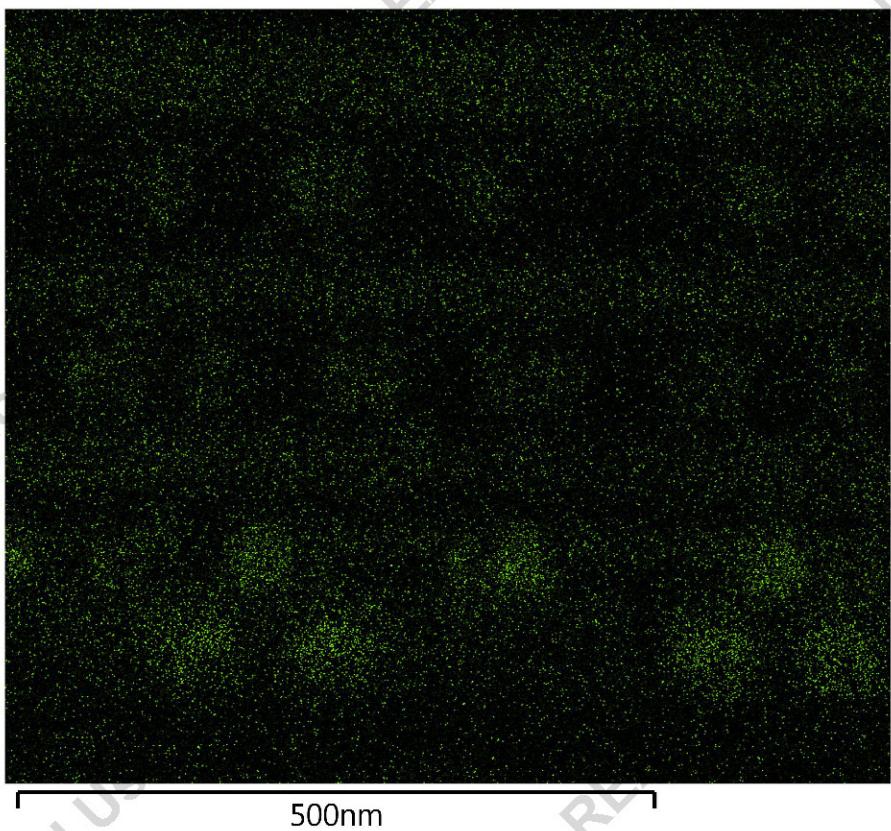


Figure 169. Germanium EDX map layer

Al K series

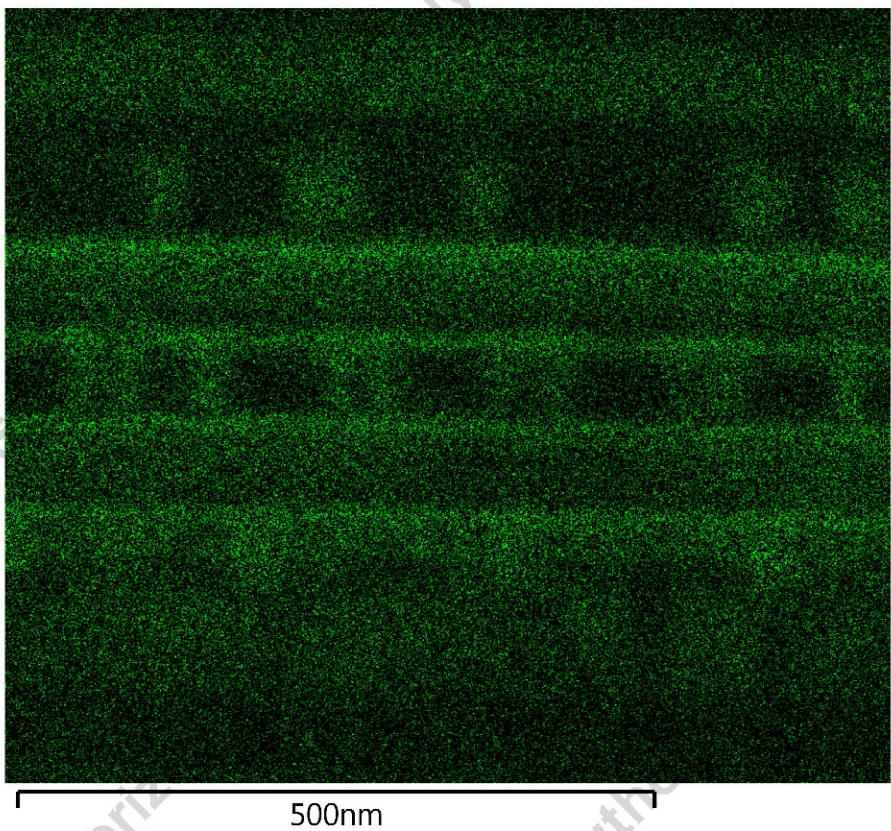


Figure 170. Aluminum EDX map layer

Si K series

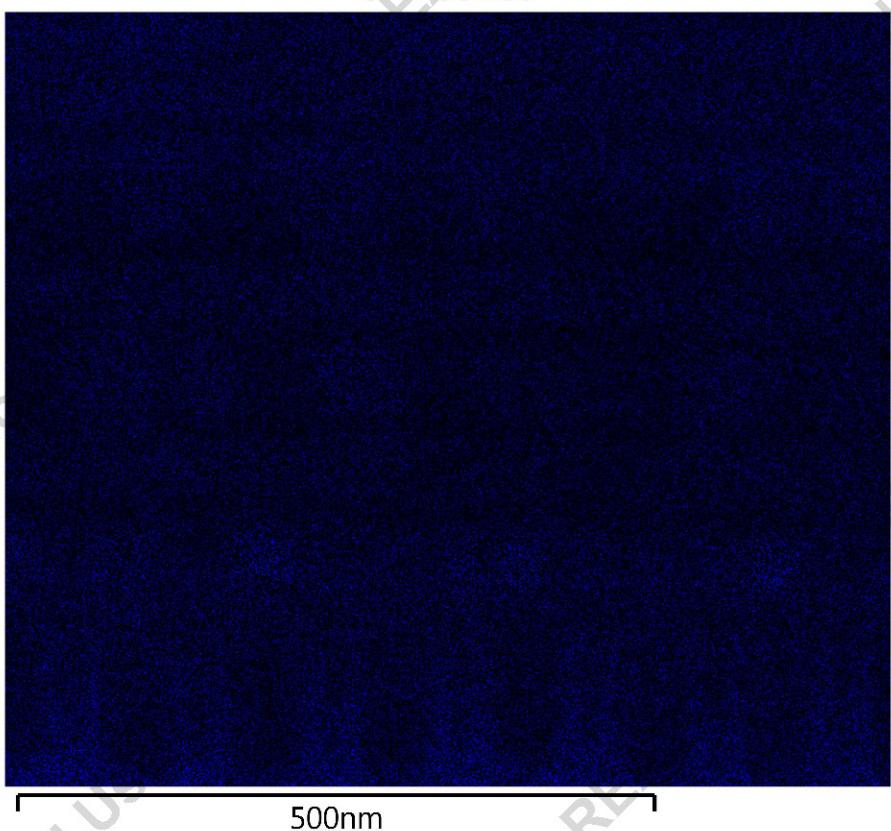


Figure 171. Silicon EDX map layer

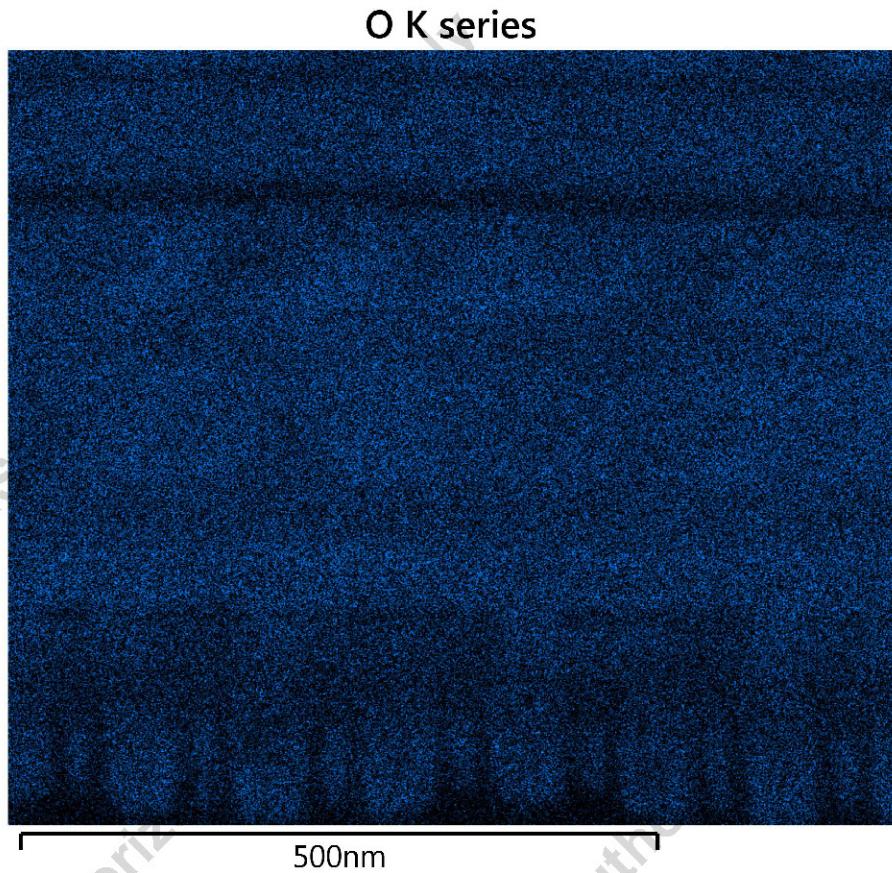


Figure 172. Oxygen EDX map layer