

Micron 
3D NAND Flash Memory

Process Analysis Report

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Device Summary Sheet

Manufacturer: Micron Technology, Inc.

Part Number: [REDACTED]

Date Code: Not identified

IC Type: Flash Memory

Technology synopsis

Package Type: BGA

Pin Count: 121

Package Size: 18,1 mm x 12,1 mm x 0,8 mm

Die Count: 3

Die Size: 15,28 mm x 11 mm (by edge of physical silicon)

15,22 mm x 10,9 mm (by edge of seal)

Number of Metal Layers: 4. One layer of aluminum interconnect and three layers of tungsten interconnect.

3D Flash memory stack comprises 38 polysilicon control gates, top and bottom select gates and bottom common electrode.

Gate Layer: One layer of polysilicon

Minimum Printed Gate Length: 307 nm

Device Isolation Type: STI

Source Device



Figure 1. [Redacted] SSD front side



Figure 2. [Redacted] SSD back side

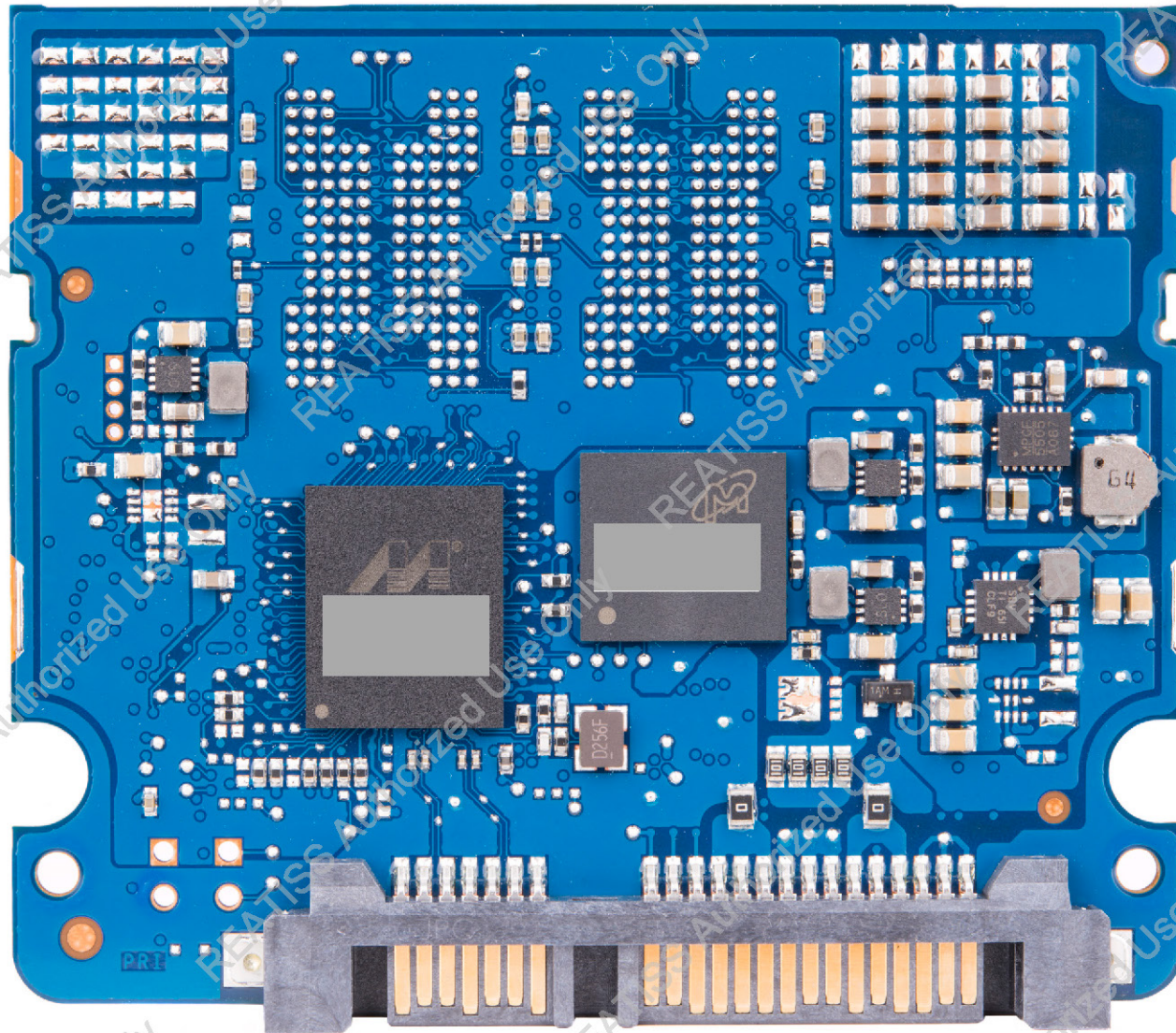


Figure 3. [Redacted] SSD PCB side A

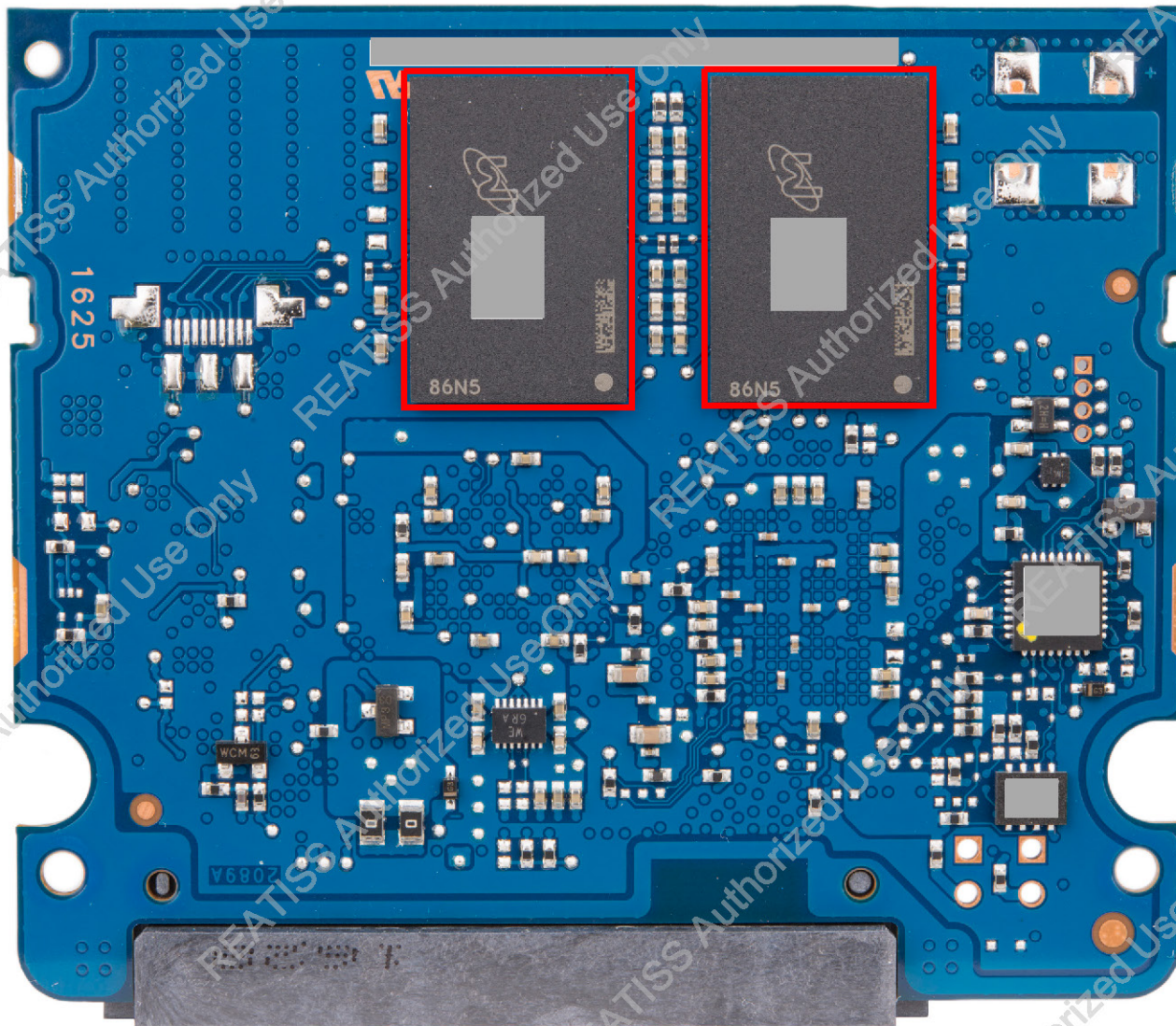




Figure 4.  SSD PCB side B

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Die and Package



Figure 5. Top package view

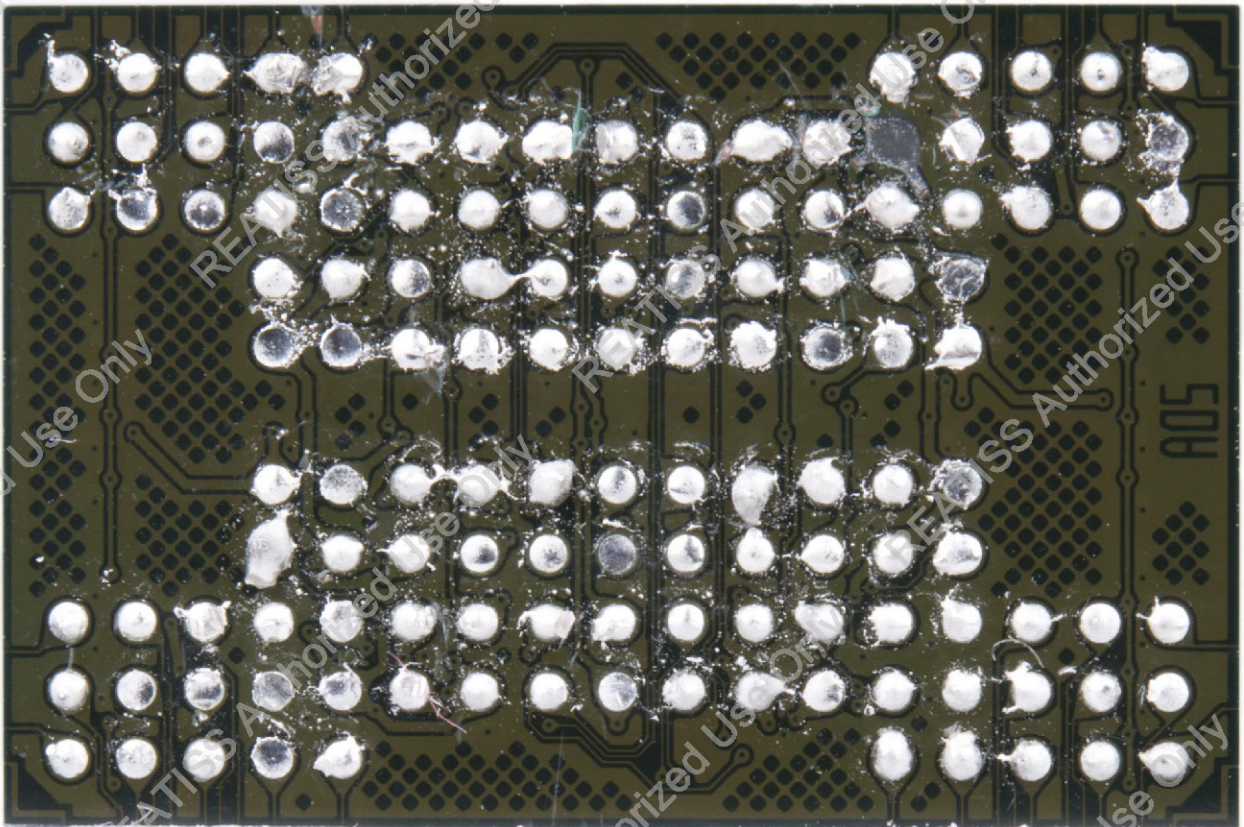


Figure 6. Bottom package view

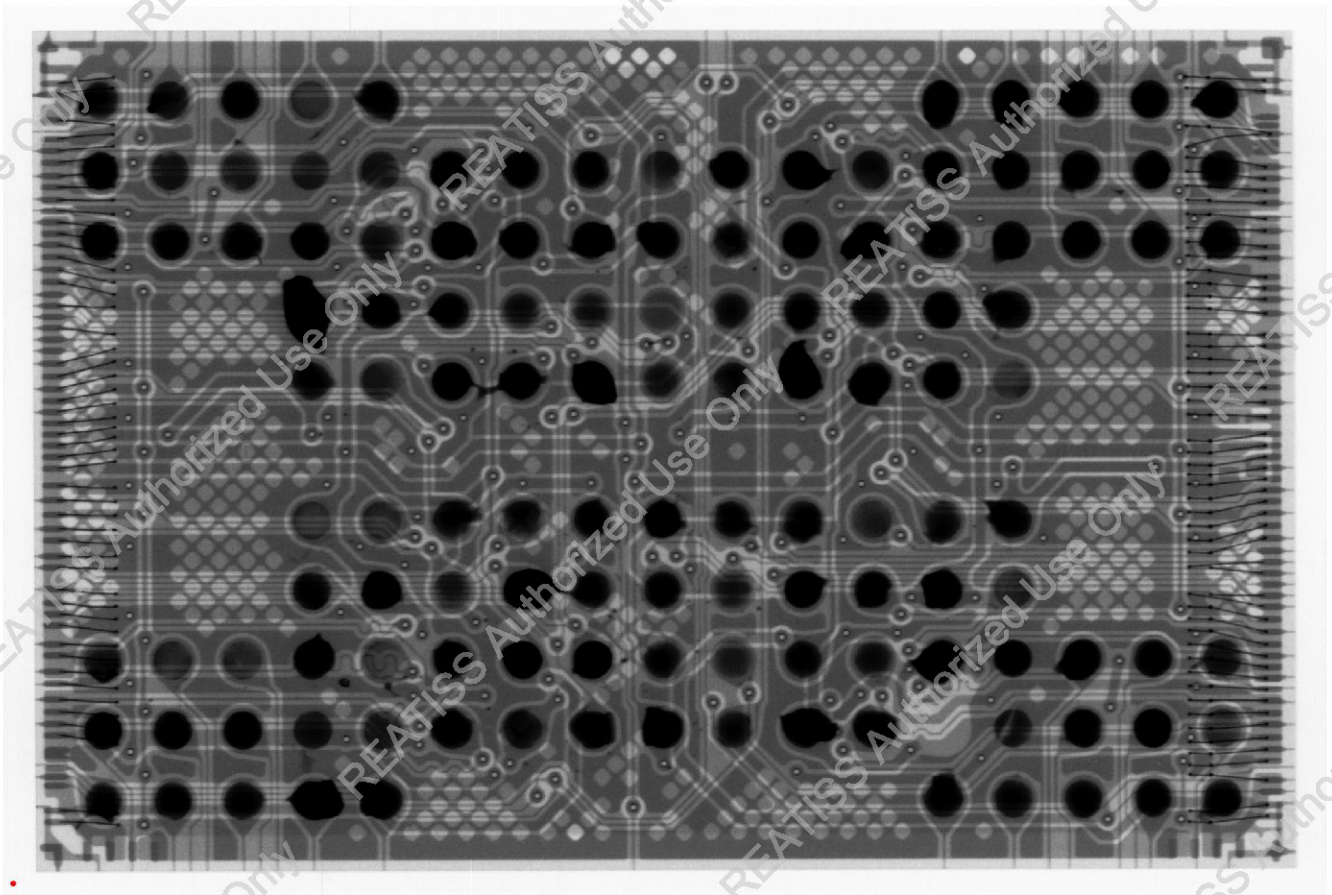


Figure 7. Top x-ray view of package

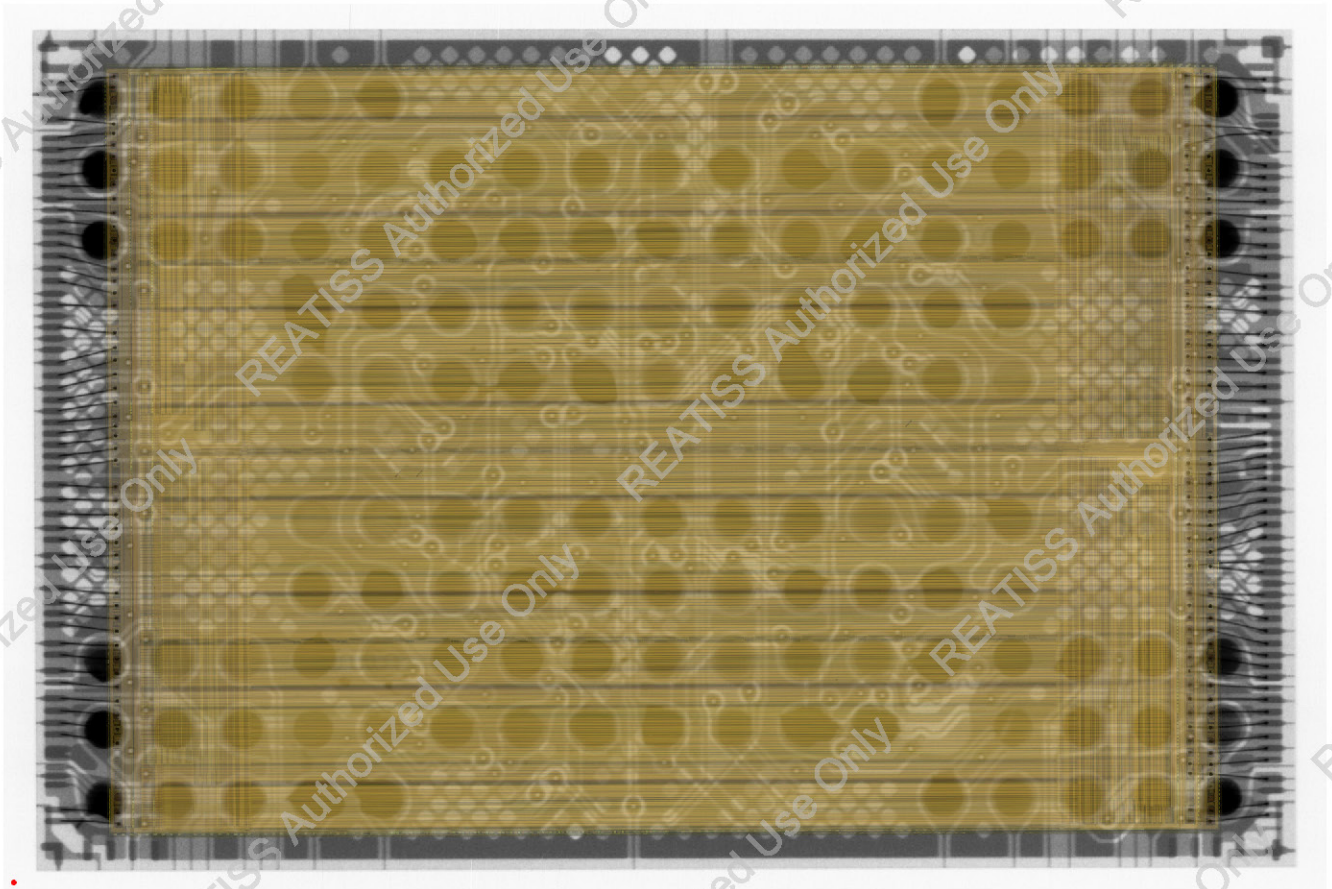


Figure 8. Top x-ray view of package combined with dice photos



Figure 9. Die photograph at the final metal level

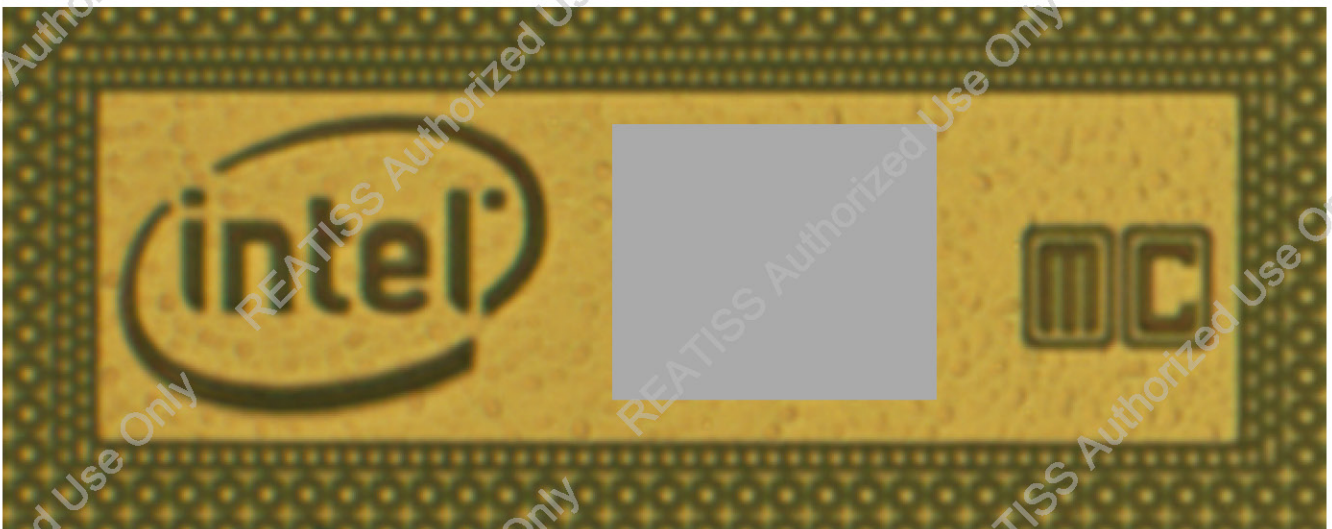


Figure 10. Die markings

Process

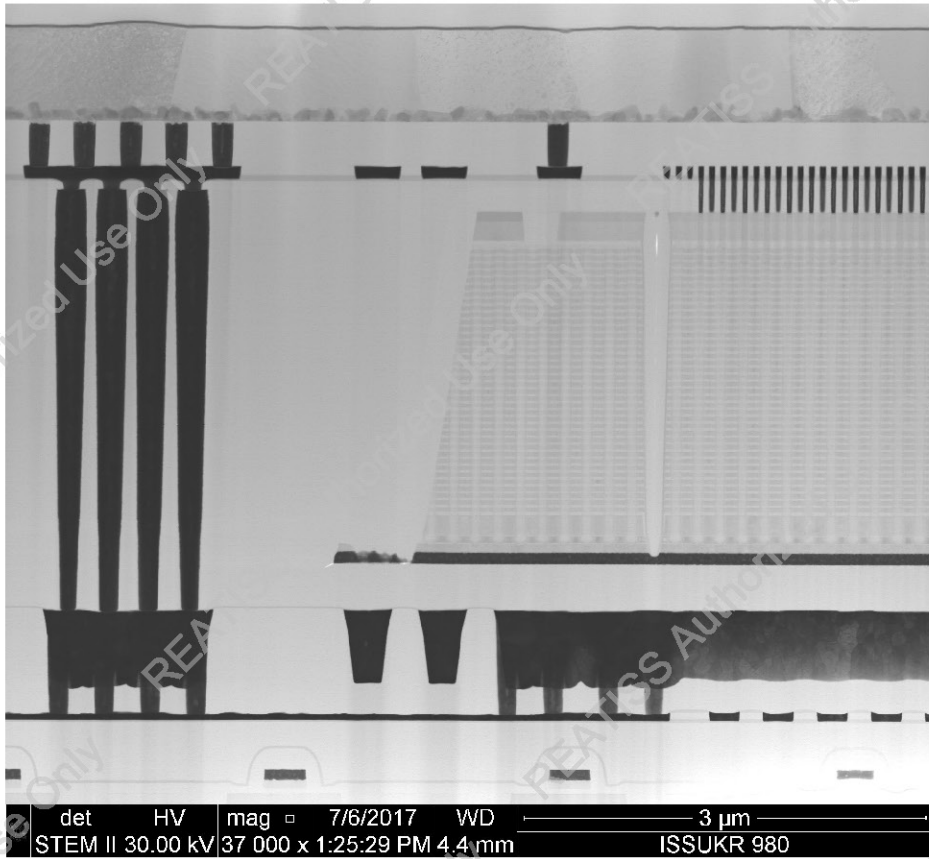


Figure 11. General structure

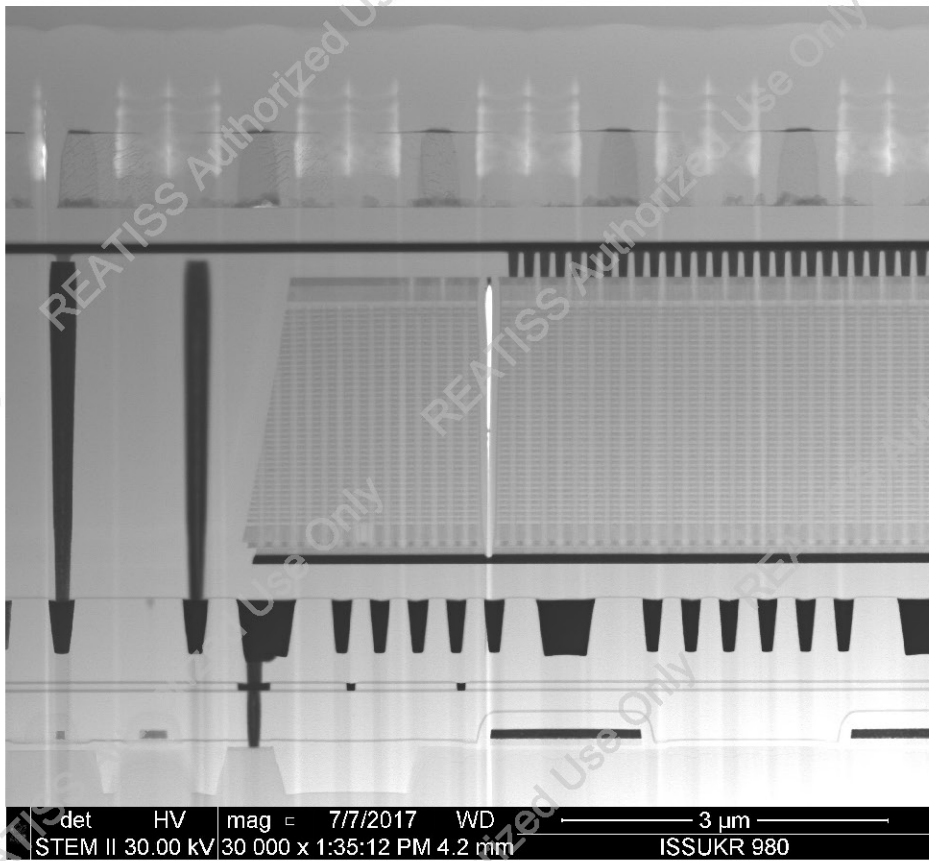


Figure 12. General structure



Figure 13. General structure

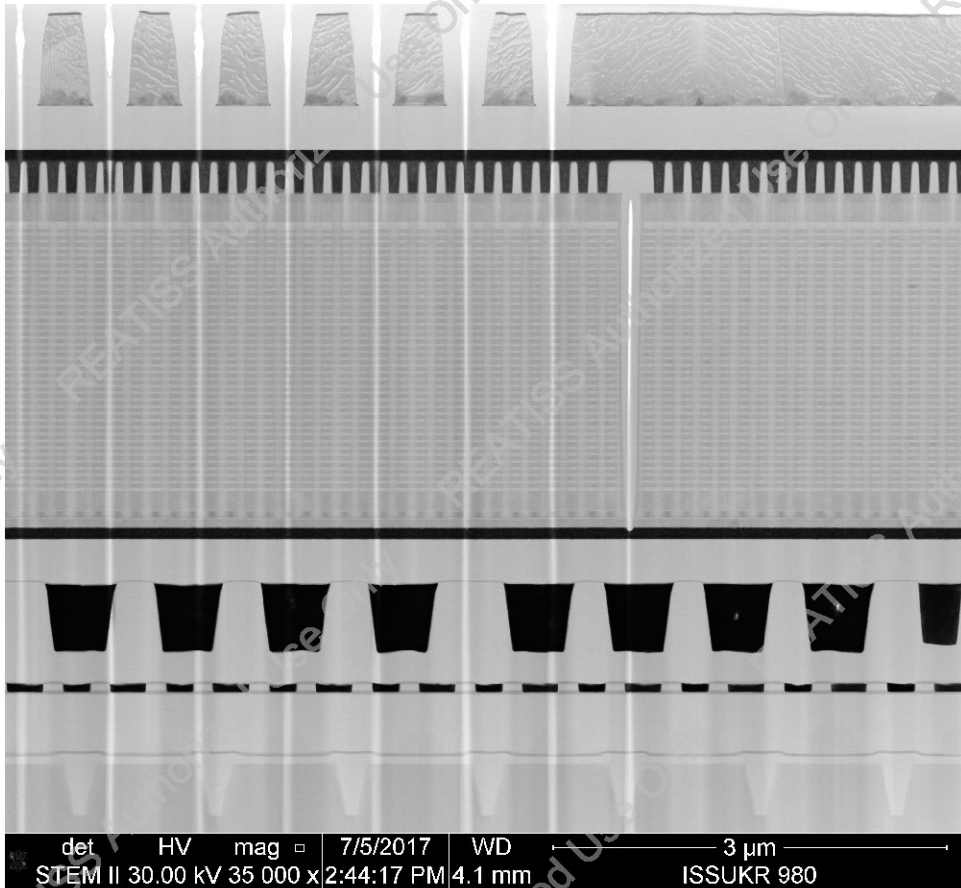


Figure 14. General structure

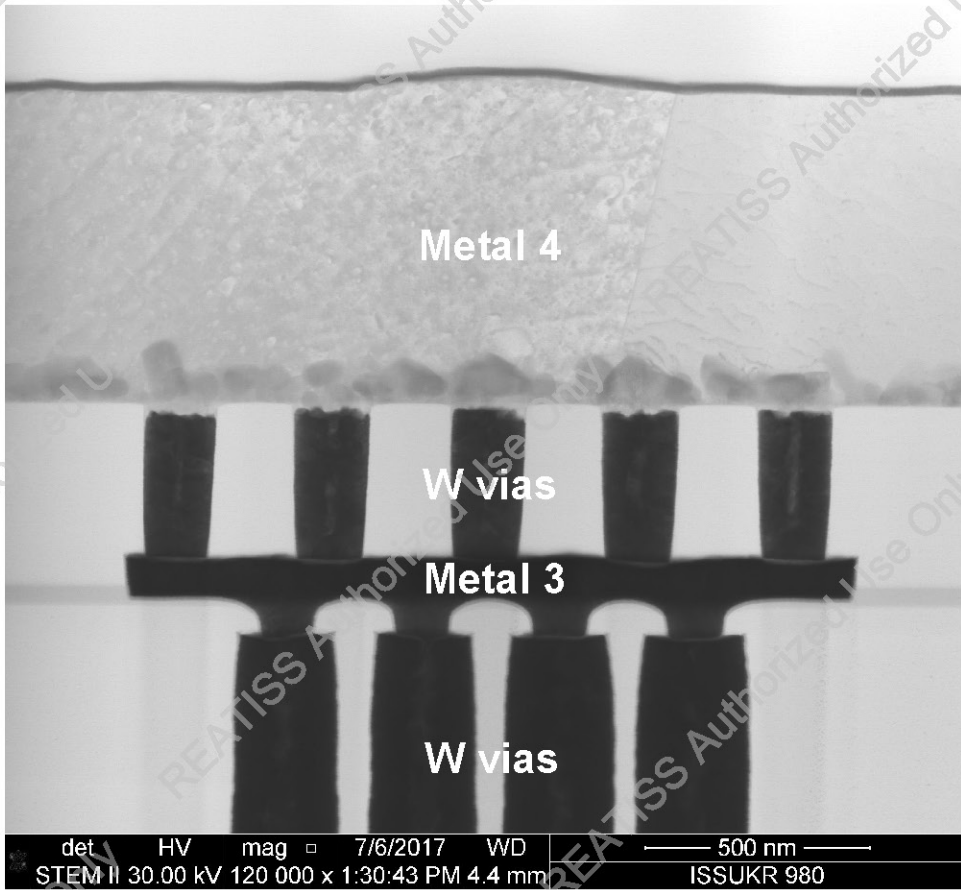


Figure 15. Al M4, W M3 lines, W vias

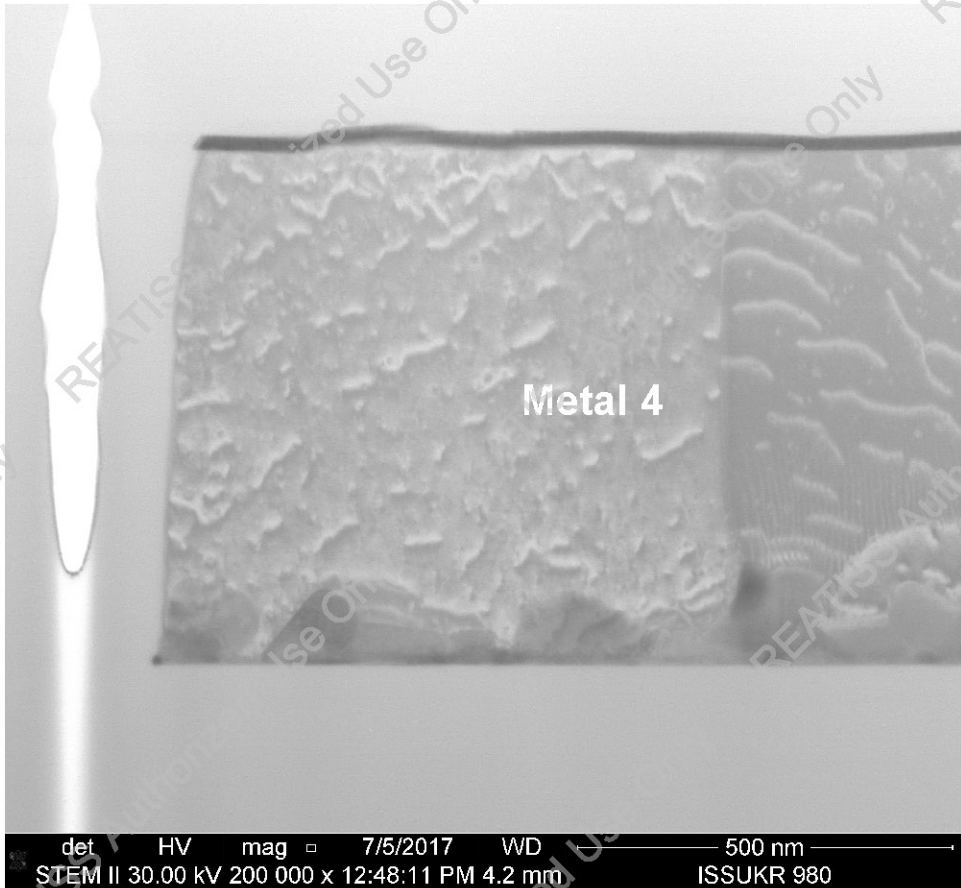


Figure 16. Al M4 line

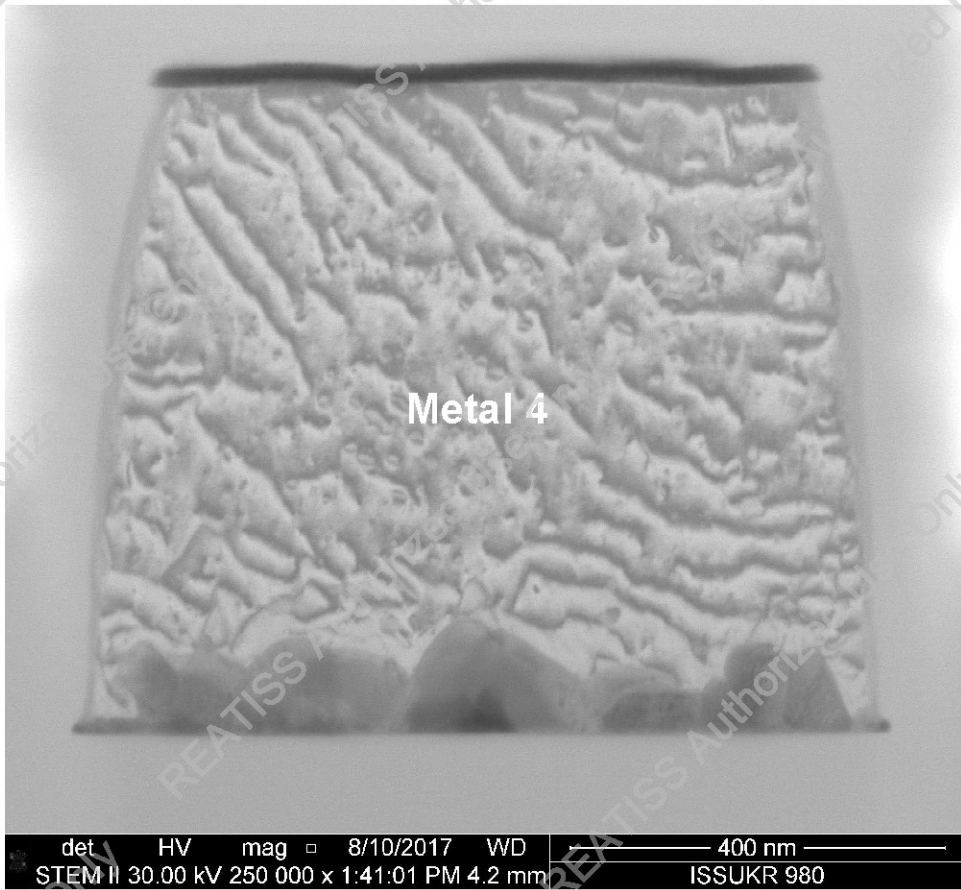


Figure 17. Al M4 line

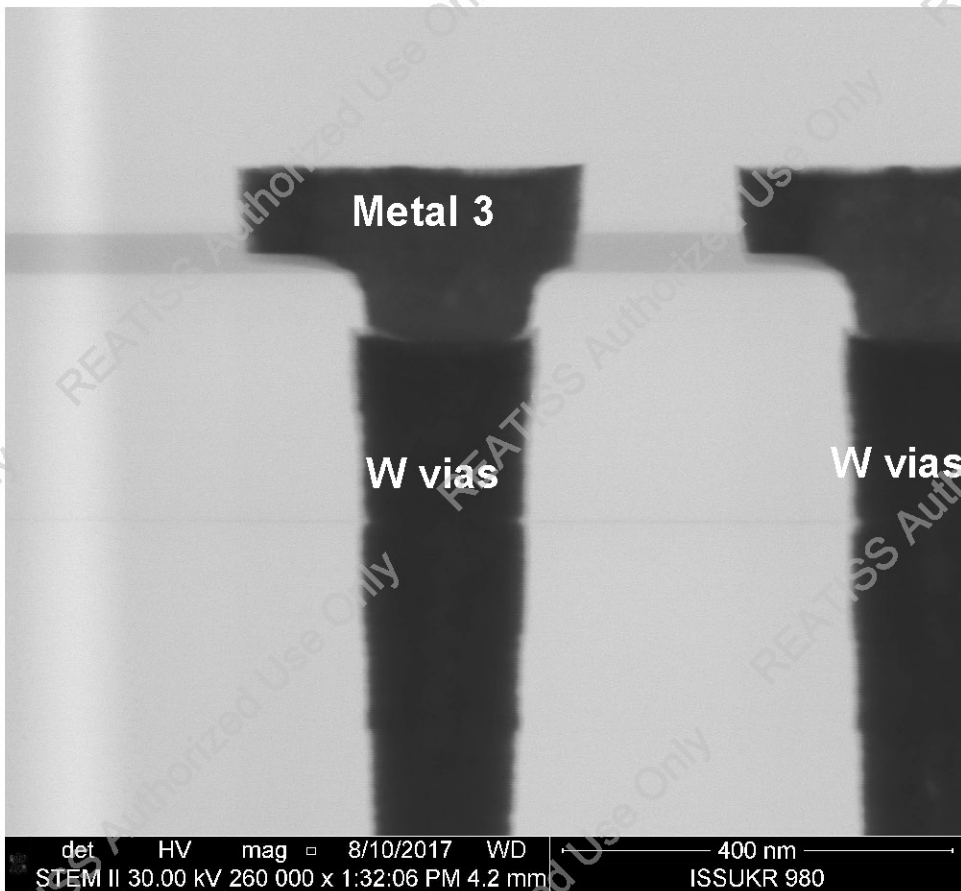


Figure 18. W M3 lines, W vias

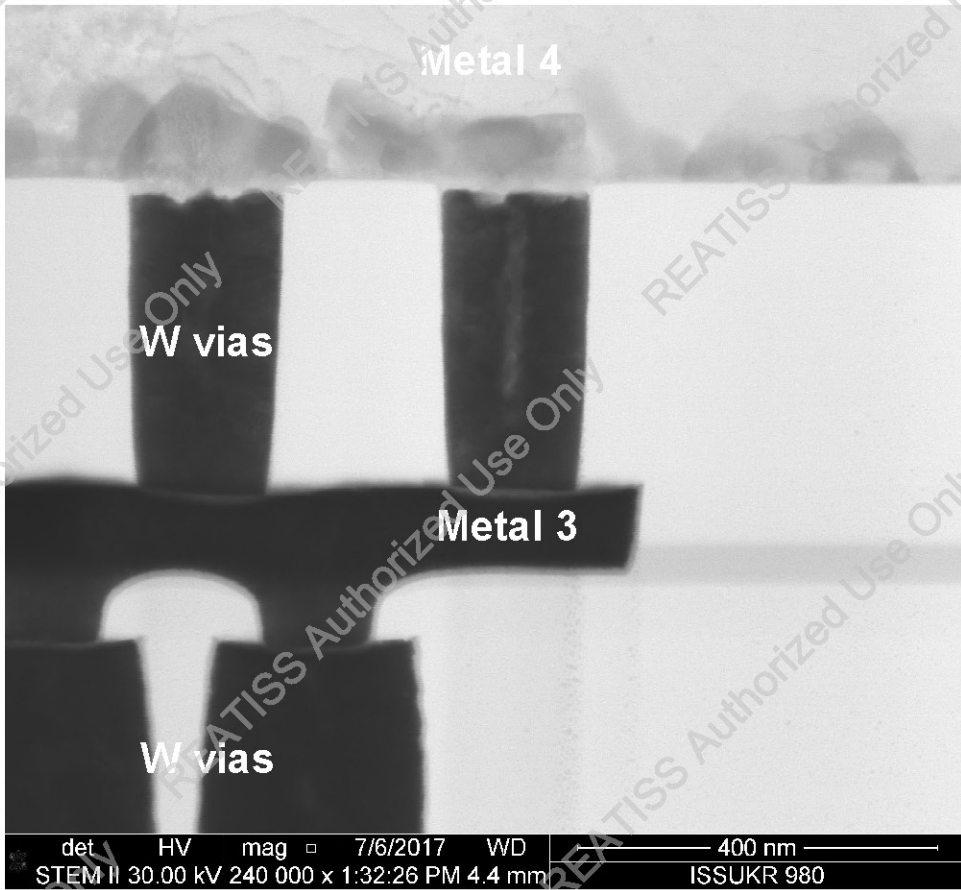


Figure 19. Al M4, W M3 lines, W vias

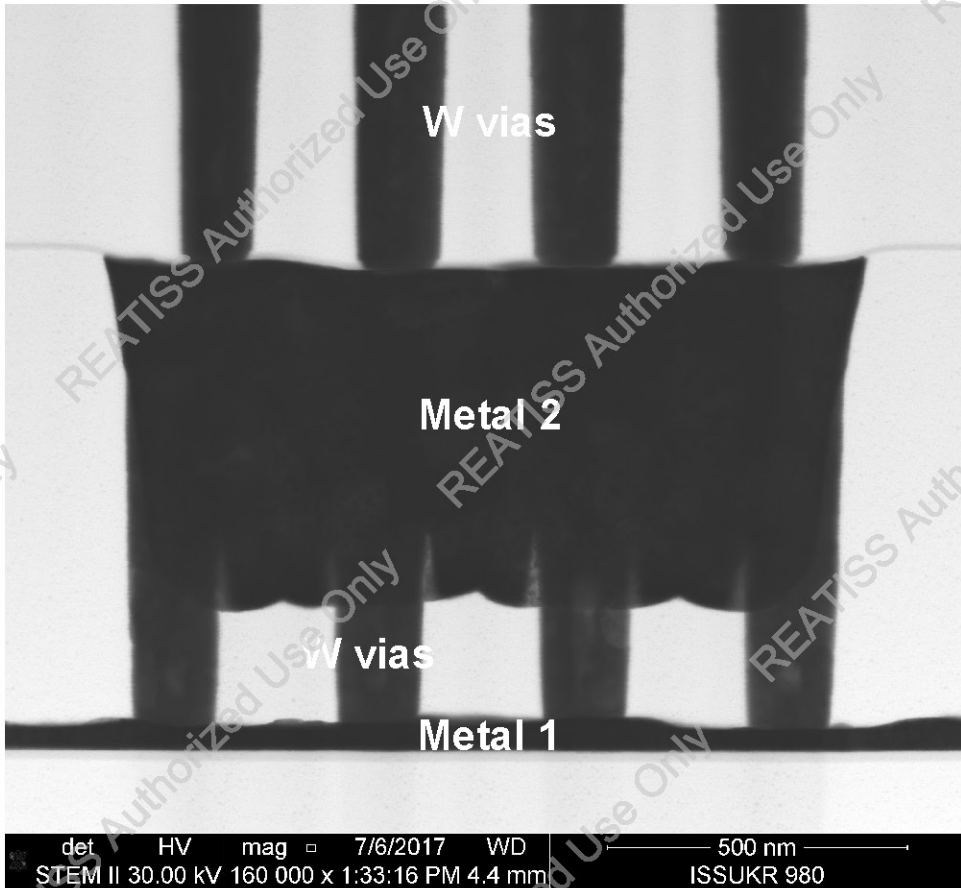


Figure 20. W M1, M2 lines, W vias

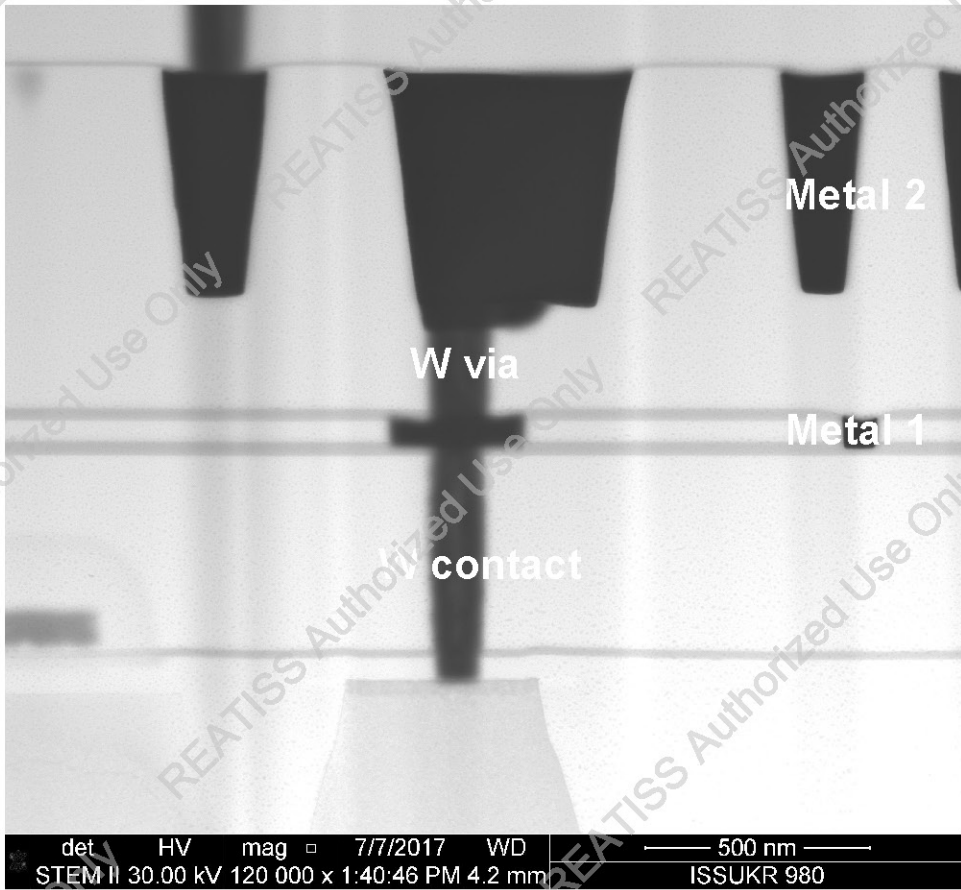


Figure 21. W M1, M2 lines, W via and contact

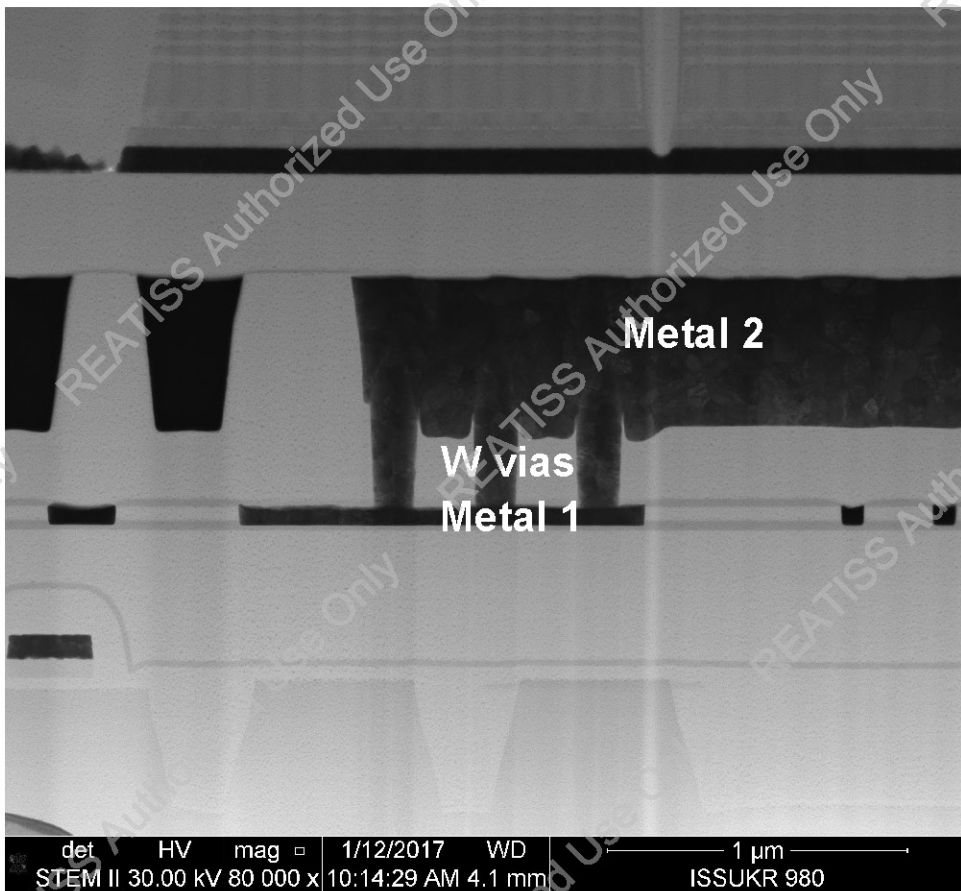


Figure 22. W M1, M2 lines, W vias

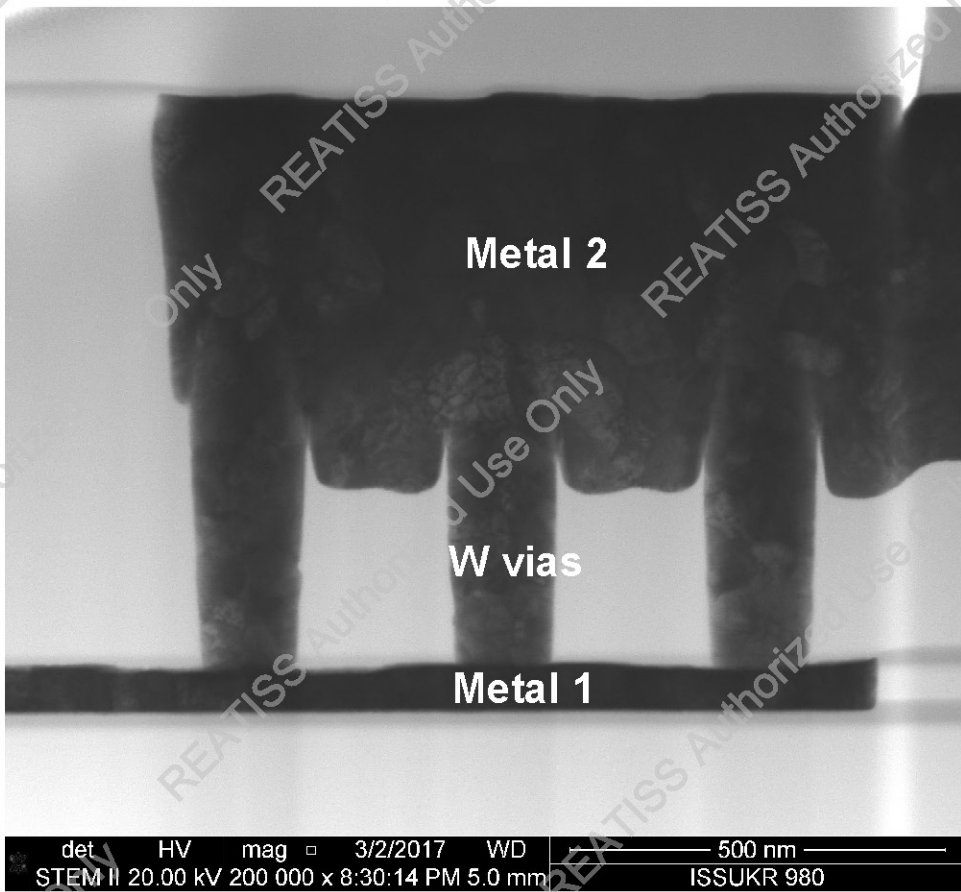


Figure 23. W M1, M2 lines, W vias

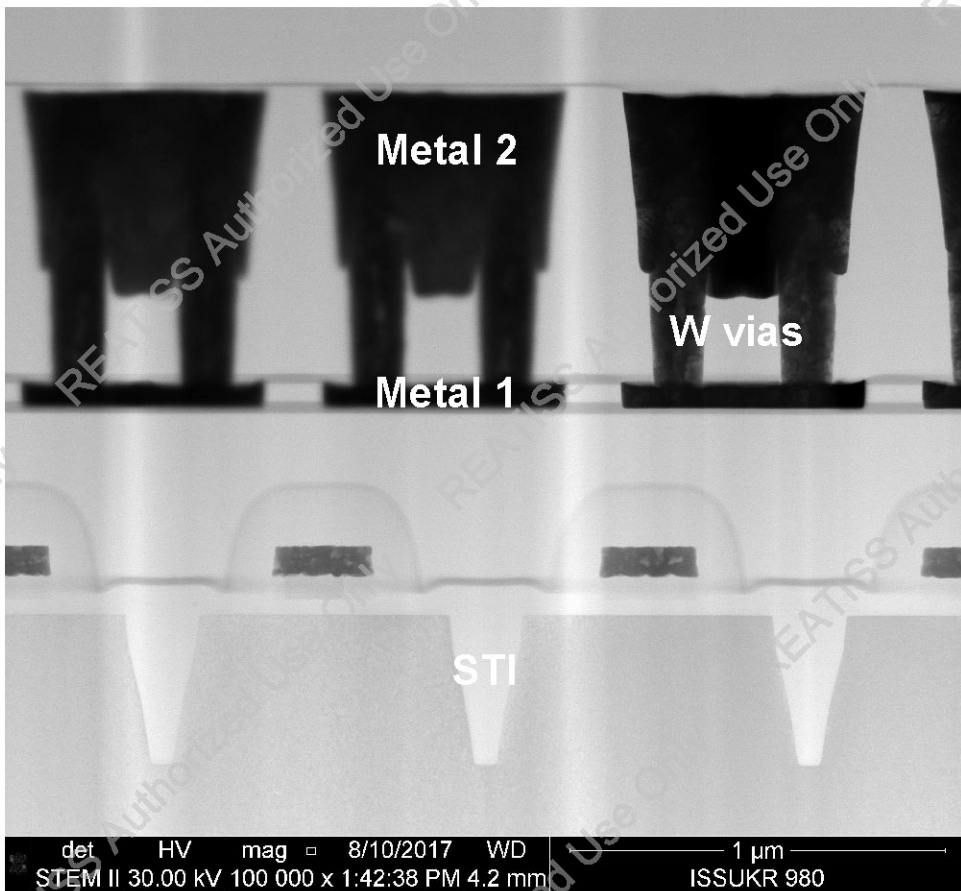


Figure 24. W M1, M2 lines, W vias, STI

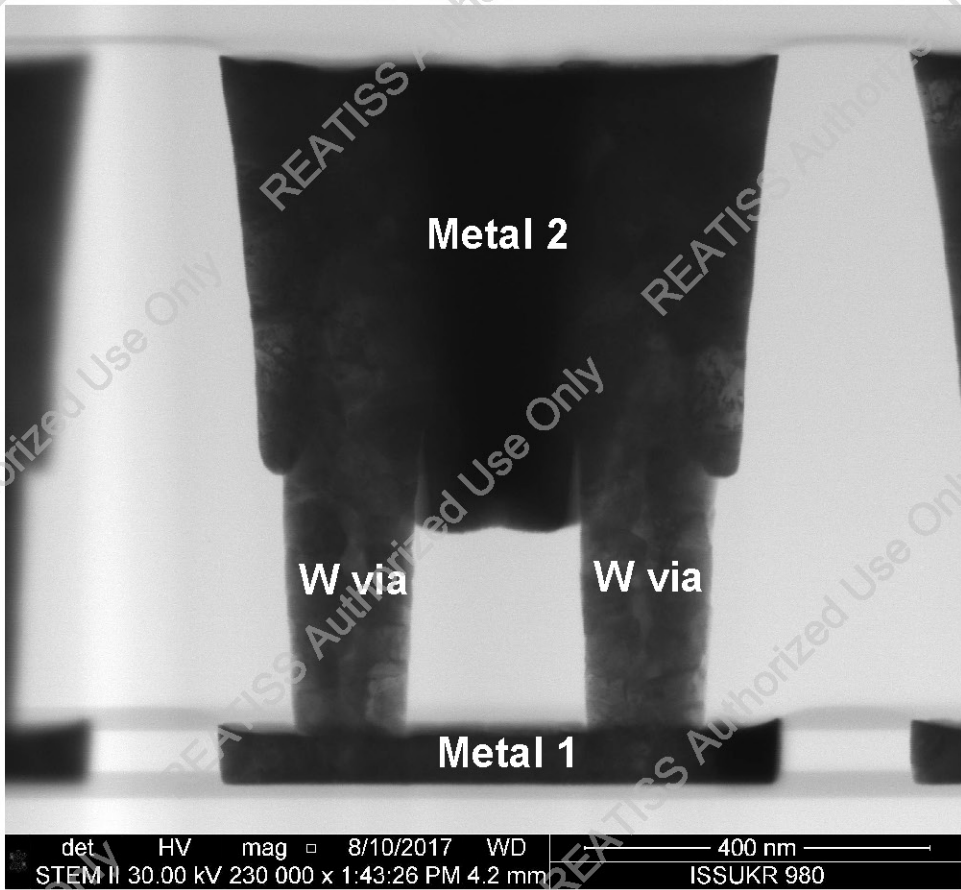


Figure 25. W M1, M2 lines, W vias

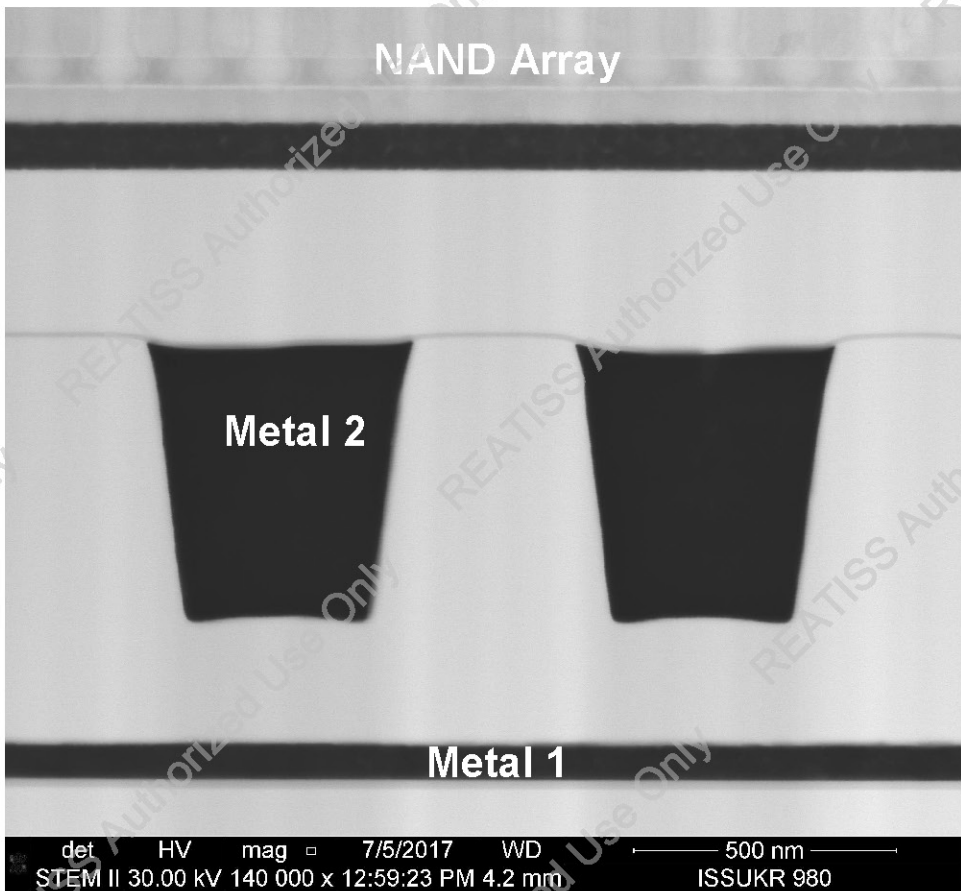


Figure 26. W M1, M2 lines

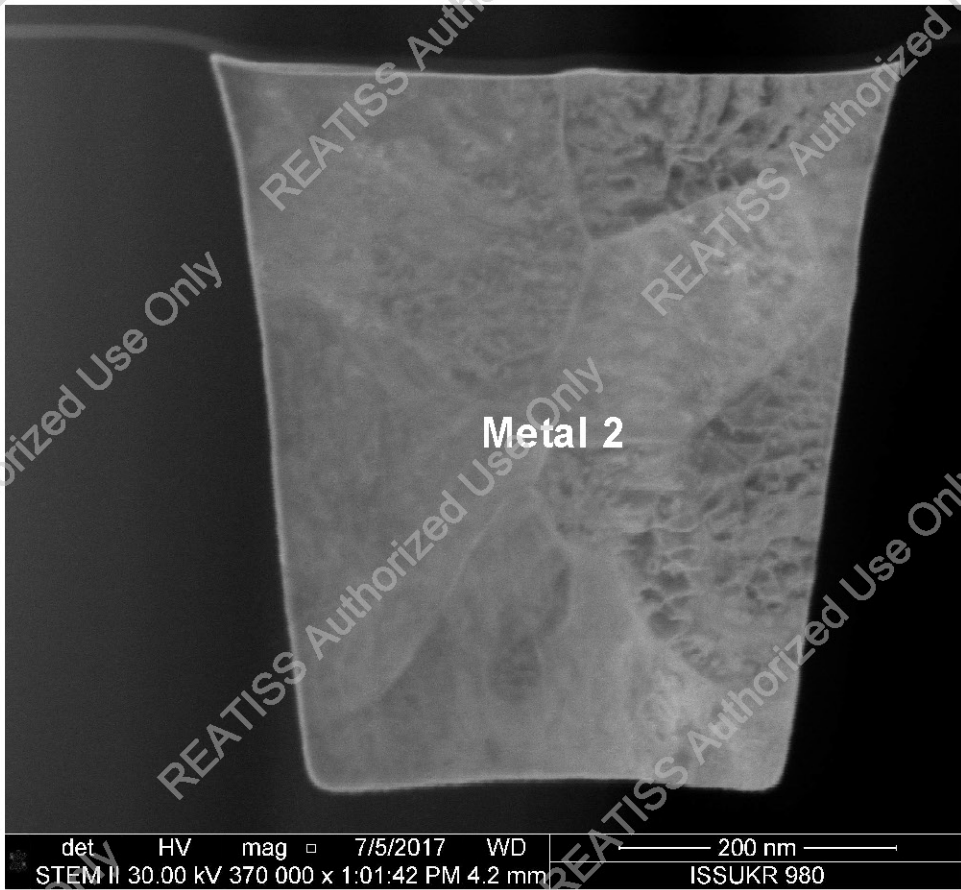


Figure 27. W M2 line

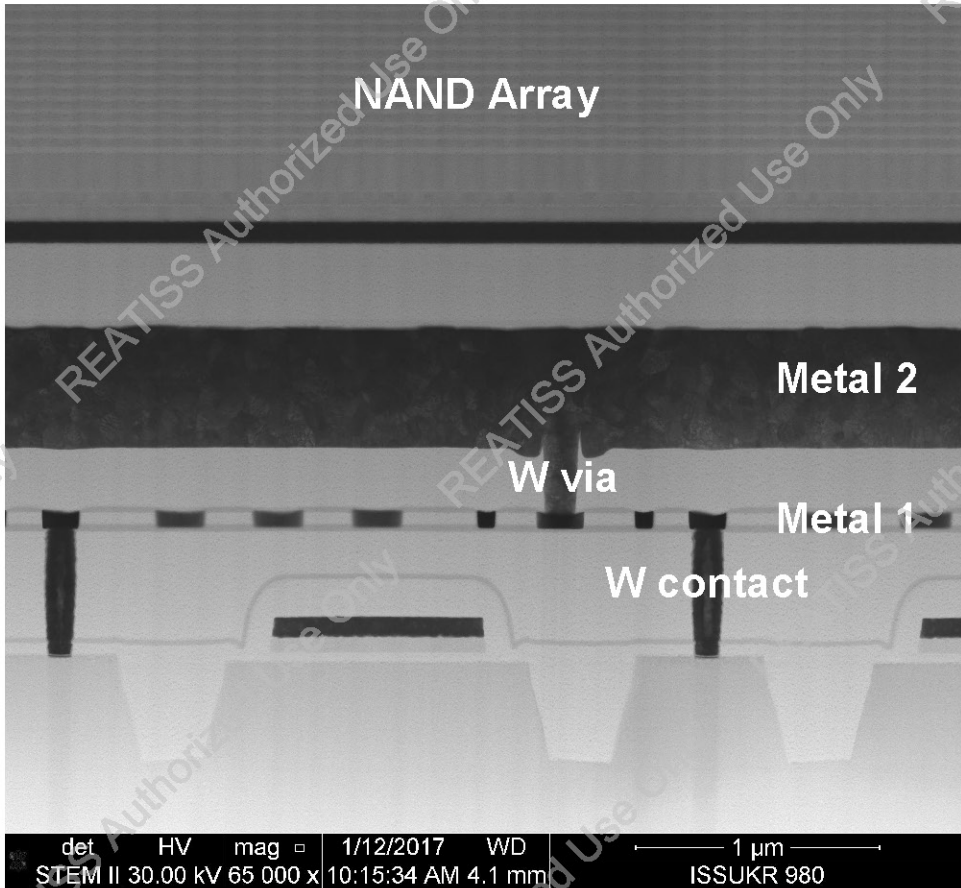


Figure 28. W M1, M2 lines, W via and contact

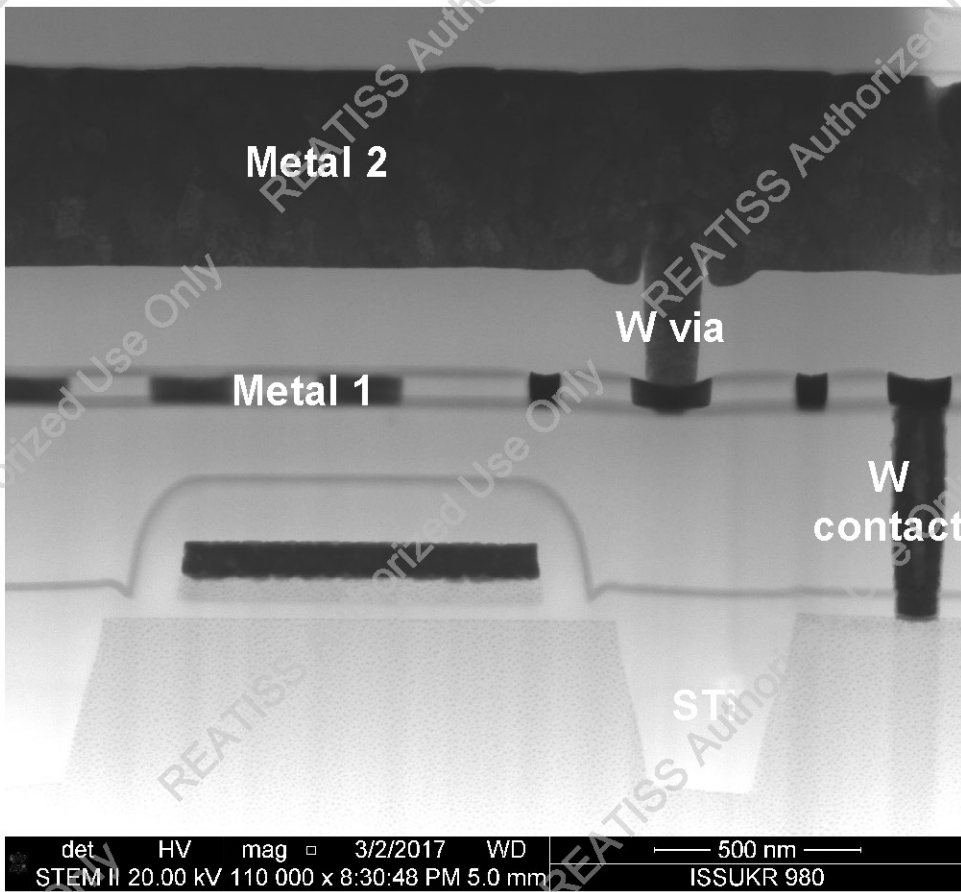


Figure 29. W M1, M2 lines, W via and contact, MOS gate, STI

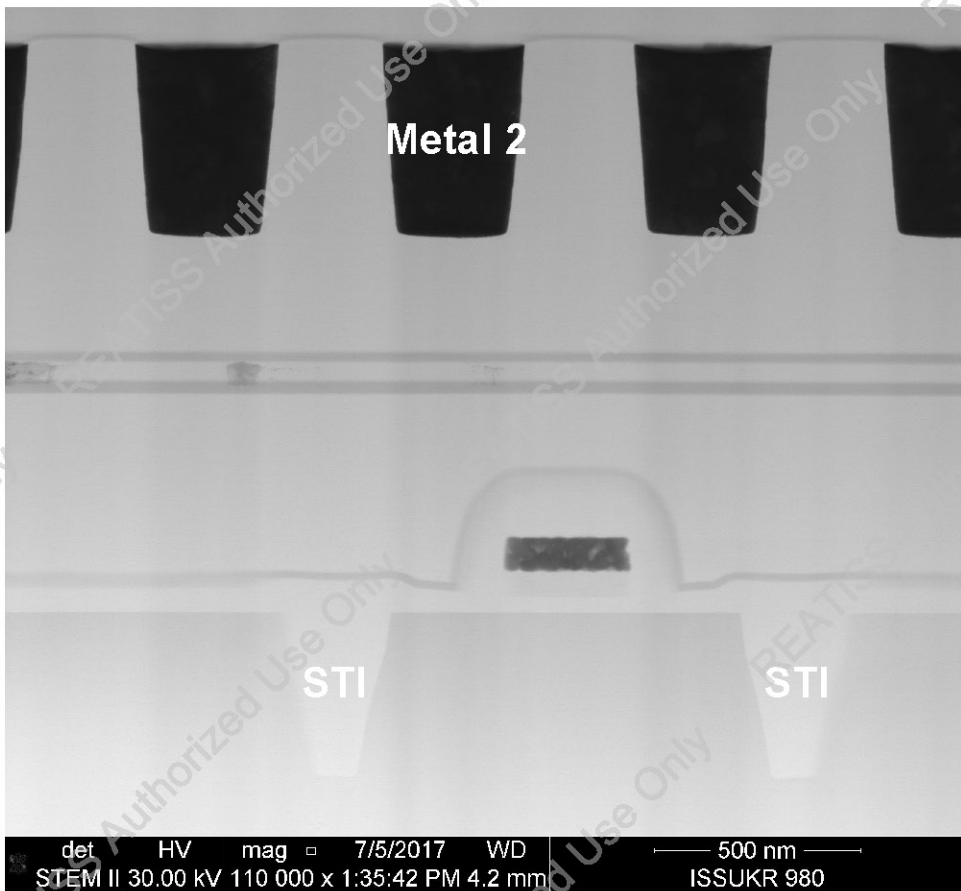


Figure 30. W M2 lines, MOS gate, STI

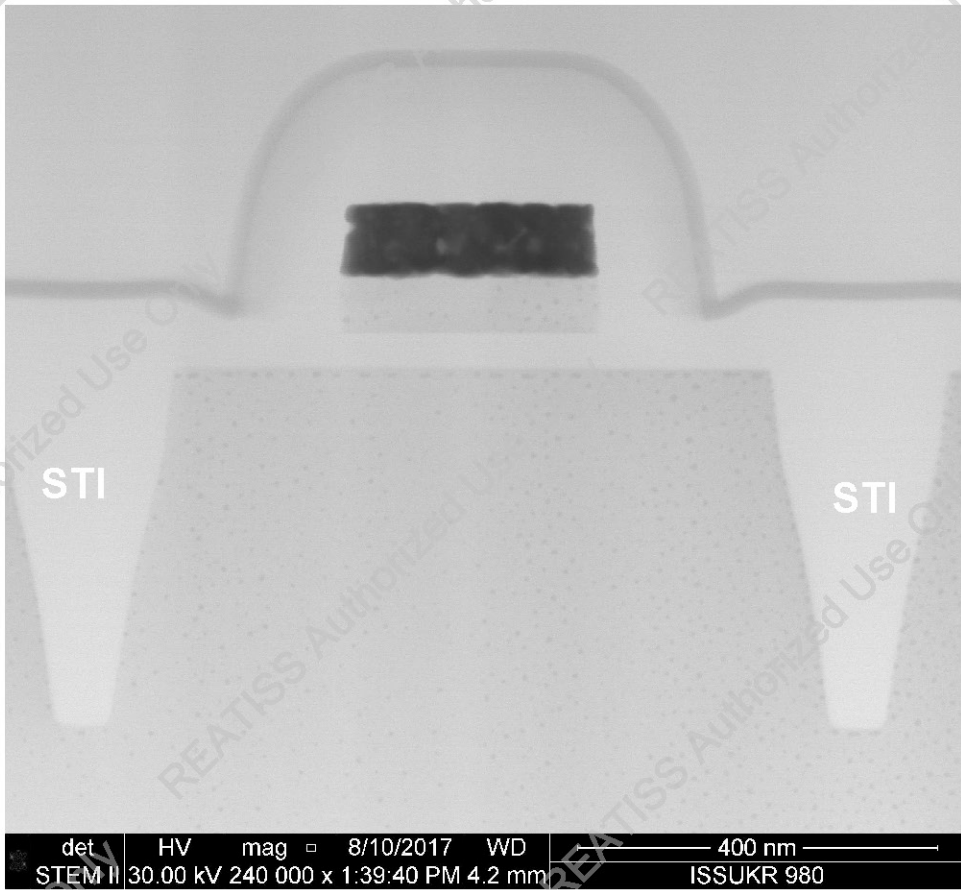


Figure 31. MOS gate, STI

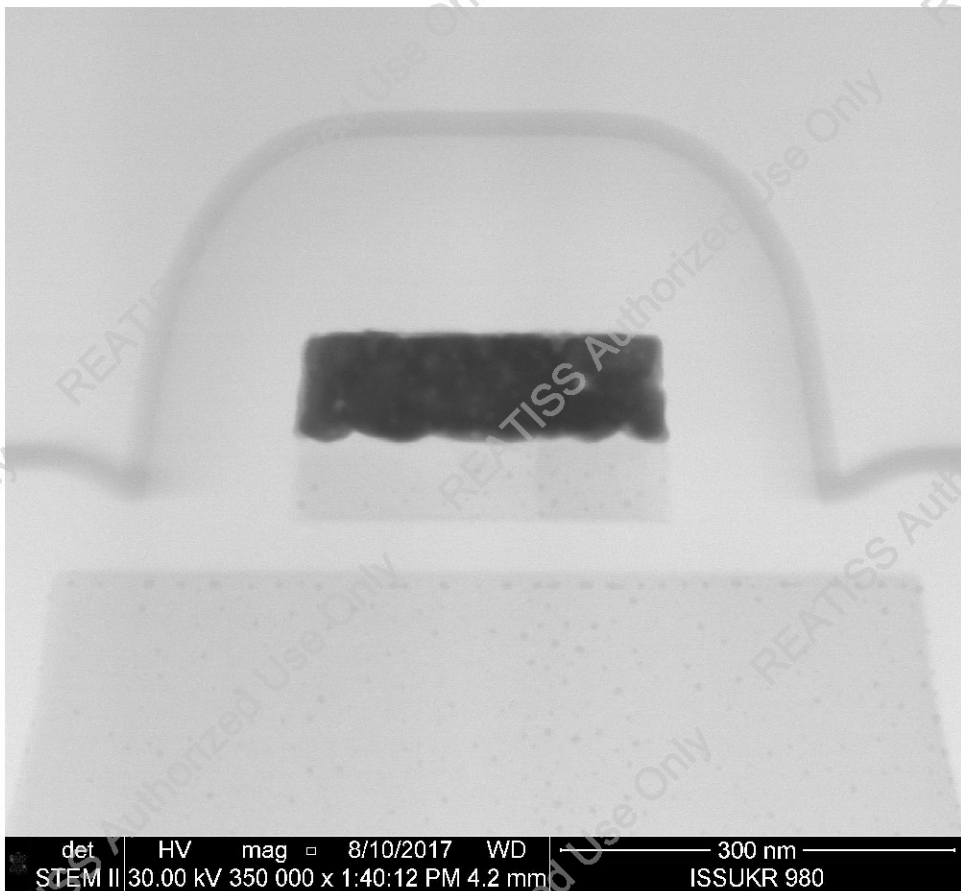


Figure 32. MOS gate



Figure 33. MOS gate

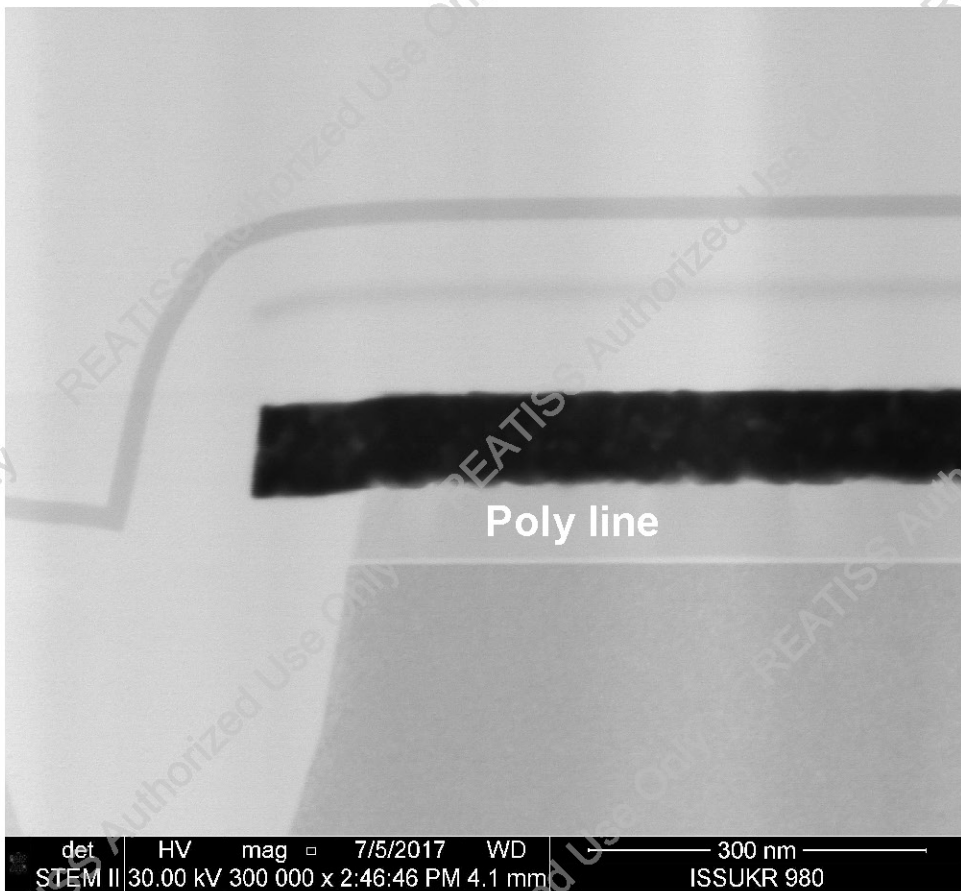


Figure 34. Poly line edge

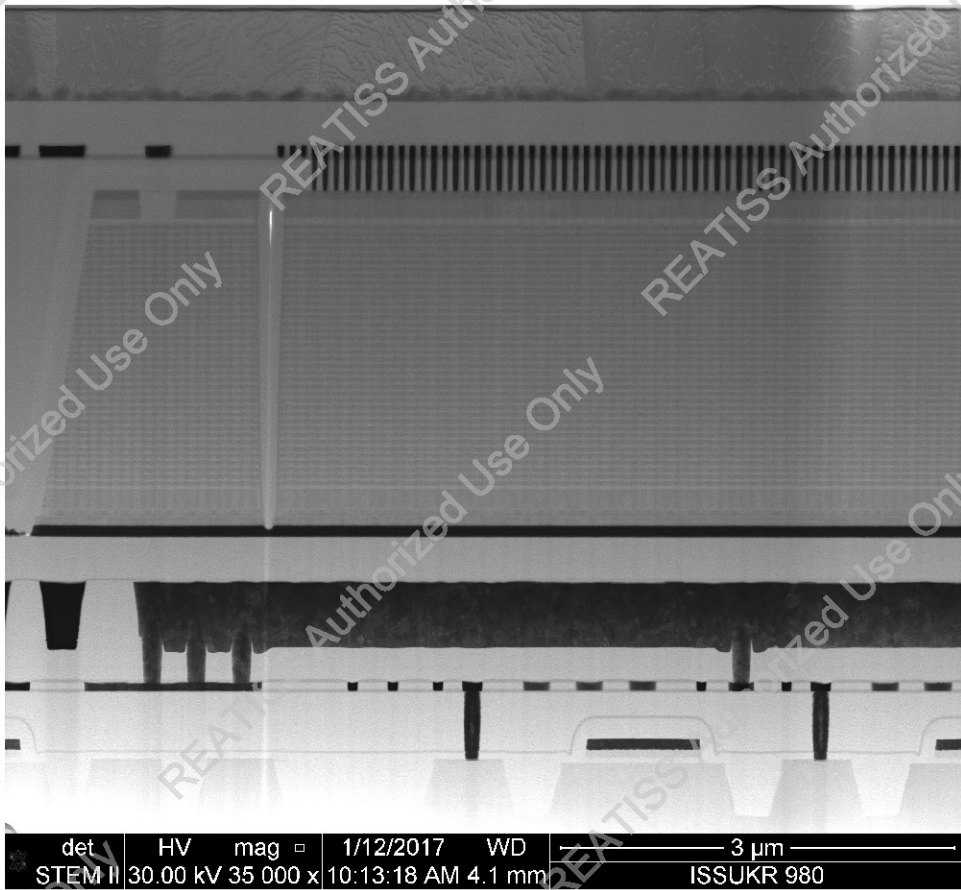


Figure 35. NAND array across bitlines

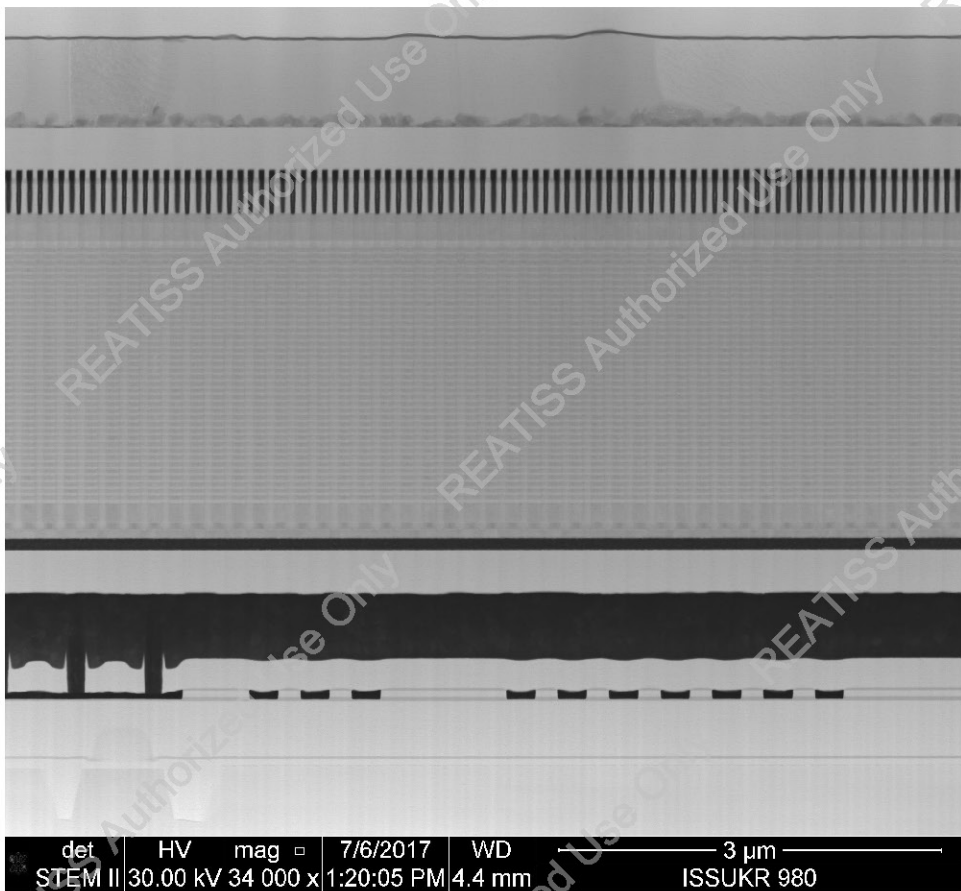


Figure 36. NAND array across bitlines

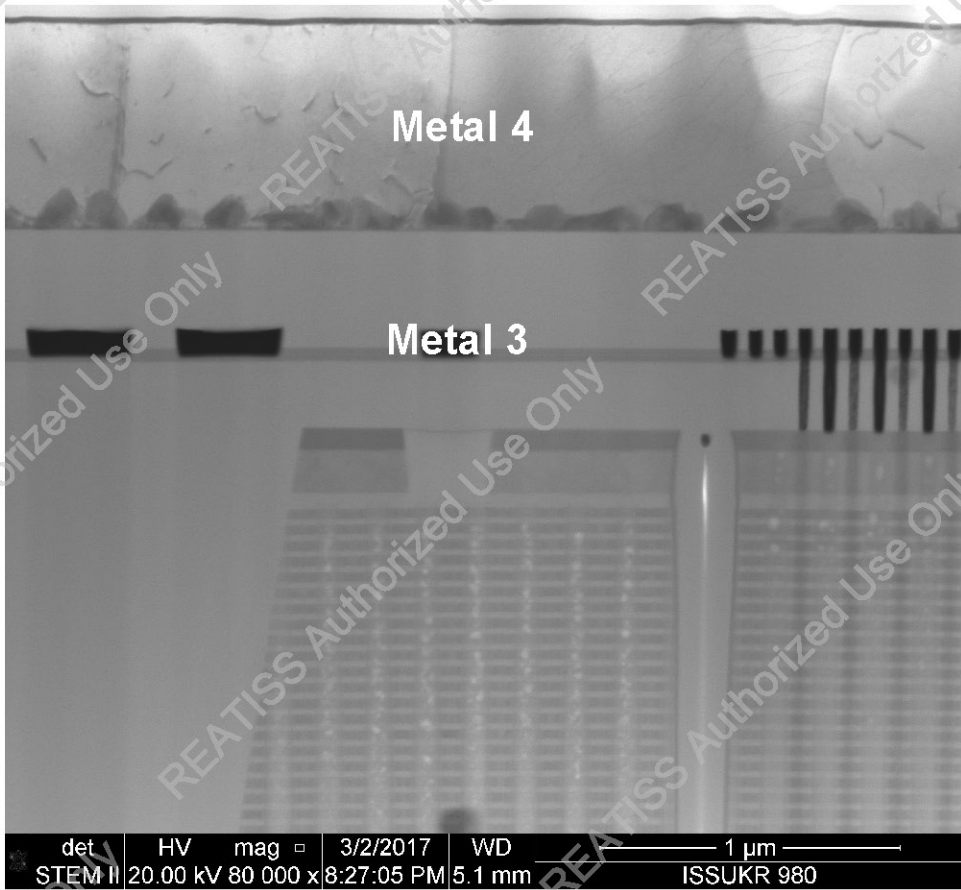


Figure 37. NAND array edge across bitlines

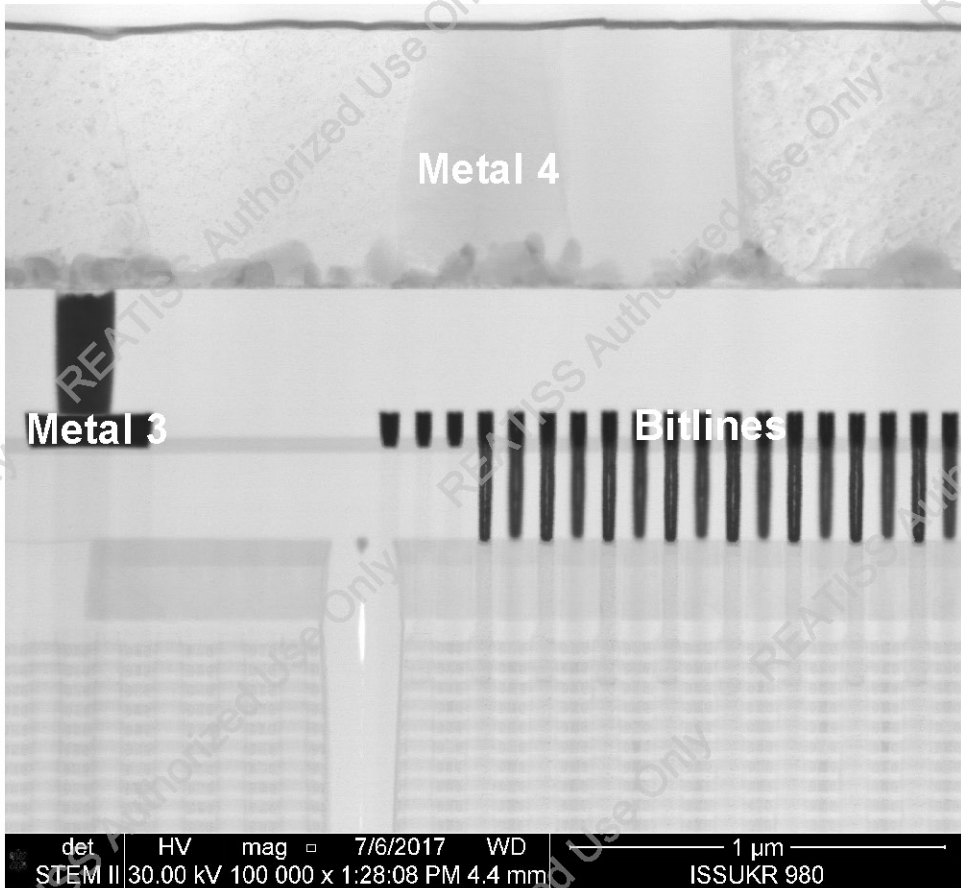


Figure 38. NAND array edge across bitlines

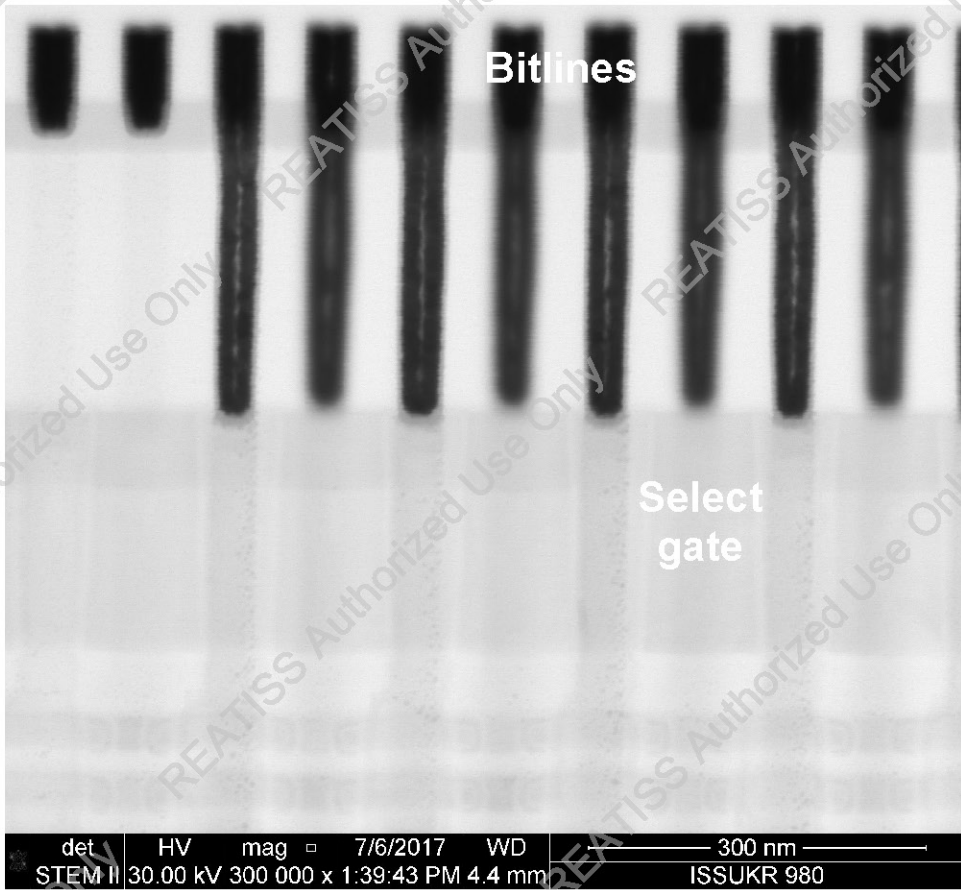


Figure 39. NAND array bitlines connection

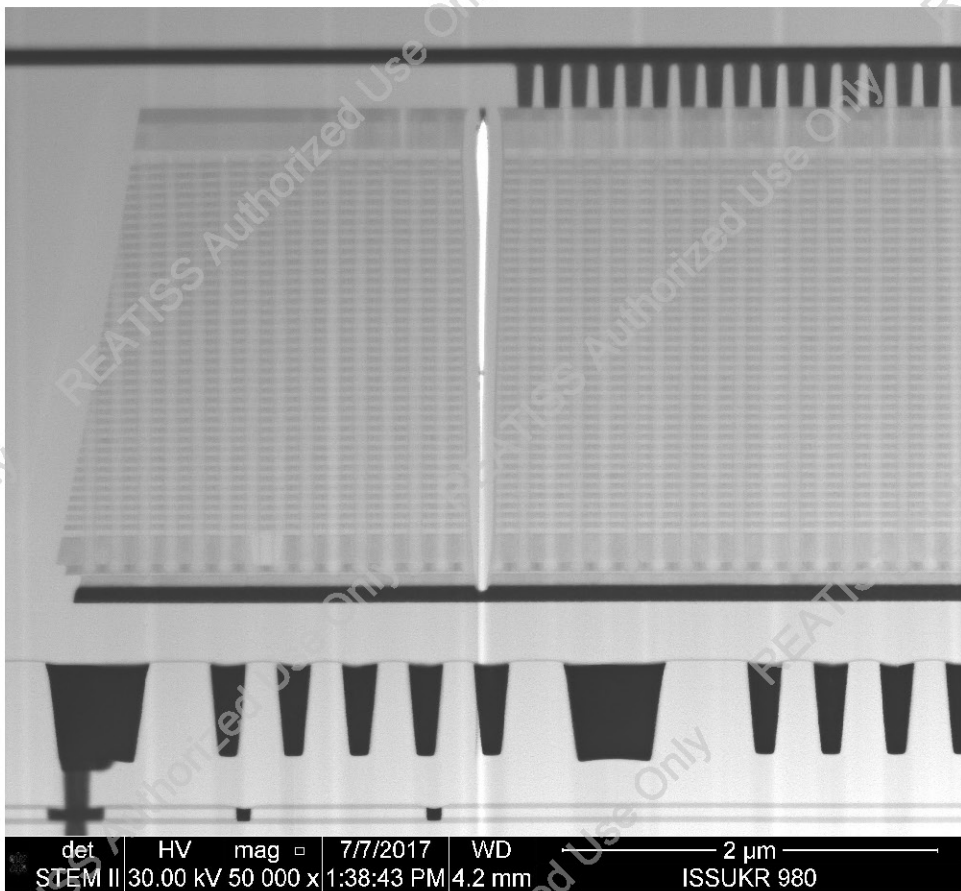


Figure 40. NAND array edge along bitlines

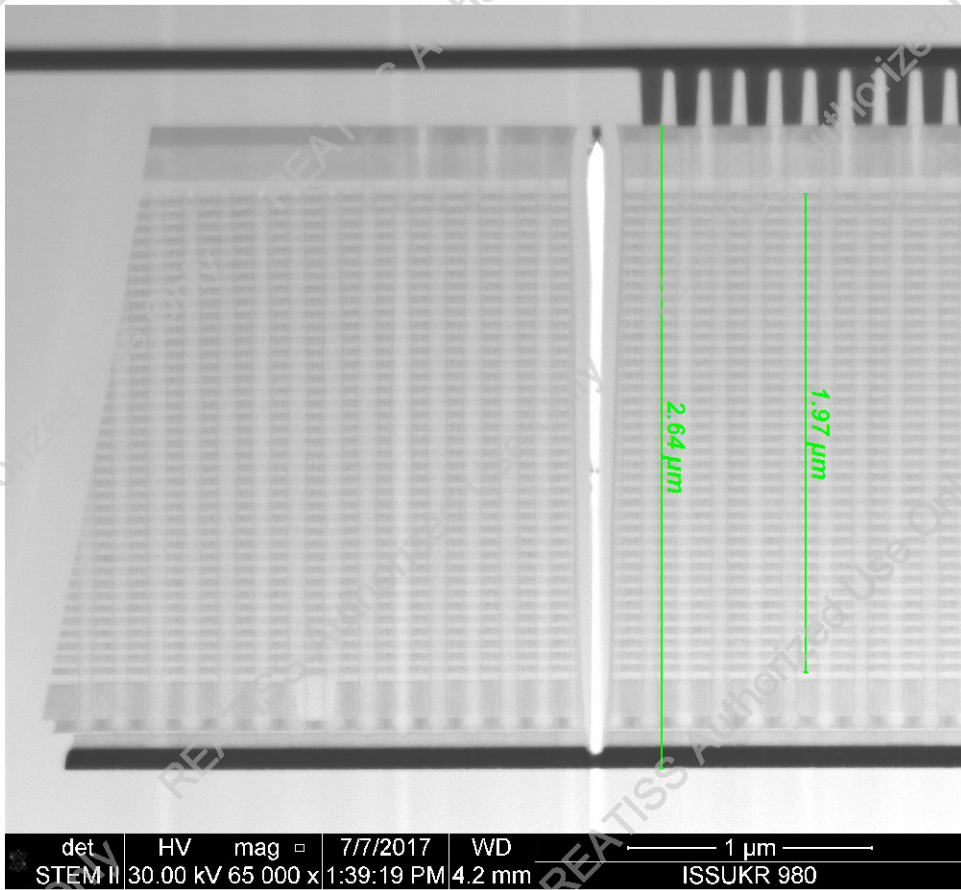


Figure 41. NAND array edge along bitlines

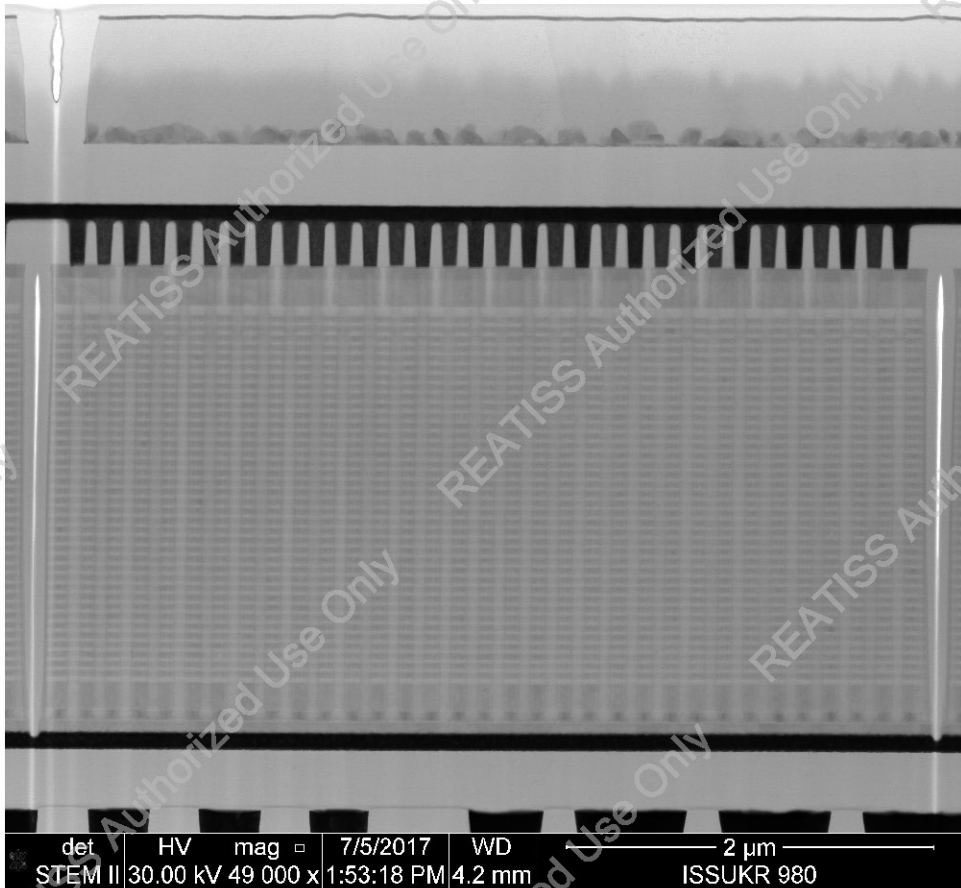


Figure 42. NAND array along bitlines

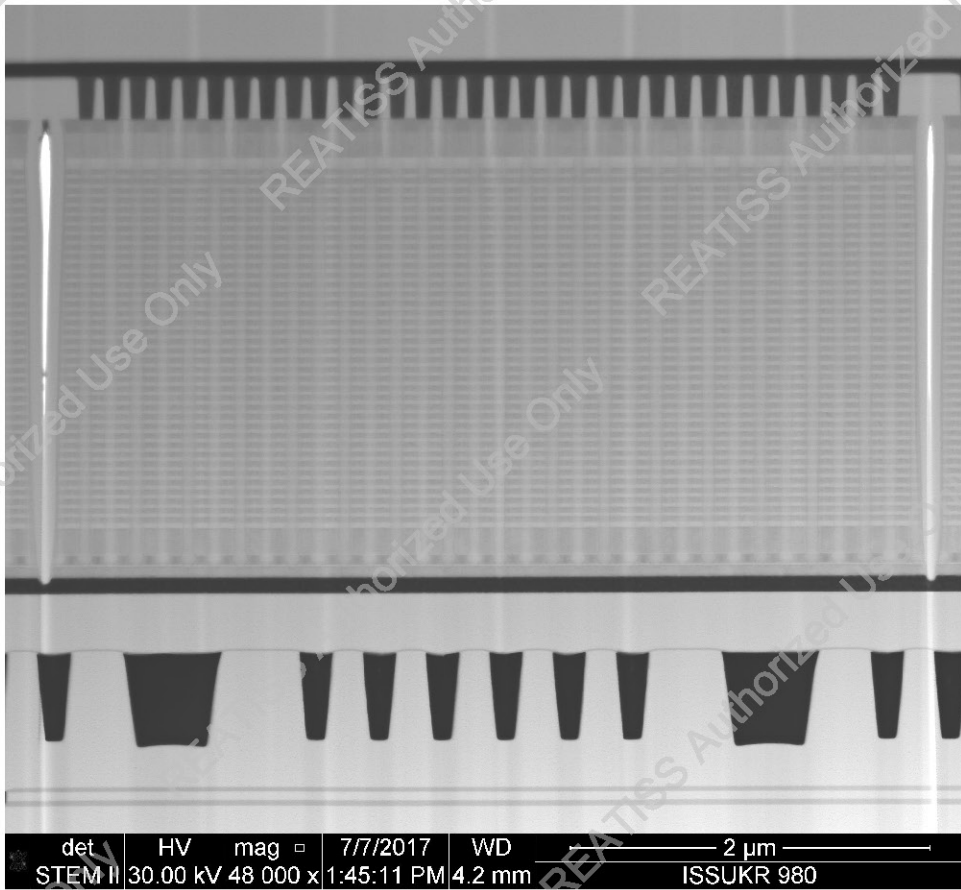


Figure 43. NAND array along bitlines

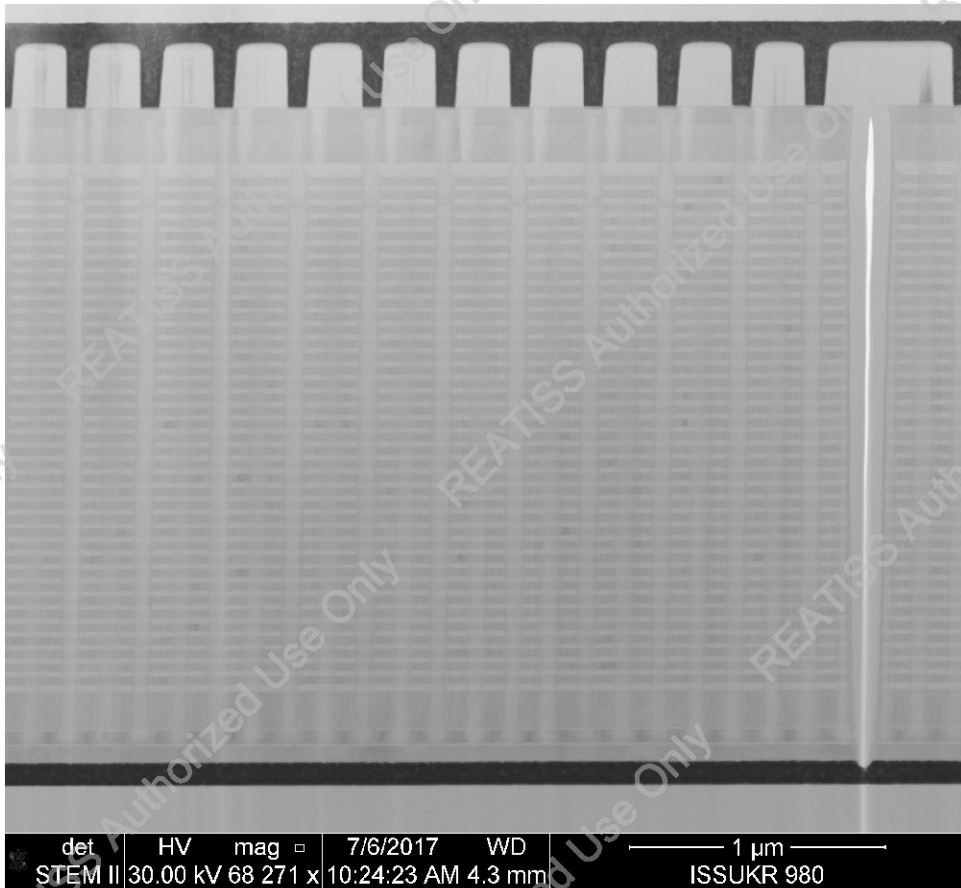


Figure 44. NAND array along bitlines

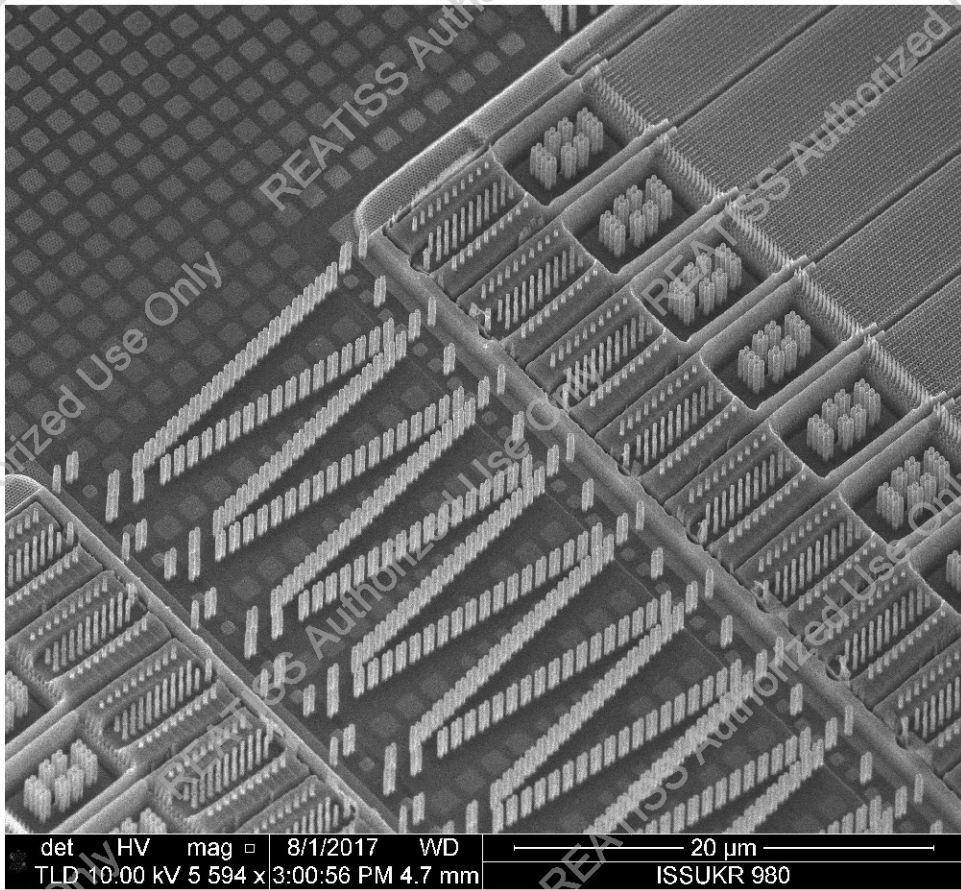


Figure 45. Top-down tilted view of NAND array edges

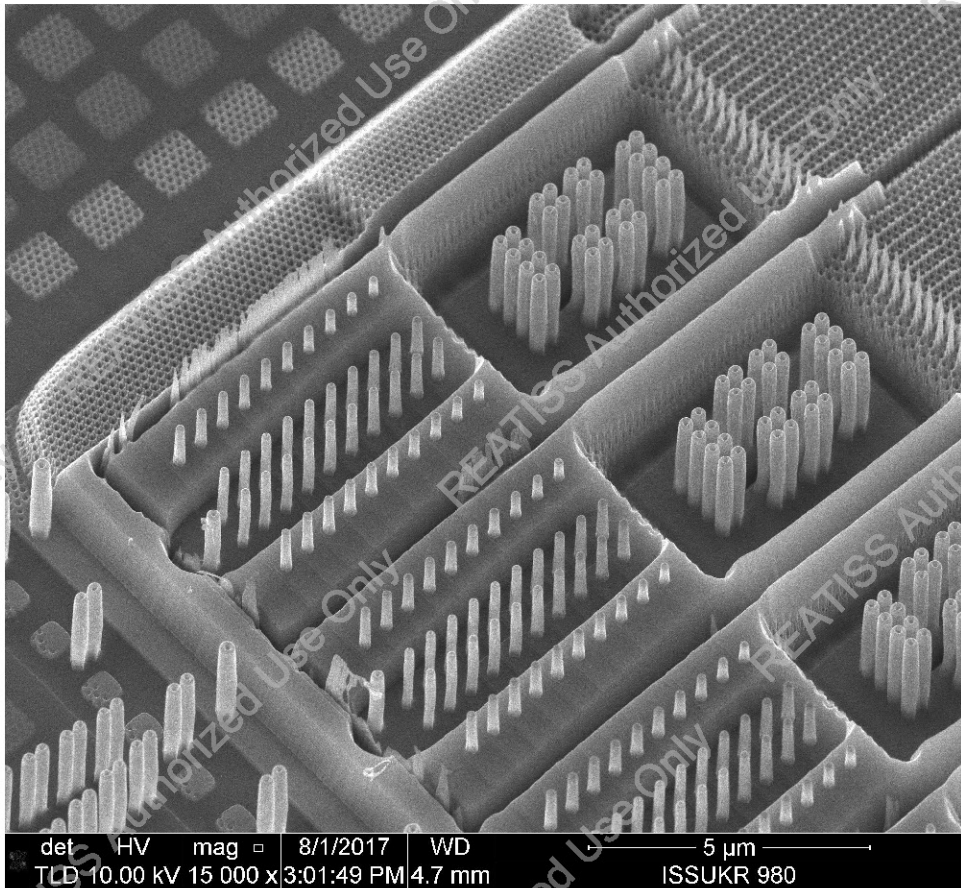


Figure 46. Top-down tilted view of NAND array edge

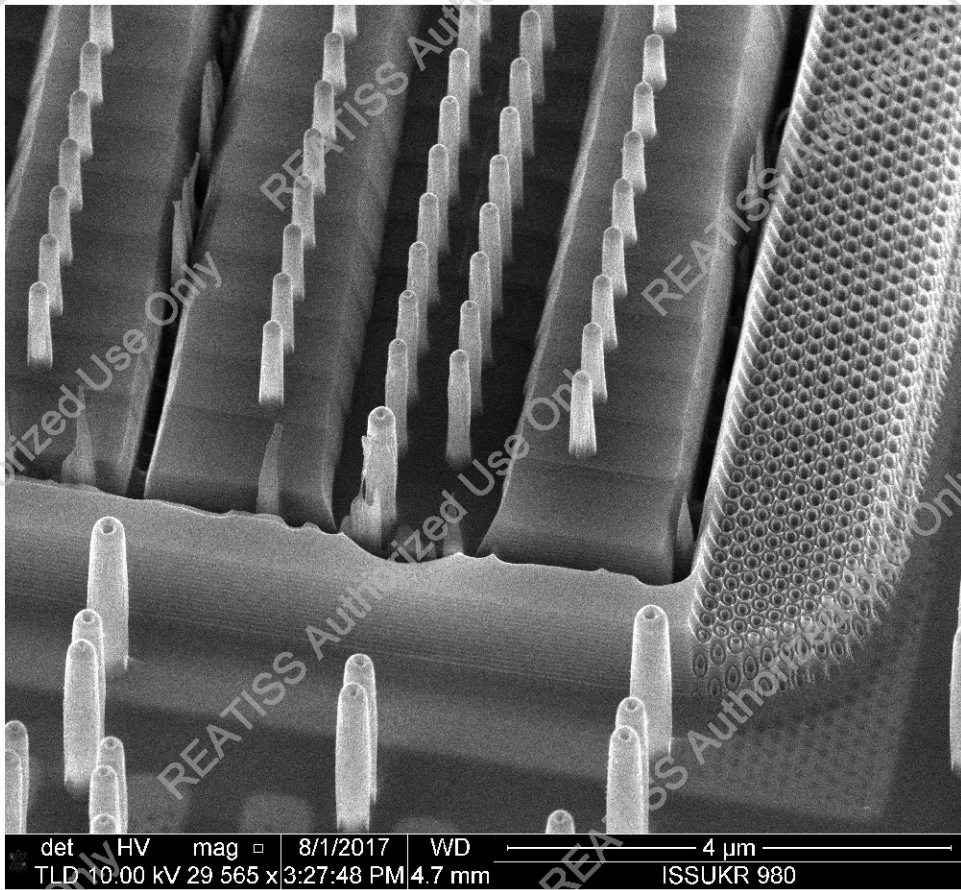


Figure 47. Top-down tilted view of NAND array edge

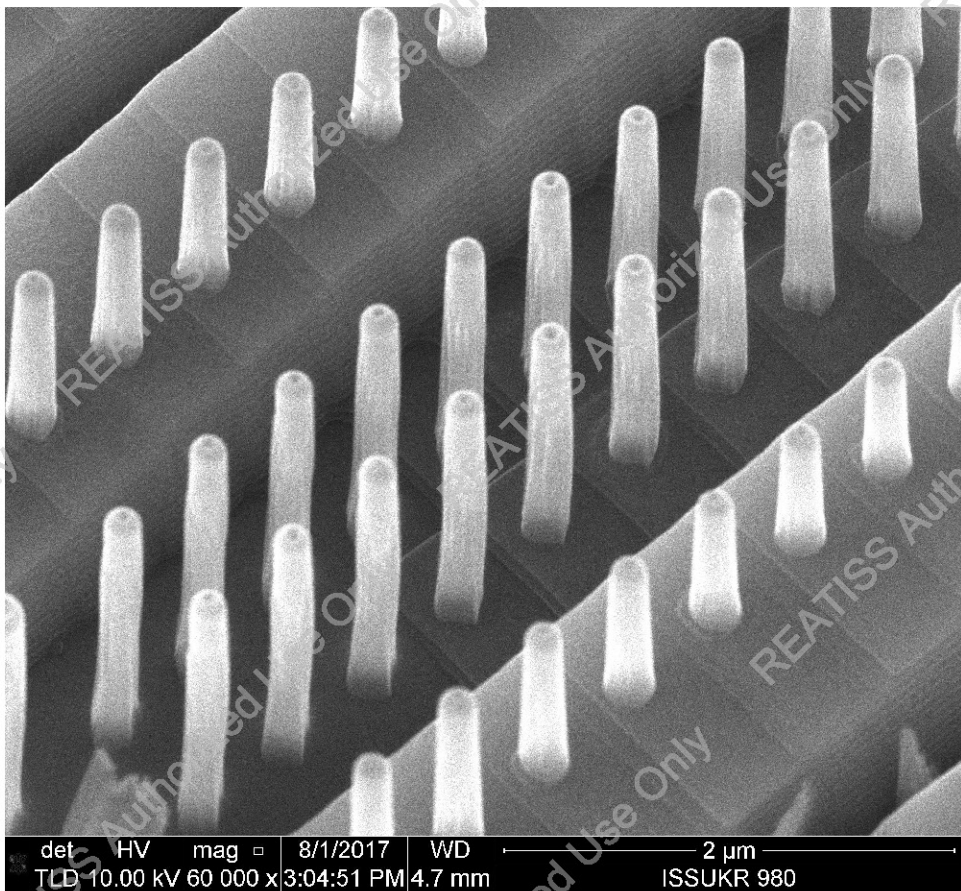


Figure 48. Top-down tilted view of control gates connection

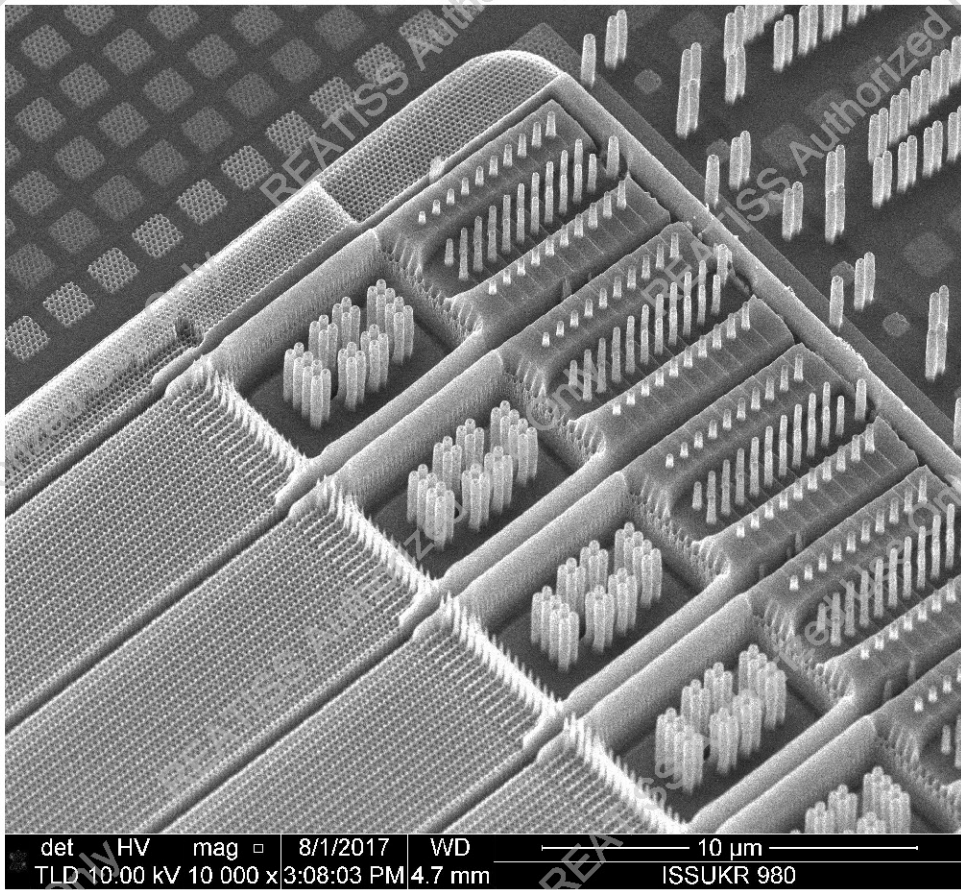


Figure 49. Top-down tilted view of NAND array edge

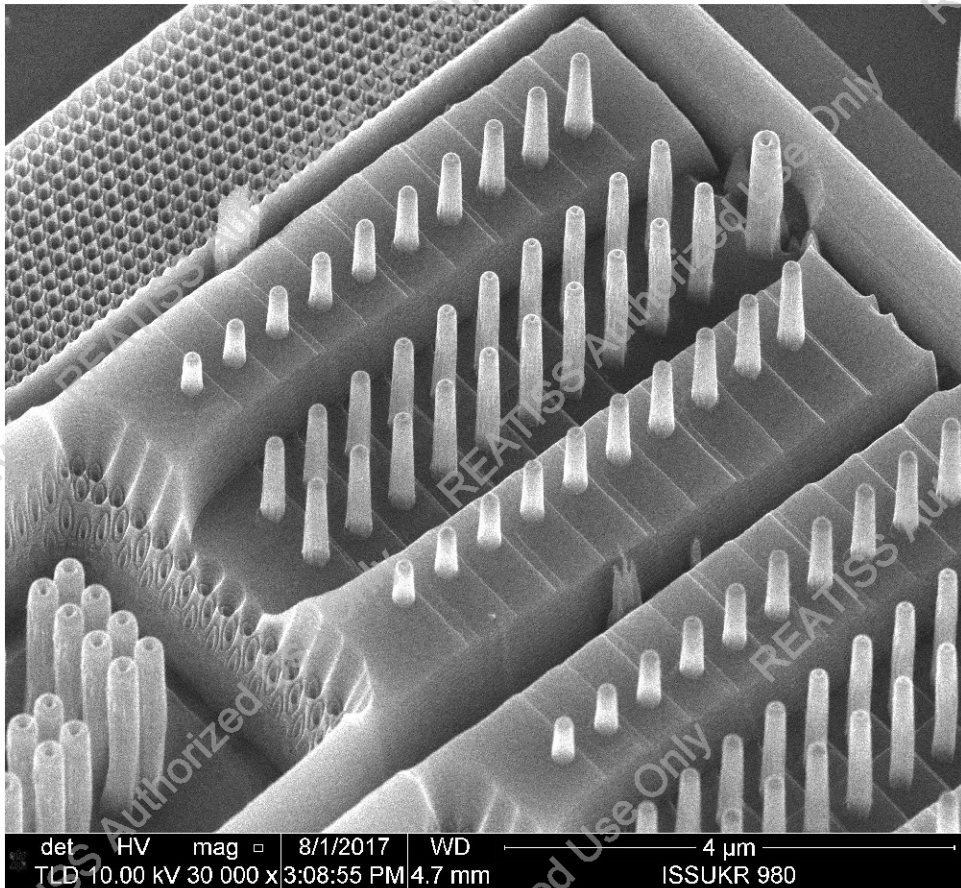


Figure 50. Top-down tilted view of NAND array edge

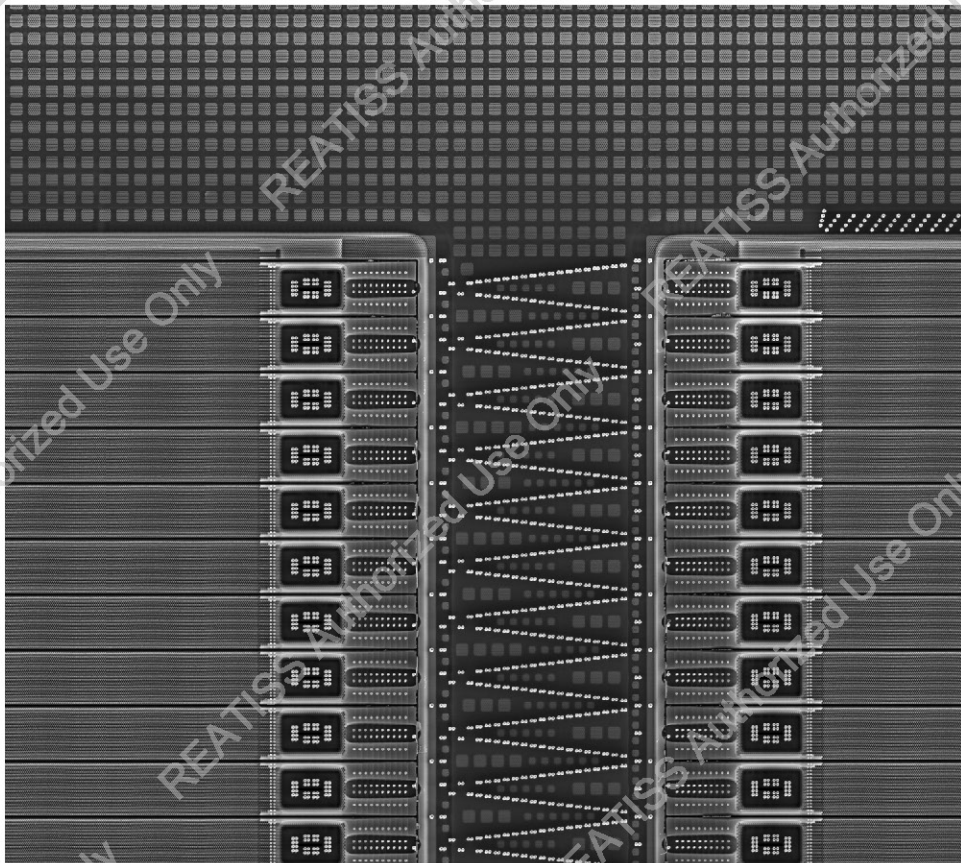


Figure 51. NAND array edges

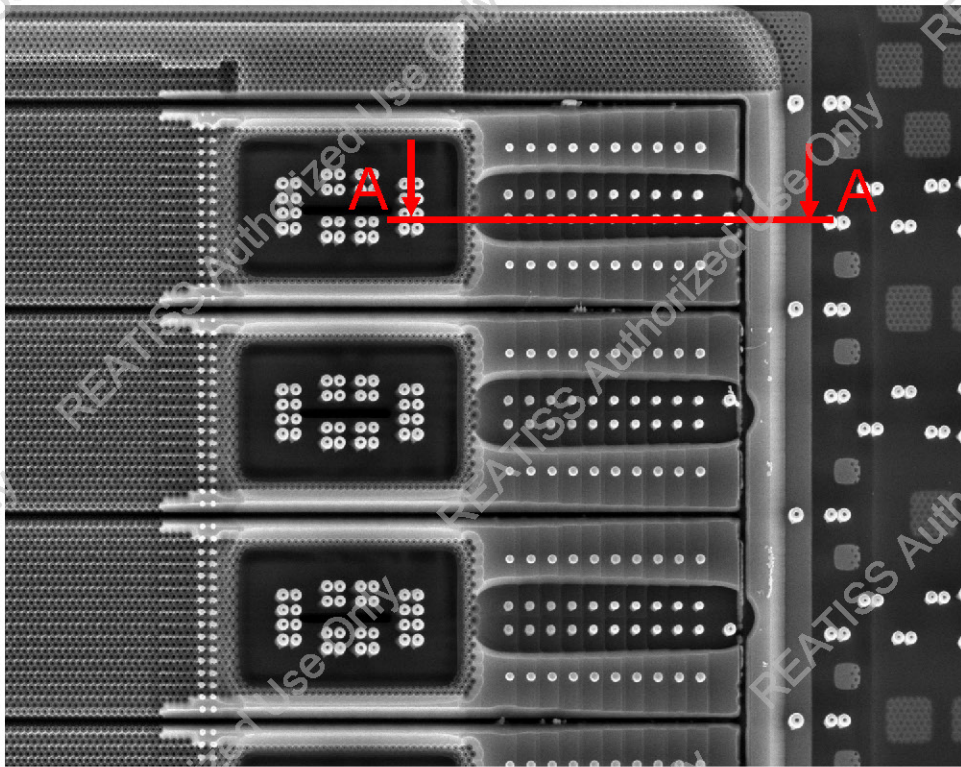


Figure 52. Control gates connections with approximate place of section A-A marked

Following figures show structures of the section A-A

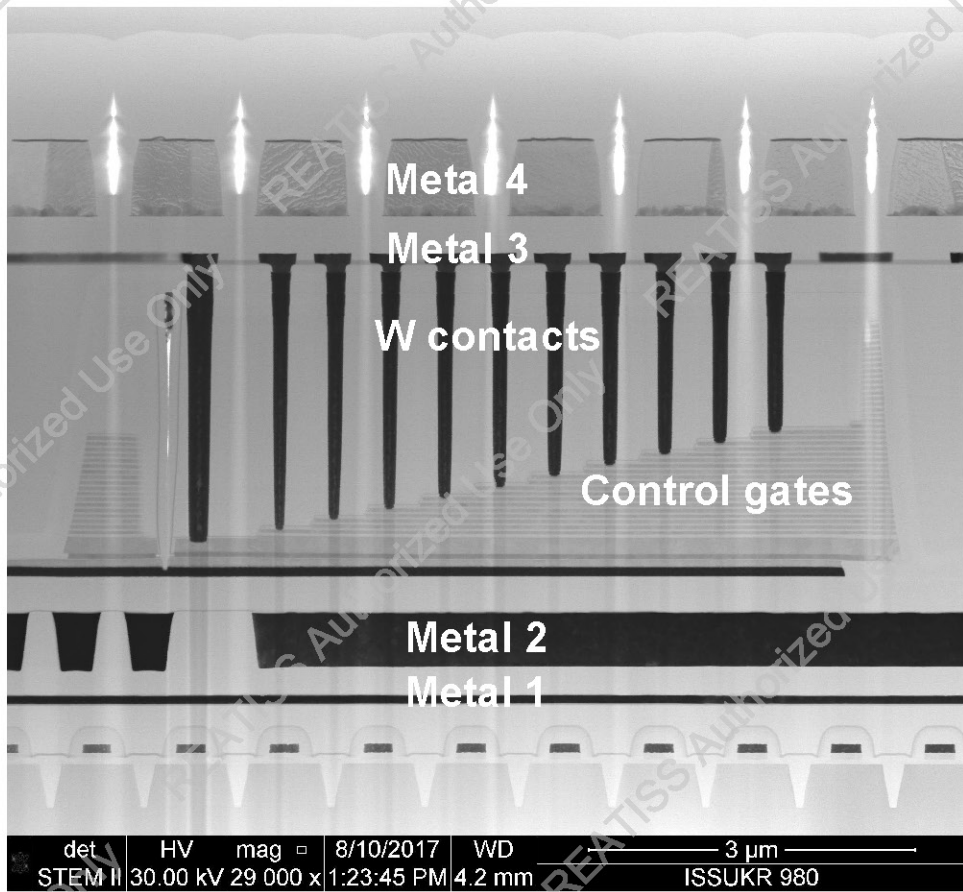


Figure 53. Control gates stack connection (section A-A)

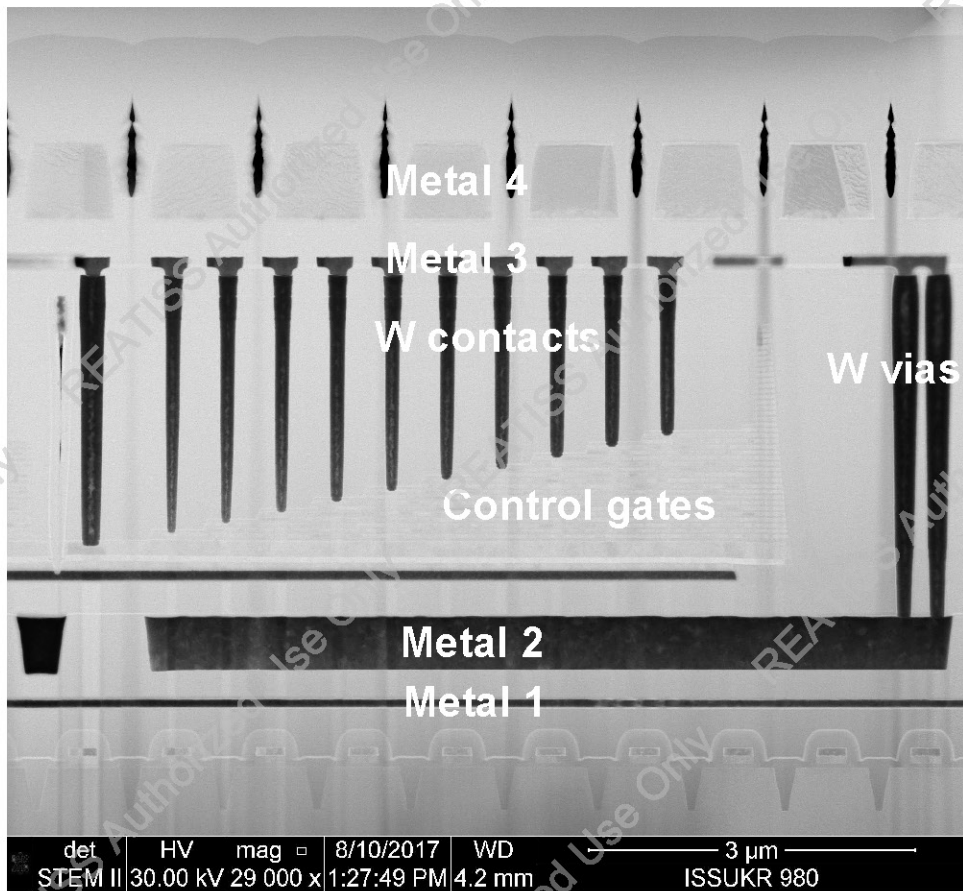


Figure 54. Control gates stack connection (section A-A)

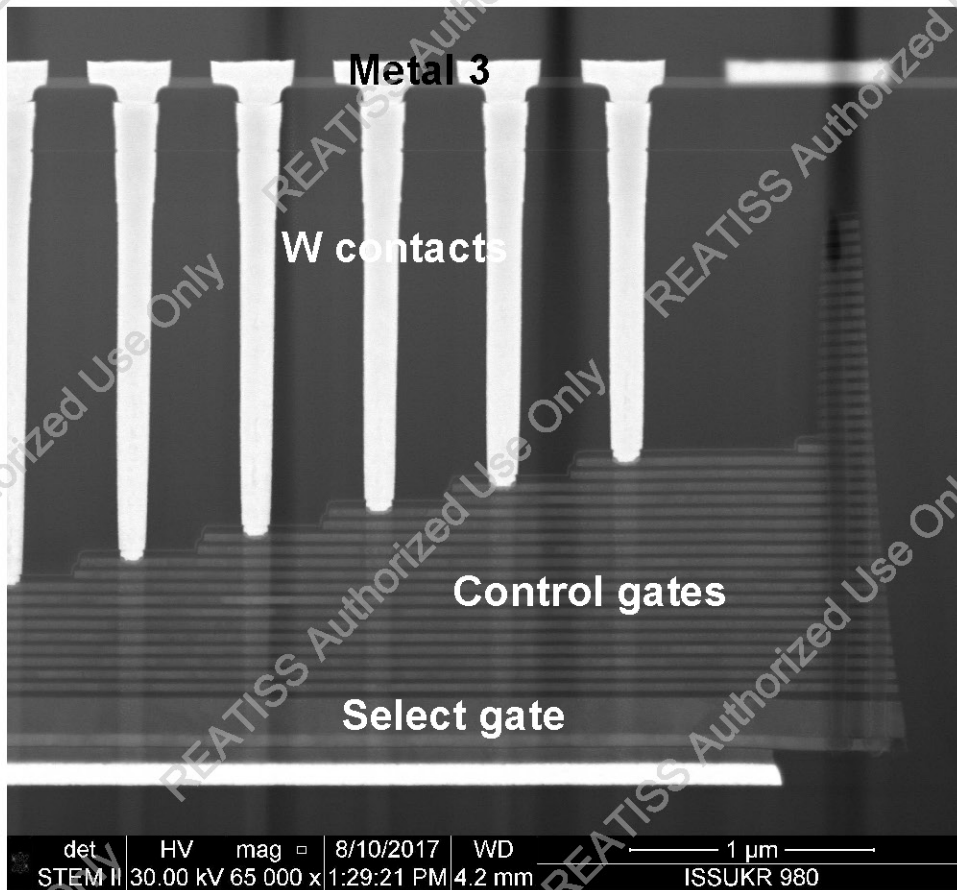


Figure 55. Control gates stack connection (section A-A)

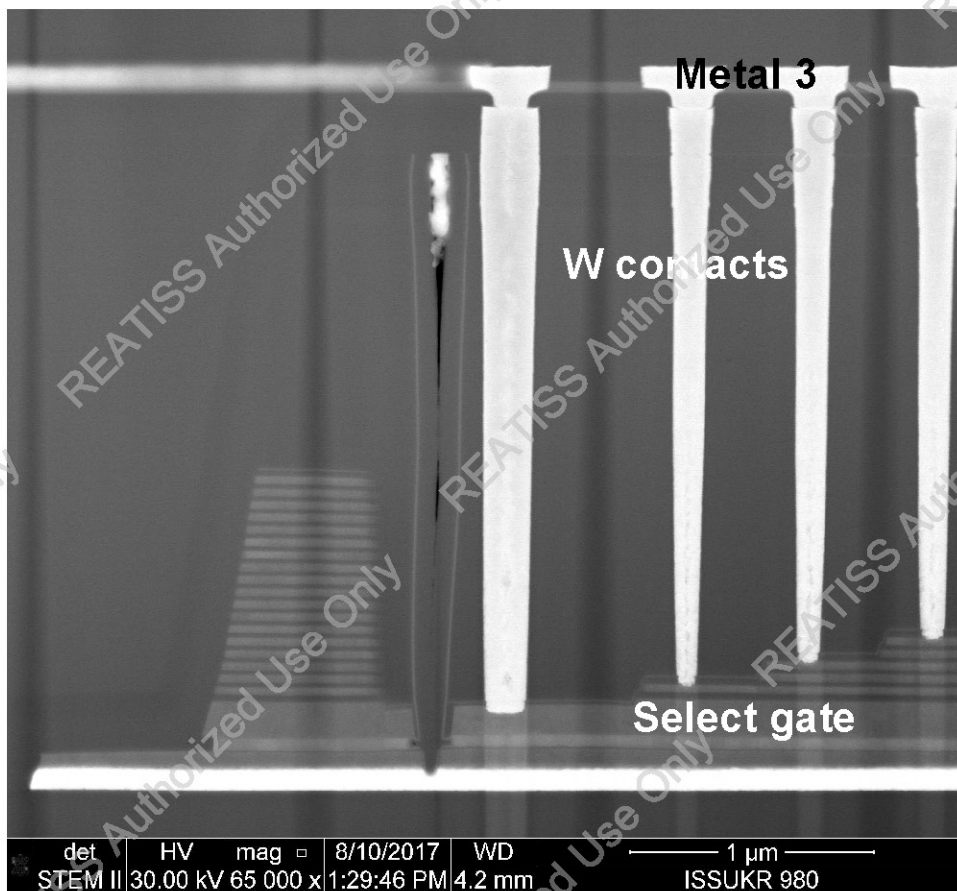


Figure 56. Control gates stack and select gate connection (section A-A)

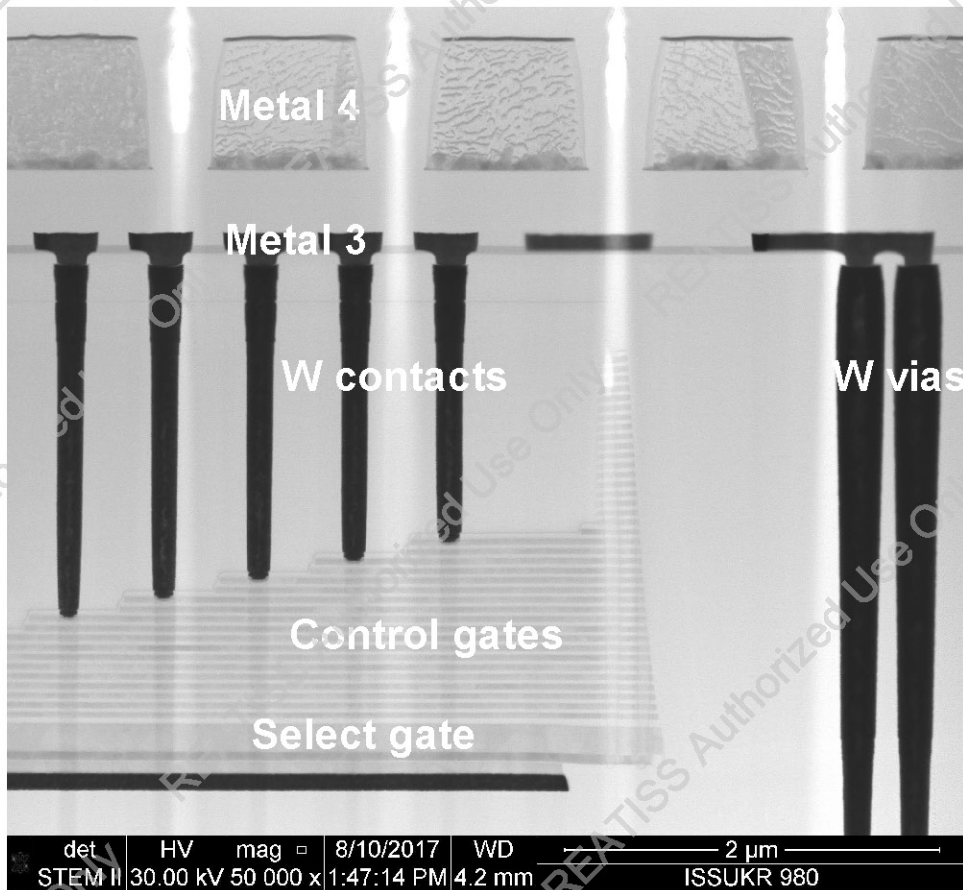


Figure 57. Control gates stack connection (section A-A)



Figure 58. Control gates connection (section A-A)

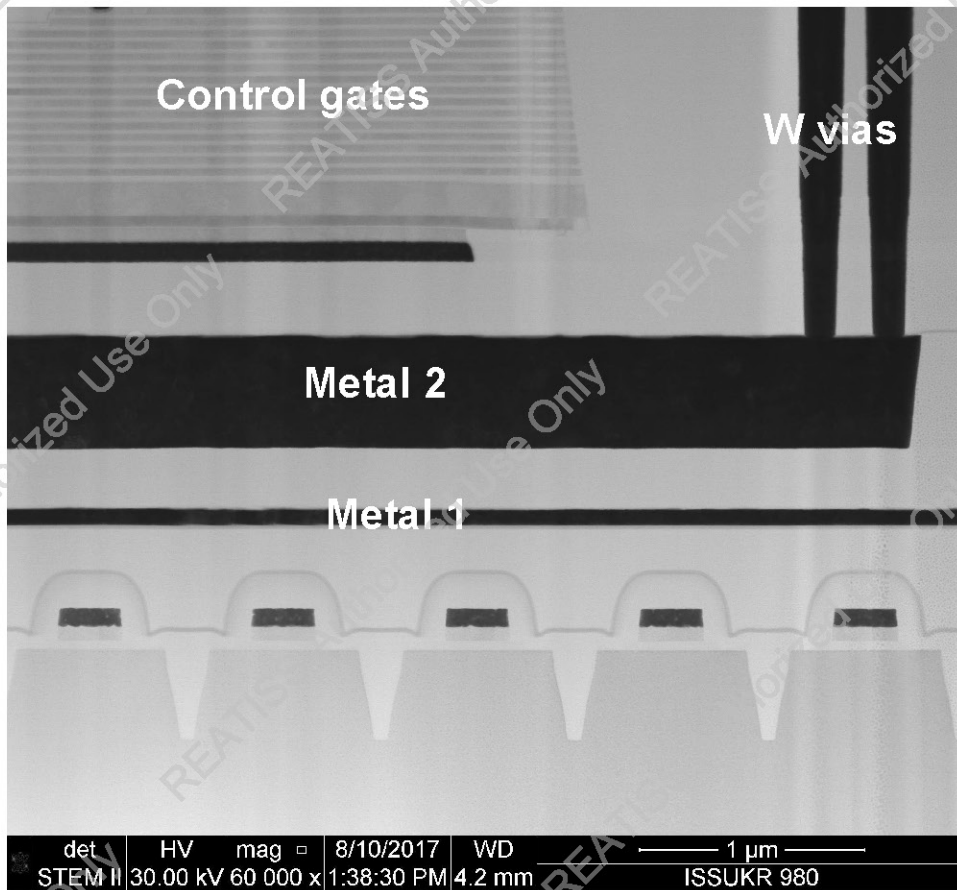


Figure 59. NAND array edge across bitlines (section A-A)

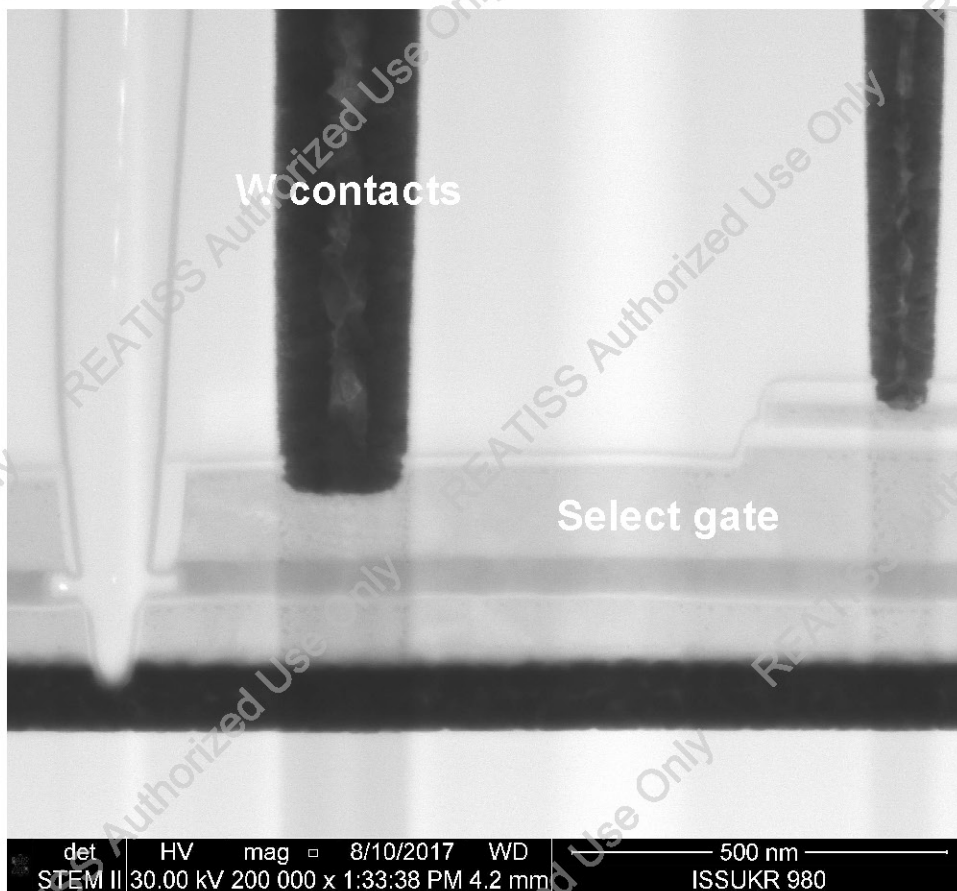


Figure 60. Select gate connection (section A-A)

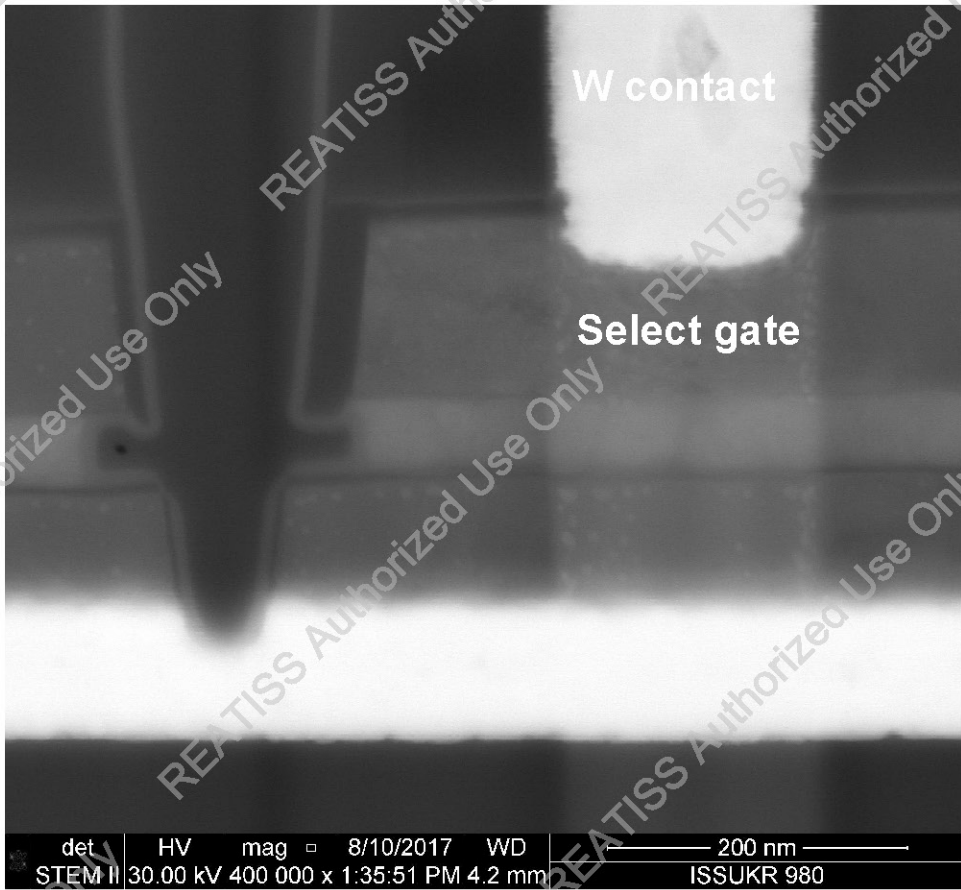


Figure 61. Select gate connection (section A-A)

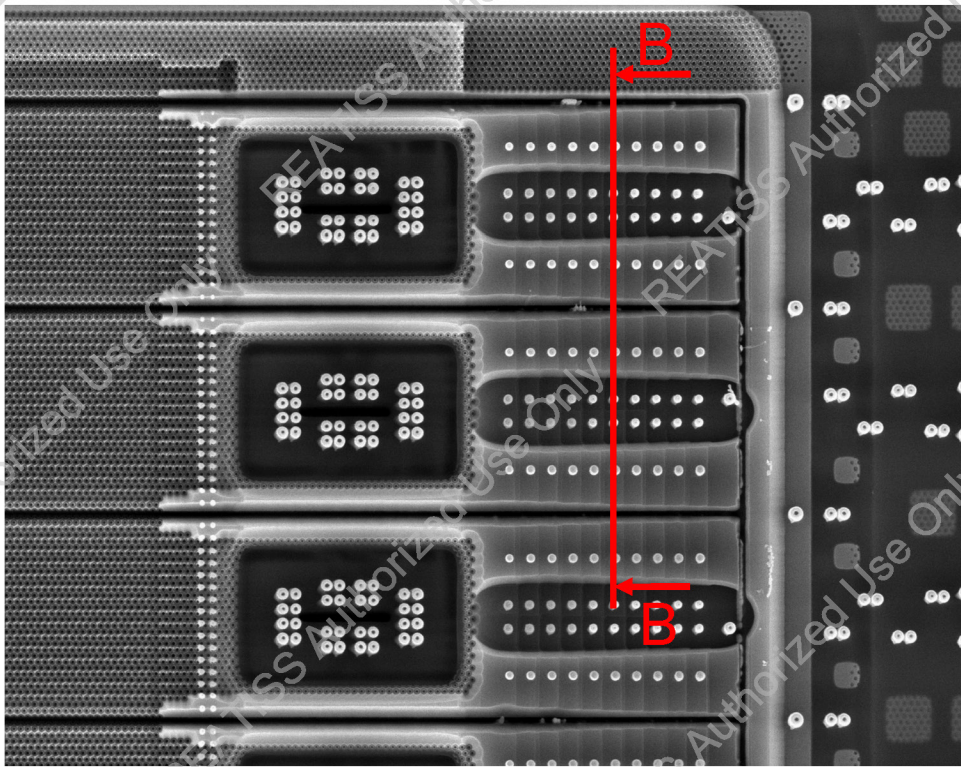


Figure 62. Control gates connections with approximate place of section B-B marked

Following figures show structures of the section B-B

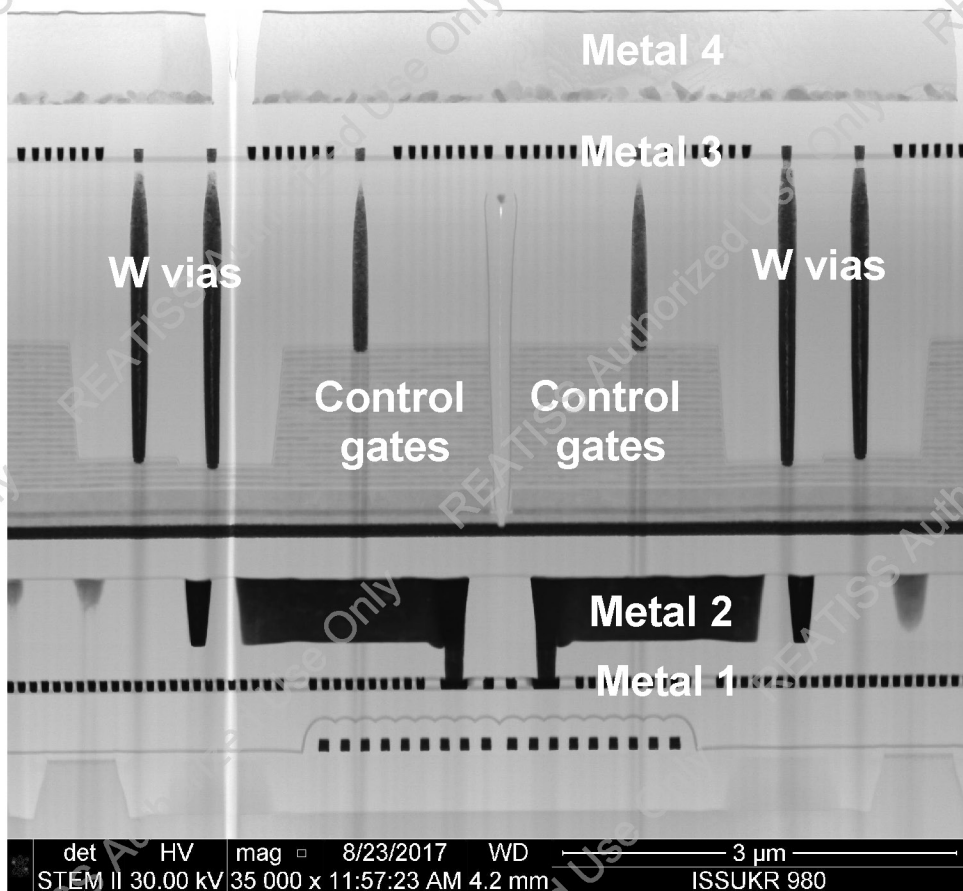


Figure 63 Control gates connections (section B-B)

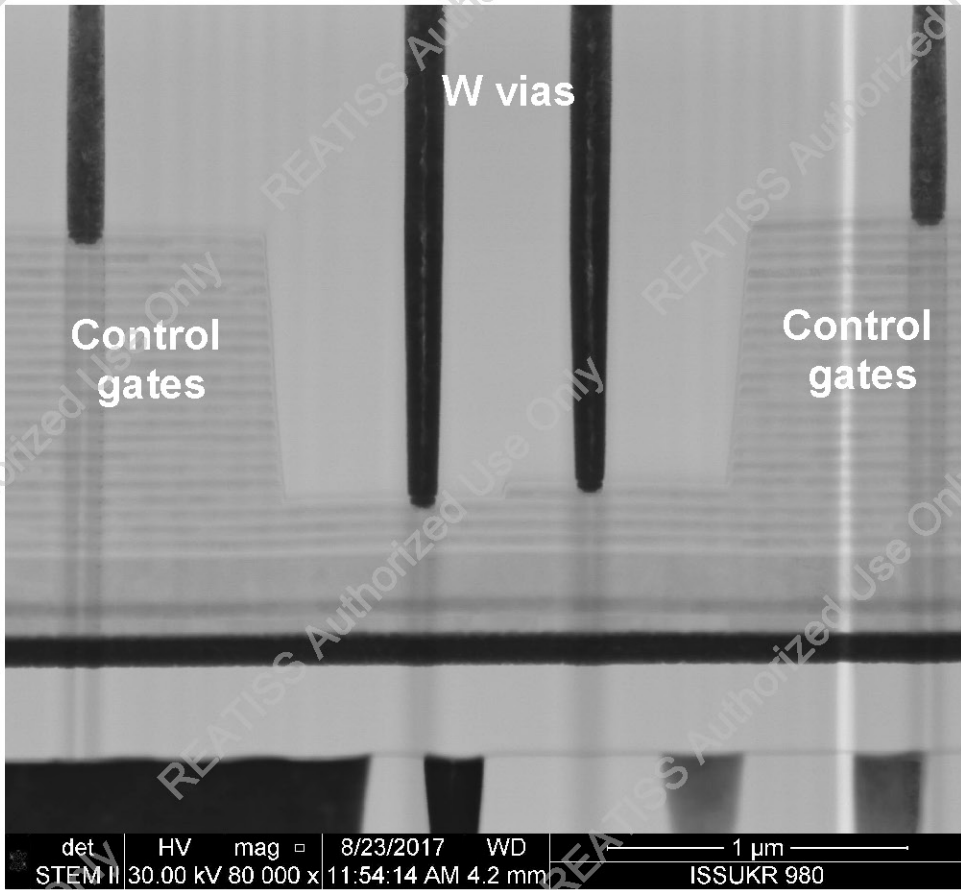


Figure 64. Control gates connections (section B-B)

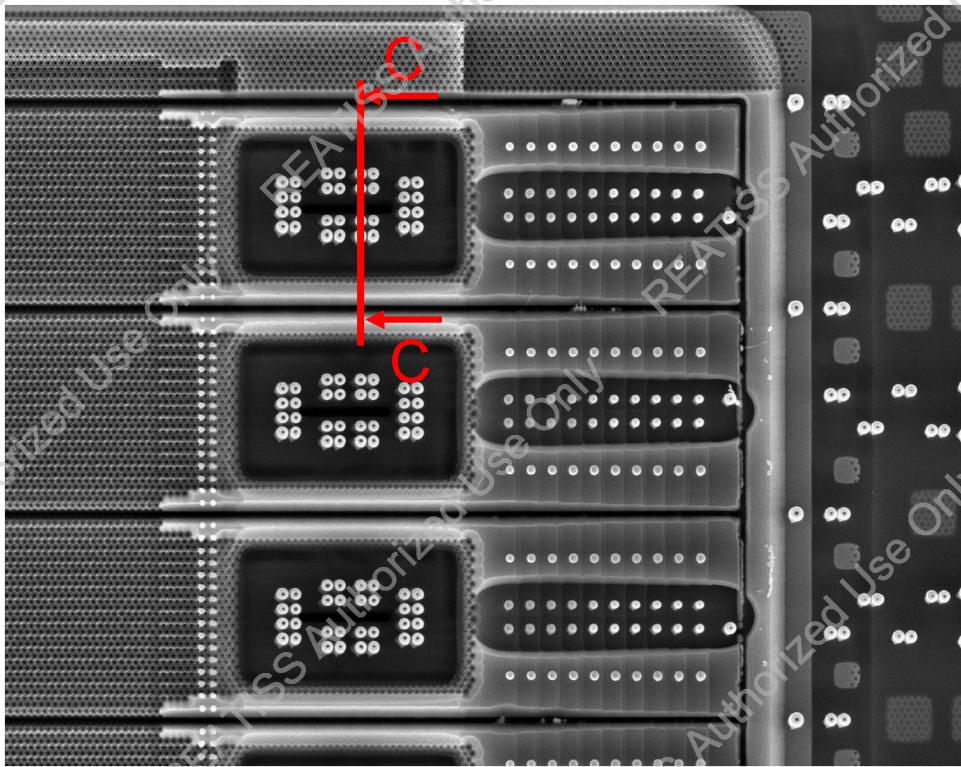


Figure 65. Control gates connections with approximate place of section C-C marked

Following figures show structures of the section C-C

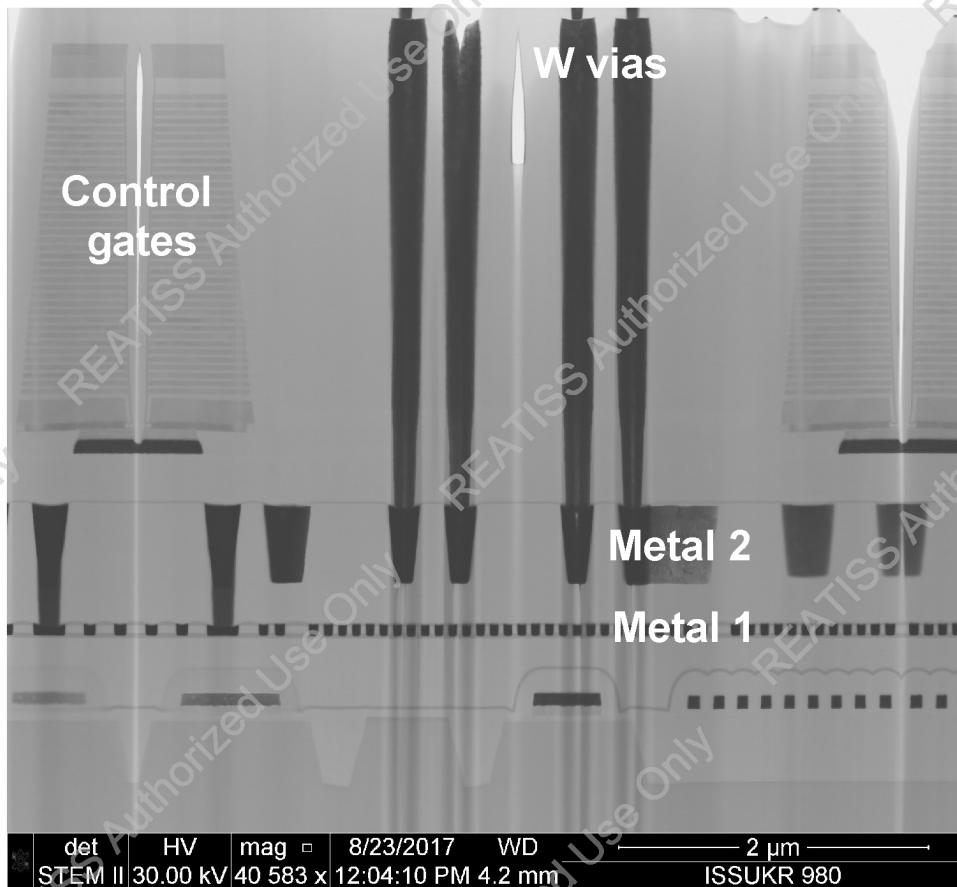


Figure 66. Control gates stacks, W M1, M2 lines and vias (section C-C)

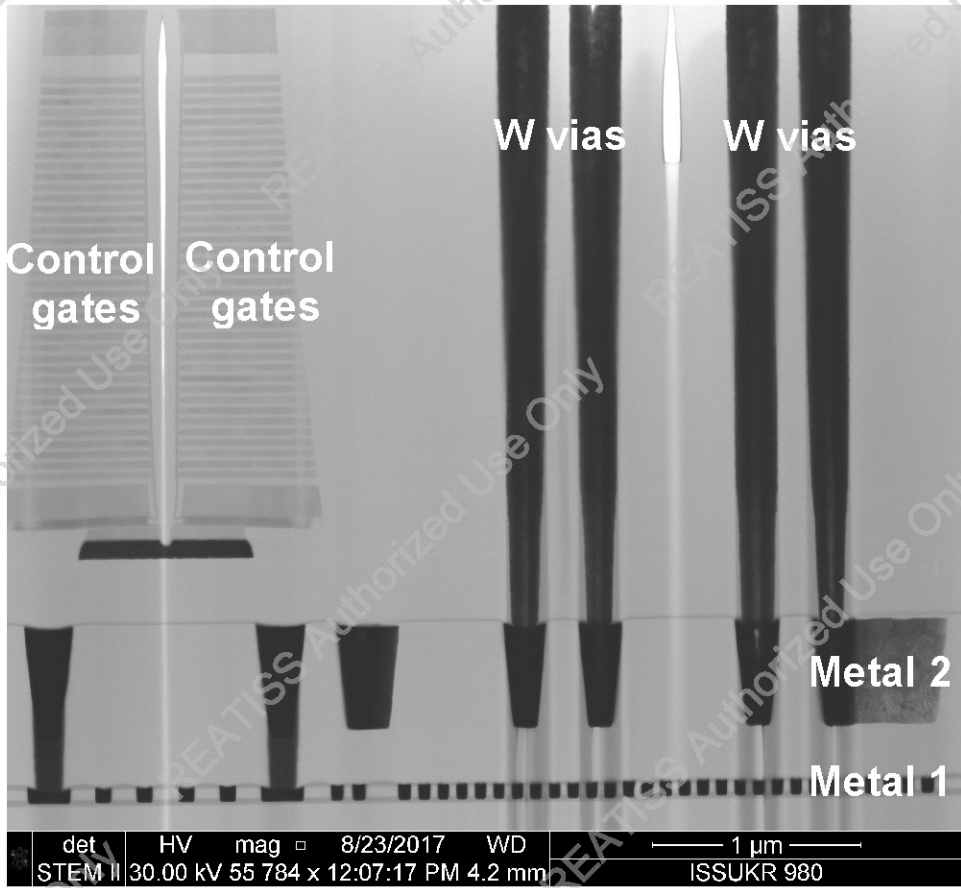


Figure 67. Control gates stacks, W M1, M2 lines and vias (section C-C)

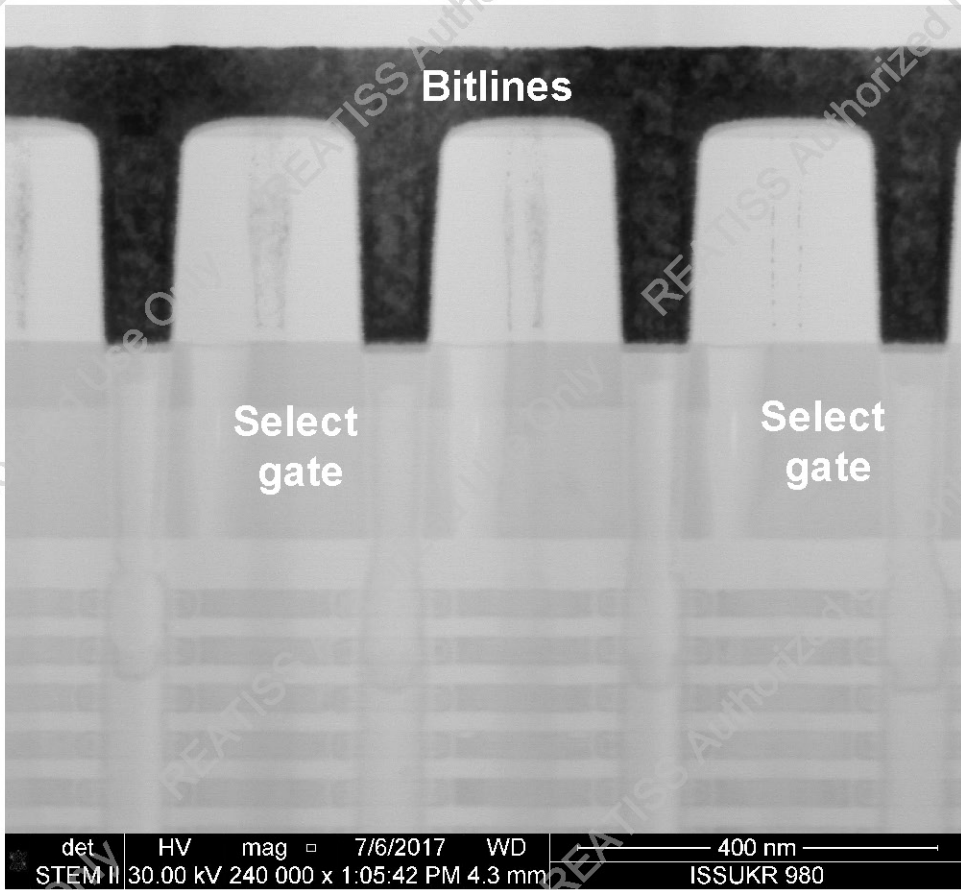


Figure 68. NAND array bitlines connection and select gates

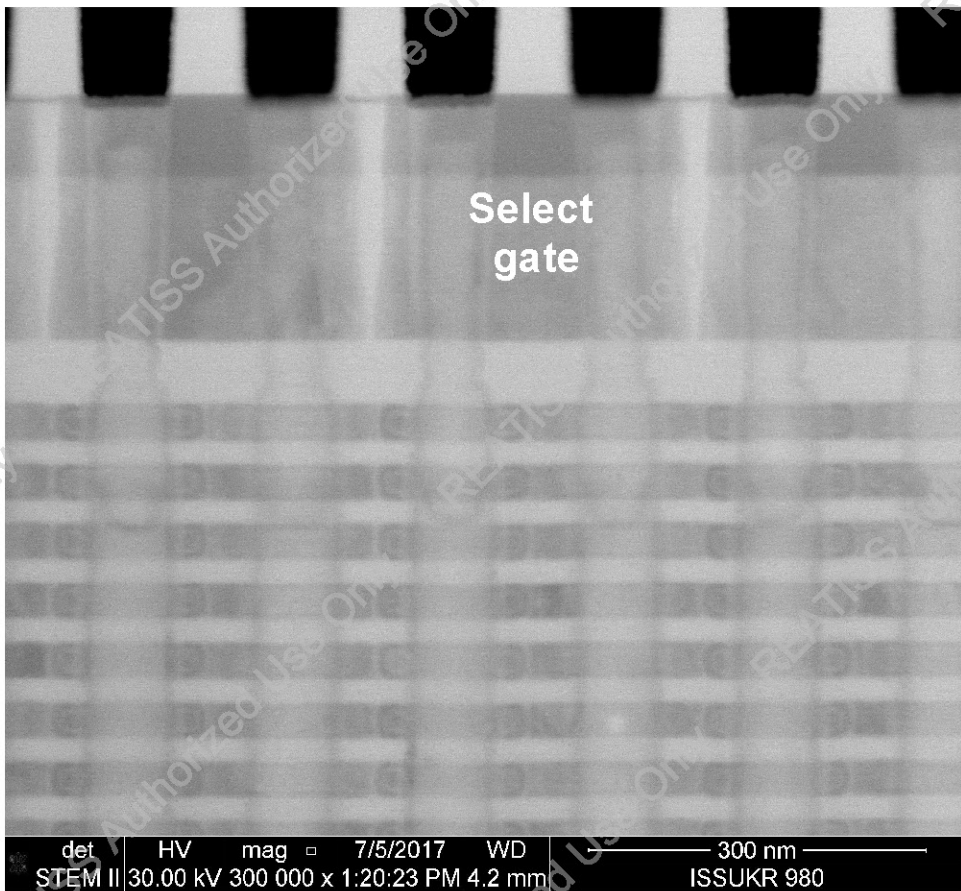


Figure 69. NAND array bitlines connection and select gates

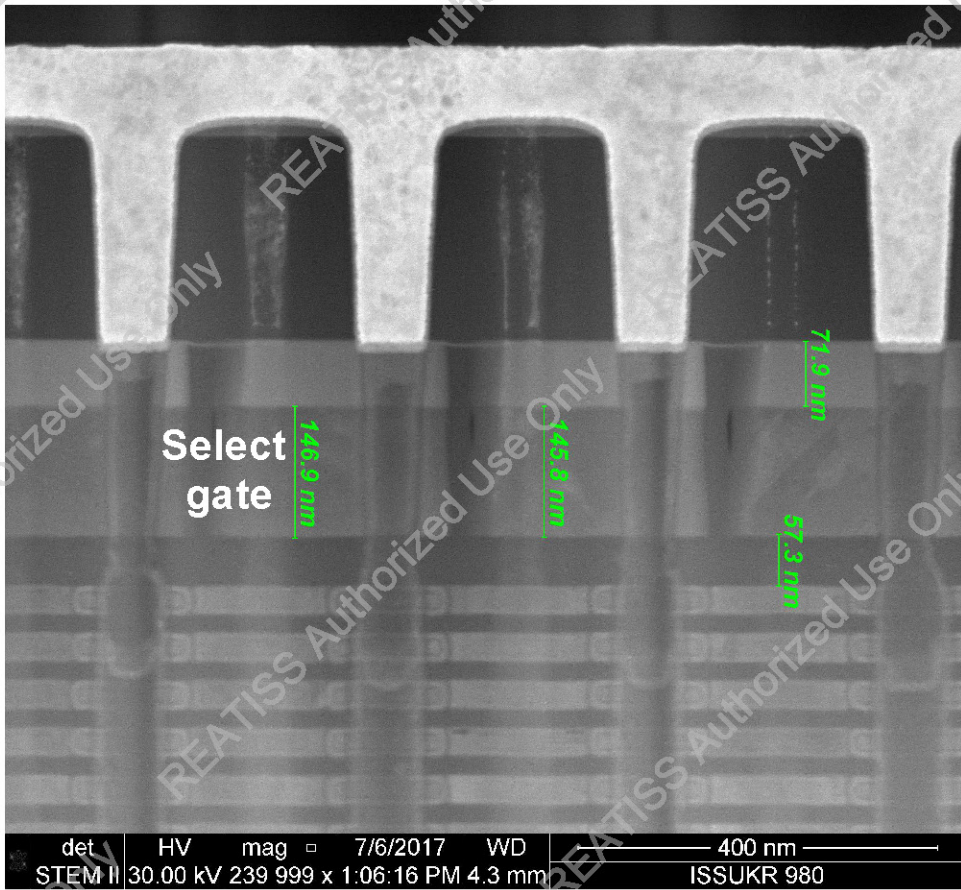


Figure 70. NAND array bitlines connection and select gates

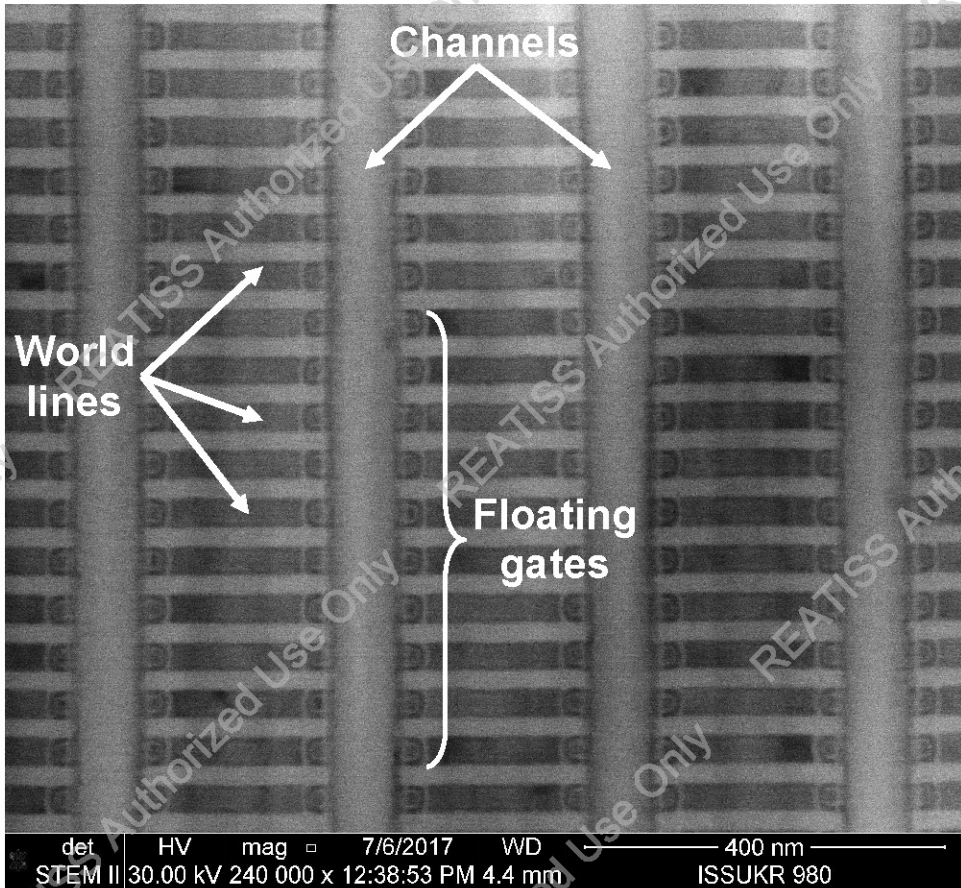


Figure 71. NAND cells array

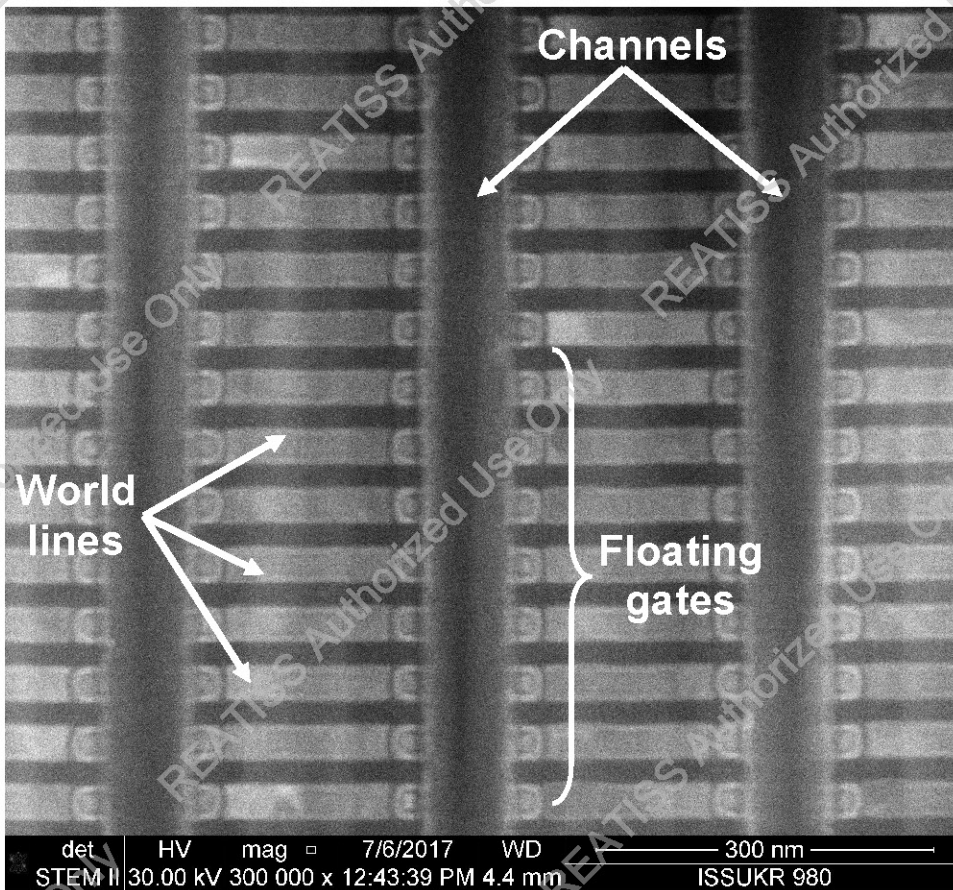


Figure 72. NAND cells array

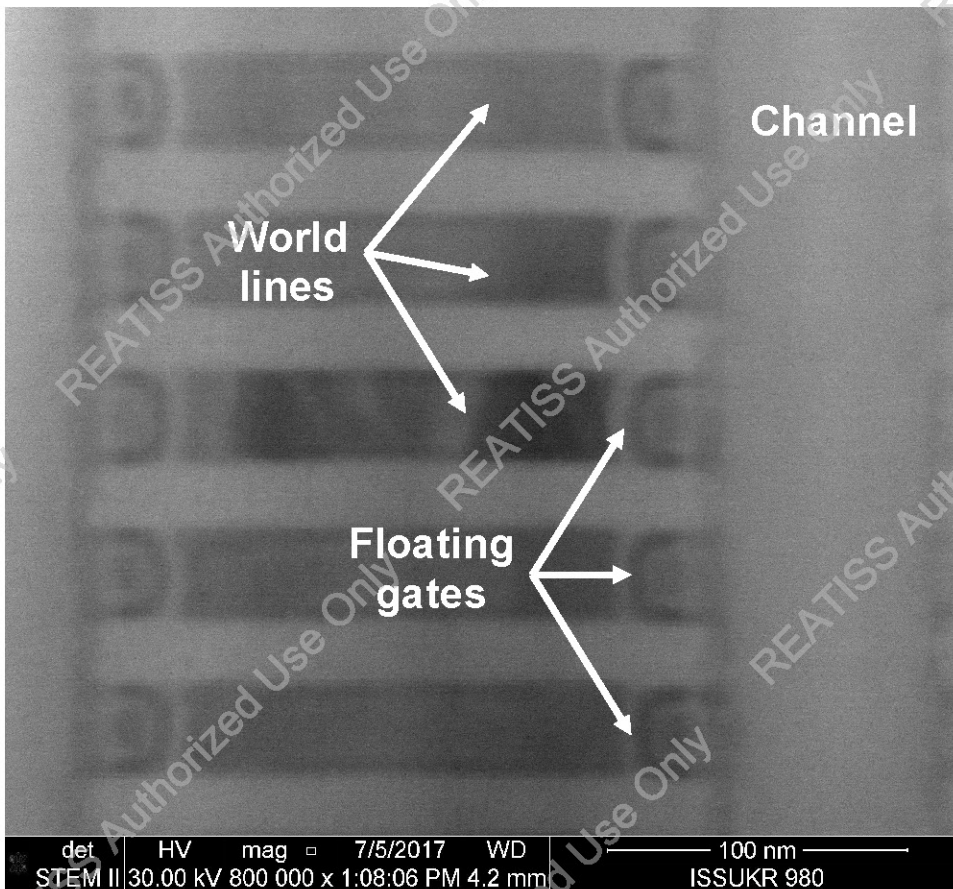


Figure 73. NAND cells

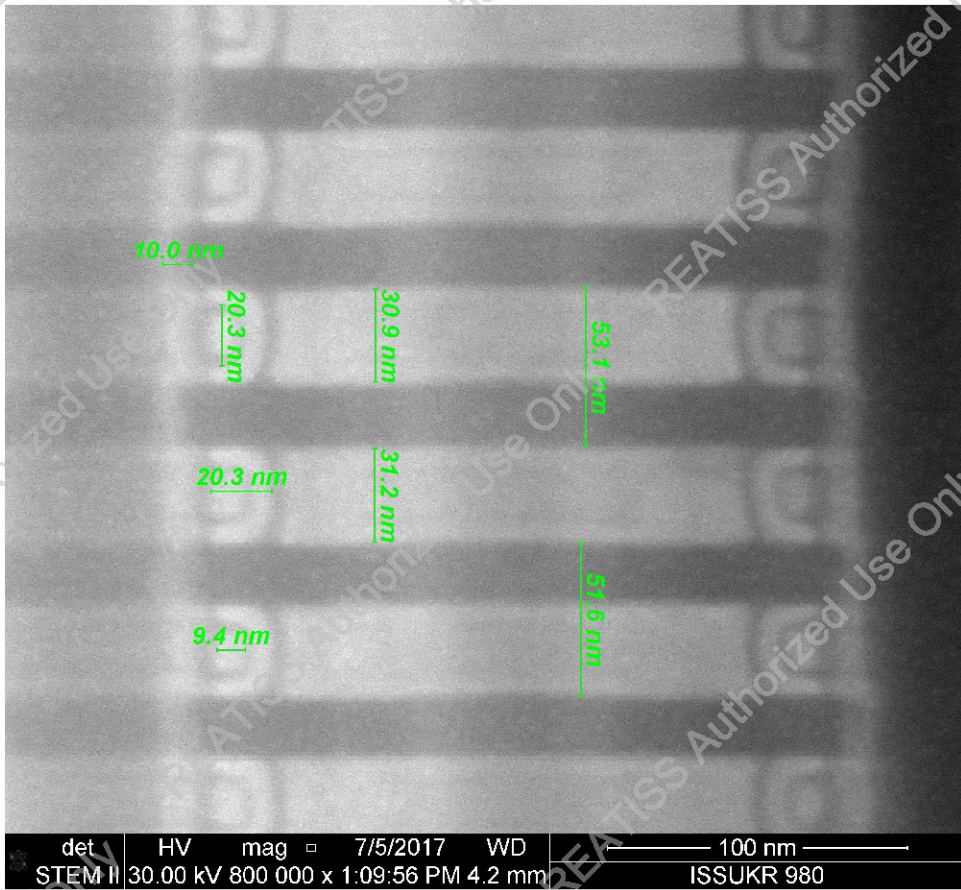


Figure 74. NAND cells

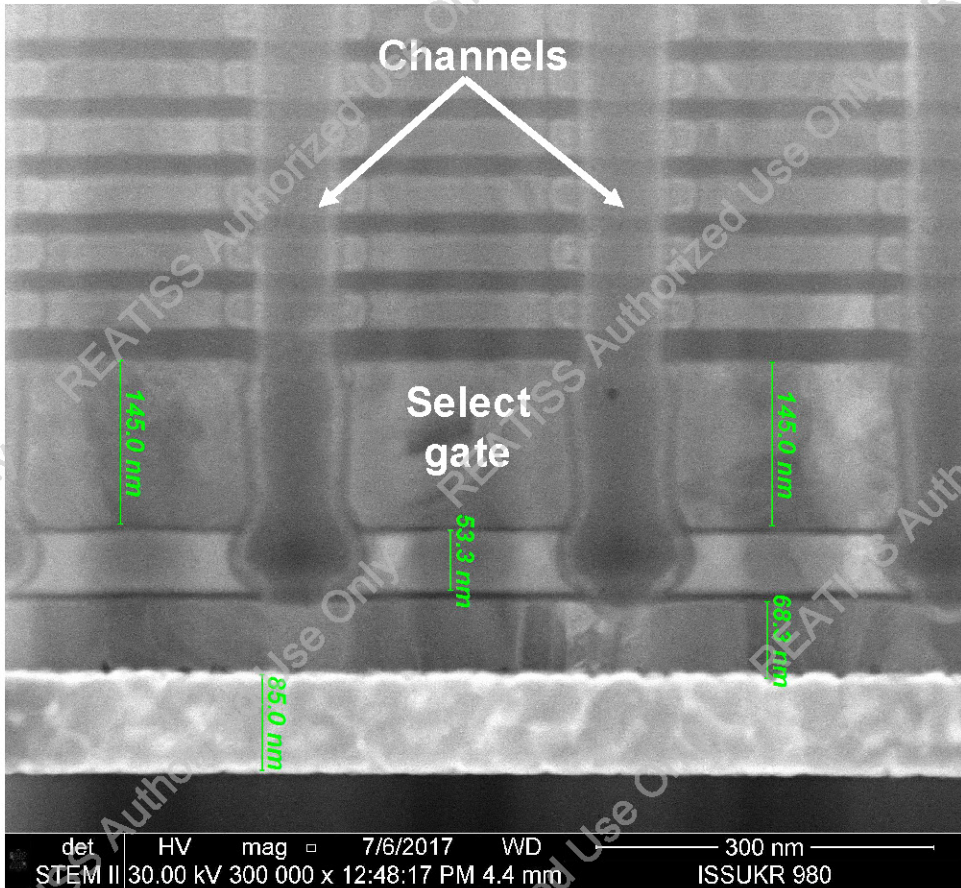


Figure 75. NAND cells array bottom

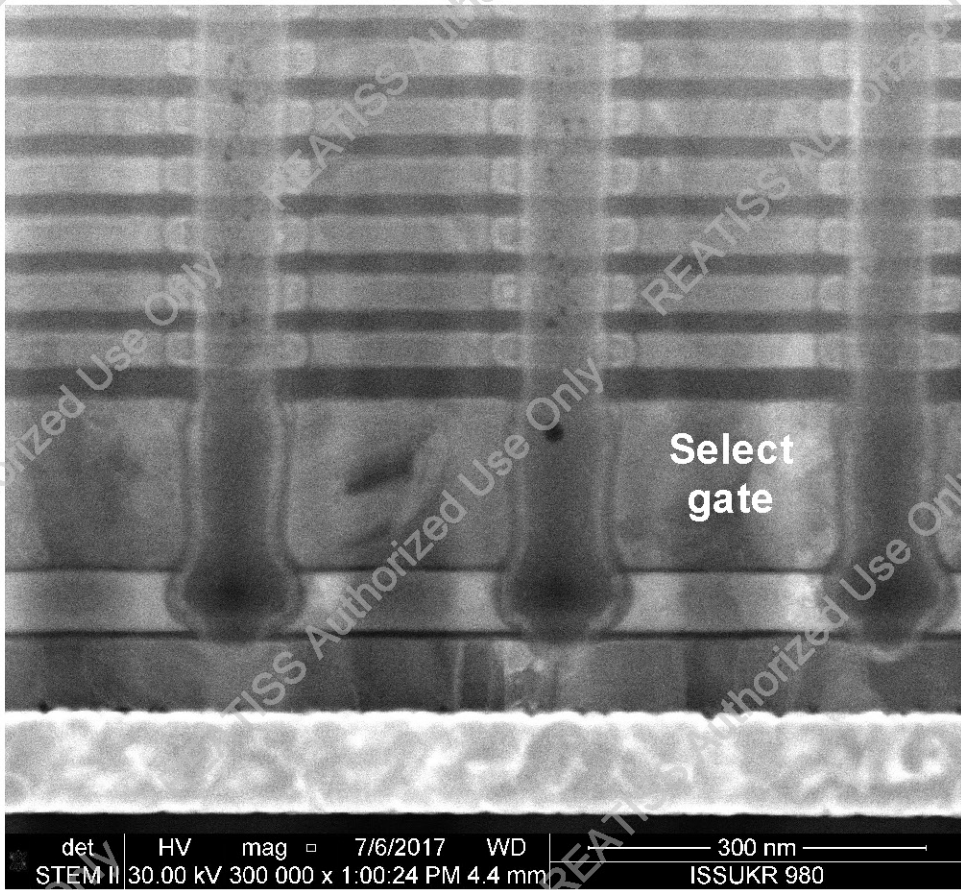


Figure 76. NAND cells array bottom

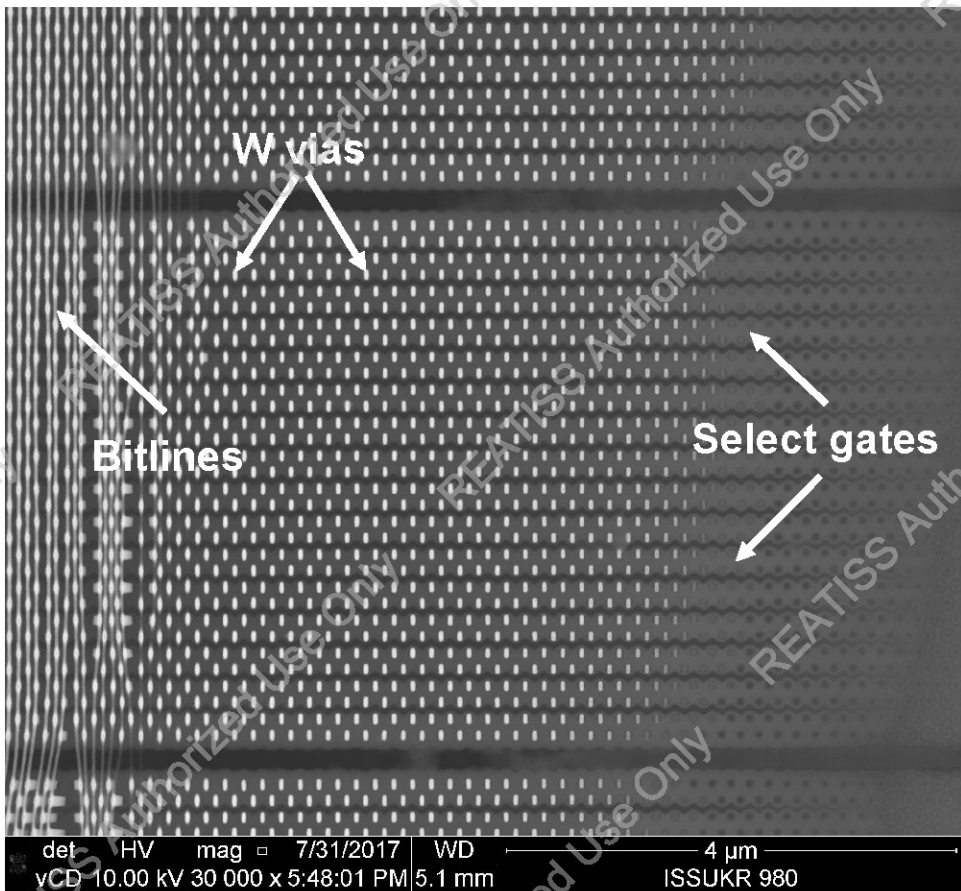


Figure 77. Top-down slanted section view of W M3 lines, W vias, select gates

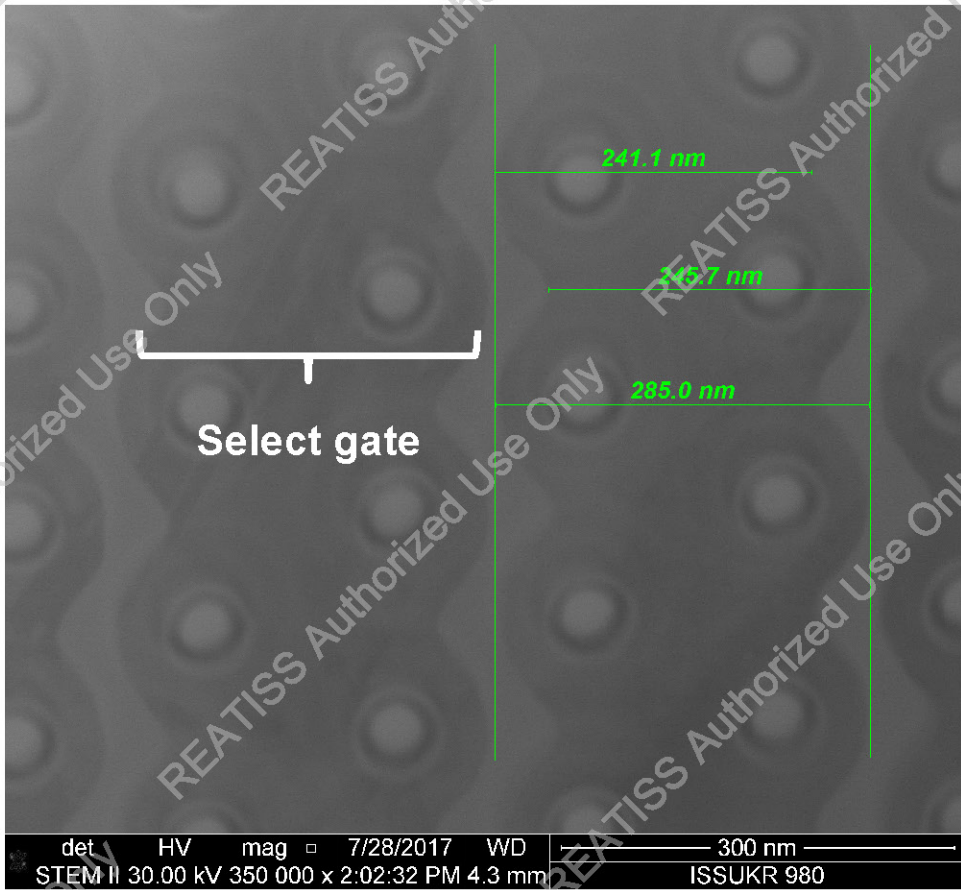


Figure 78. Top-down section view of top select gates

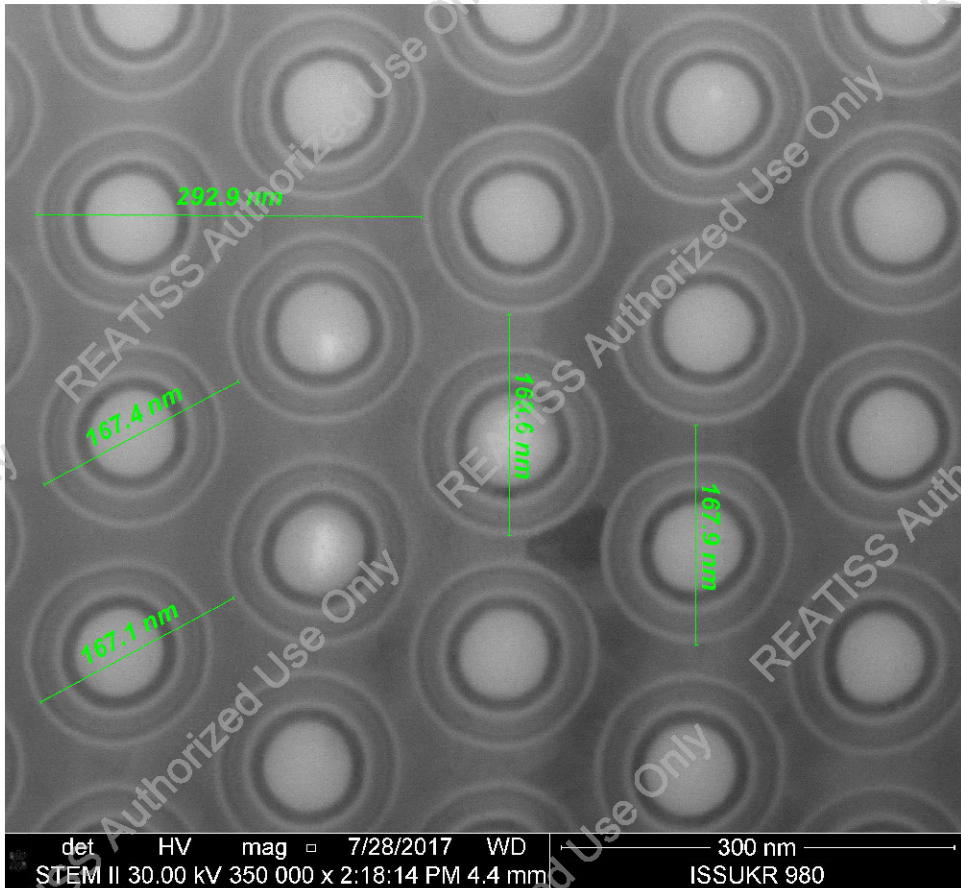


Figure 79. Top-down section of memory cells

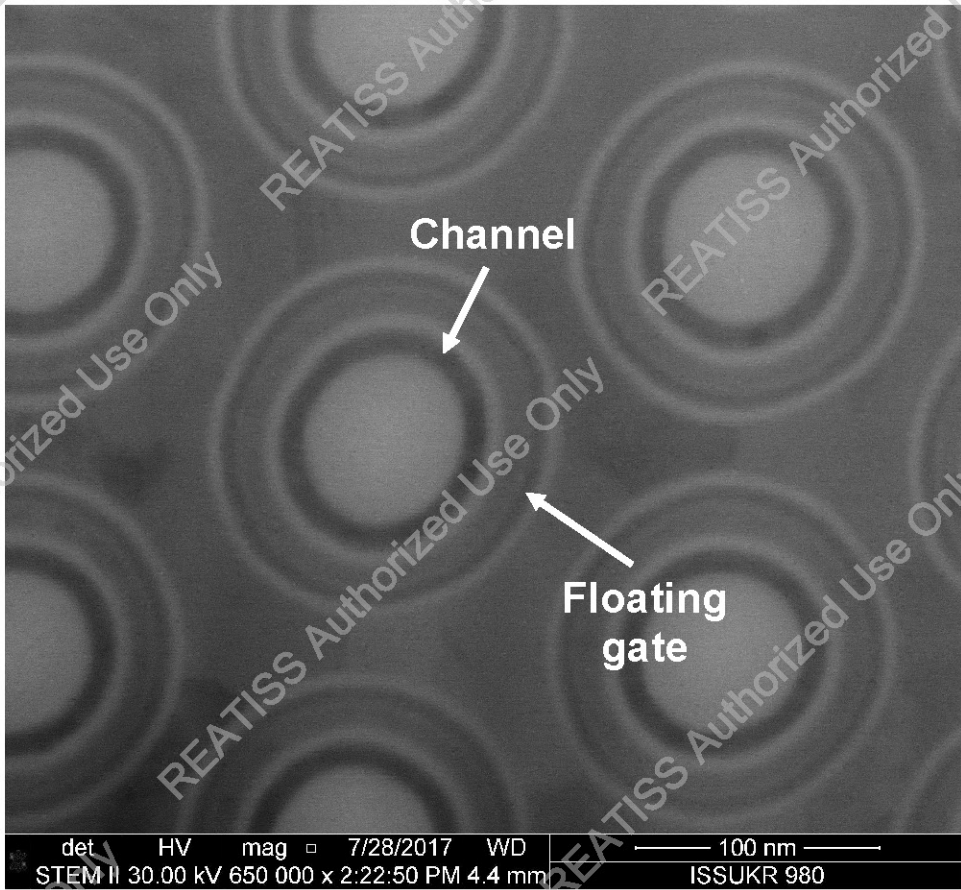


Figure 80. Top-down section of memory cells

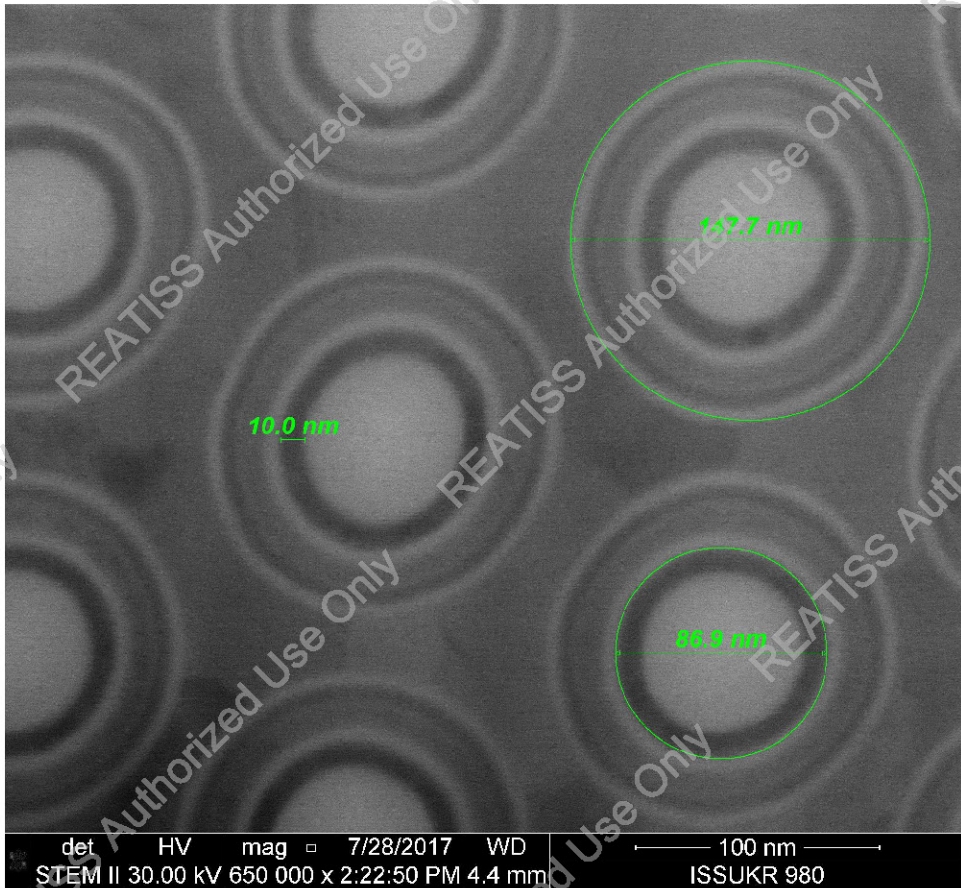


Figure 81. Top-down section of memory cells

Material Analysis

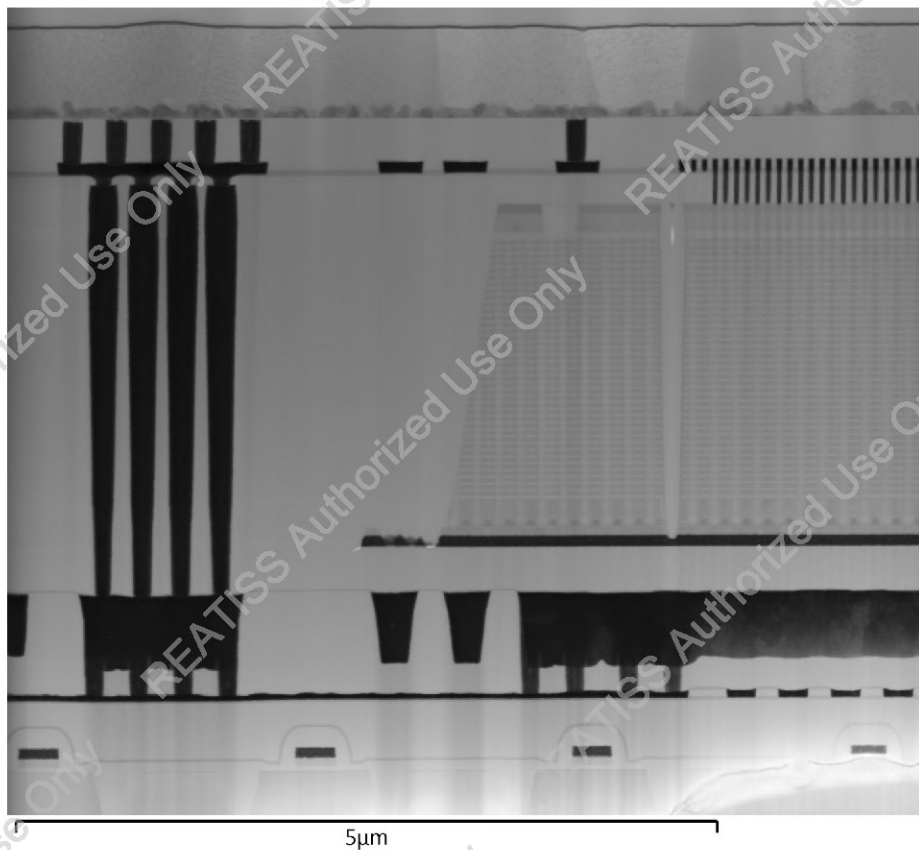


Figure 82. General structure

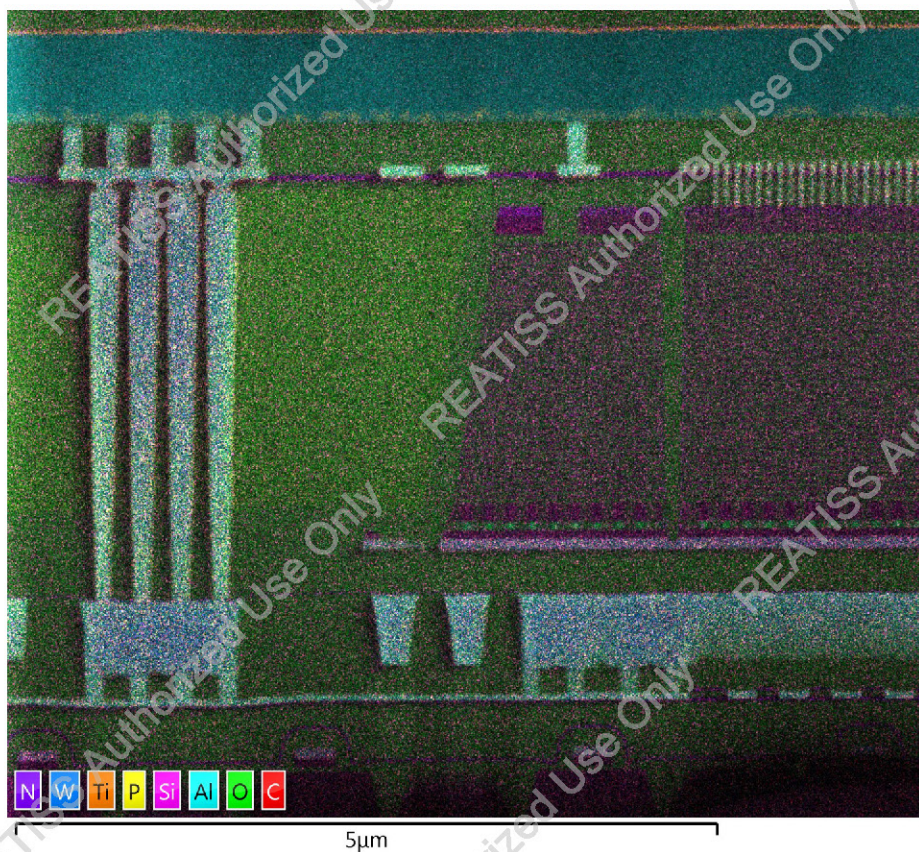


Figure 83. Layered EDX map of general structure

Al K series

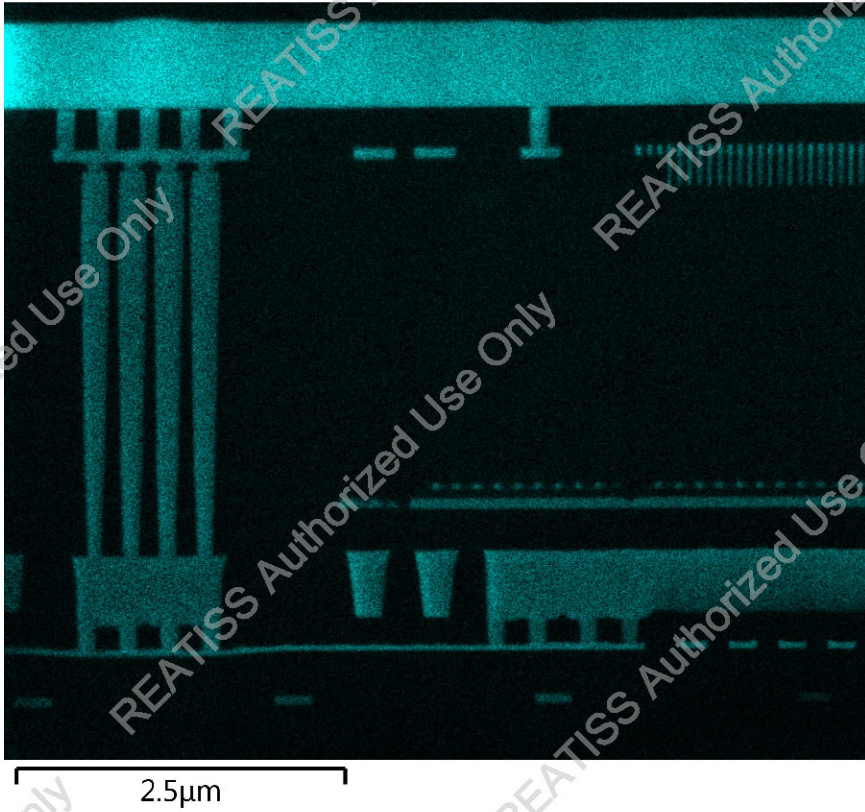


Figure 84. Aluminum EDX map layer

W L series

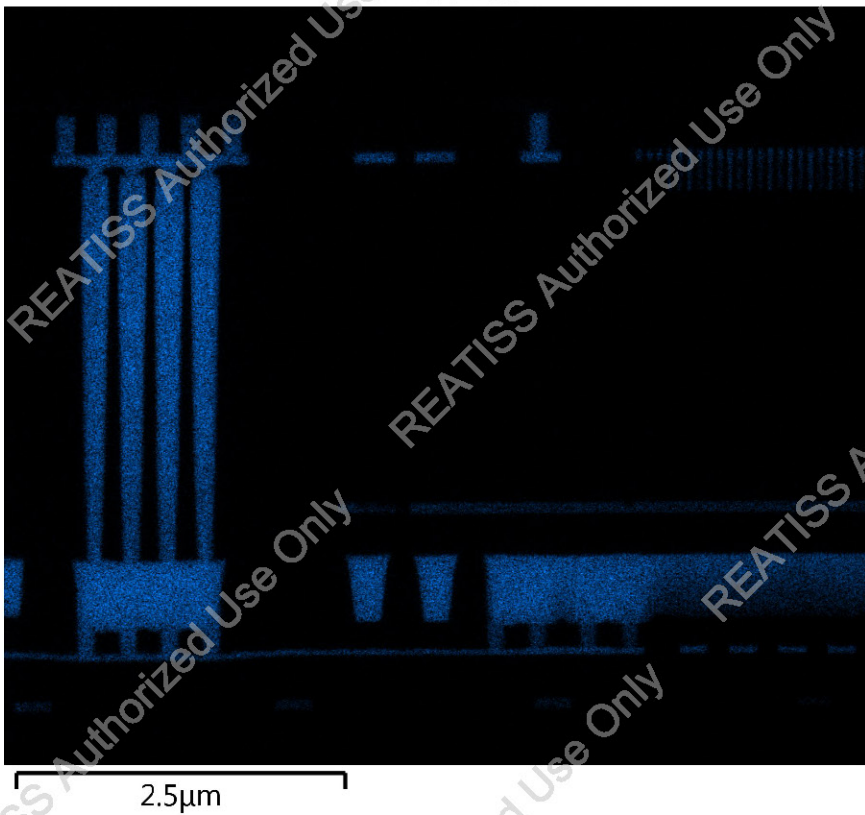


Figure 85. Tungsten EDX map layer

Ti K series

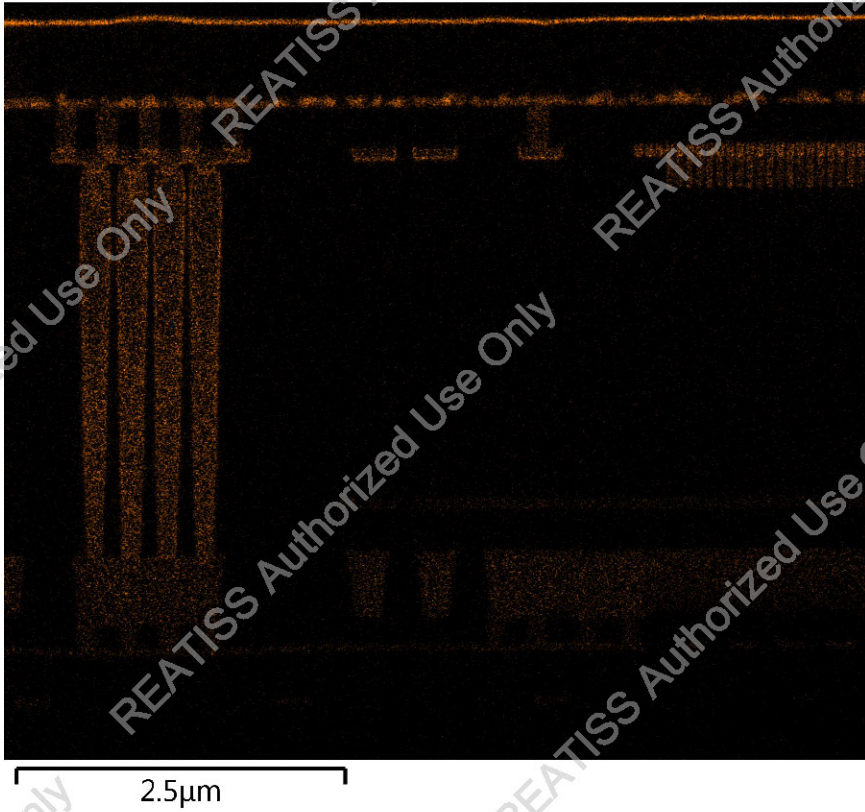


Figure 86. Titanium EDX map layer

C K series

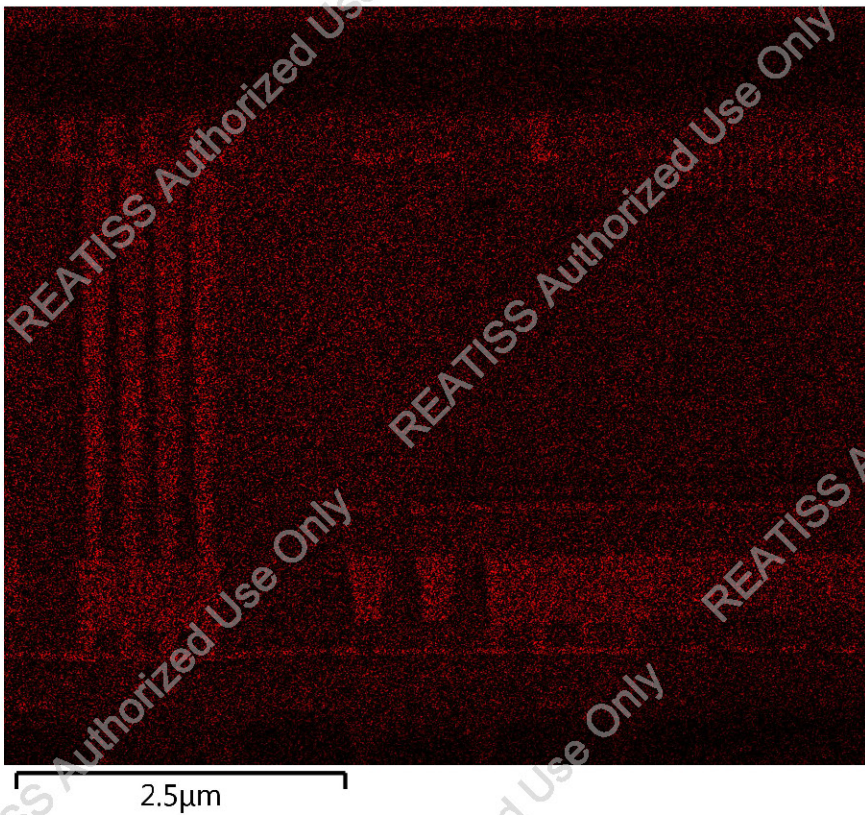


Figure 87. Carbon EDX map layer

Si K series

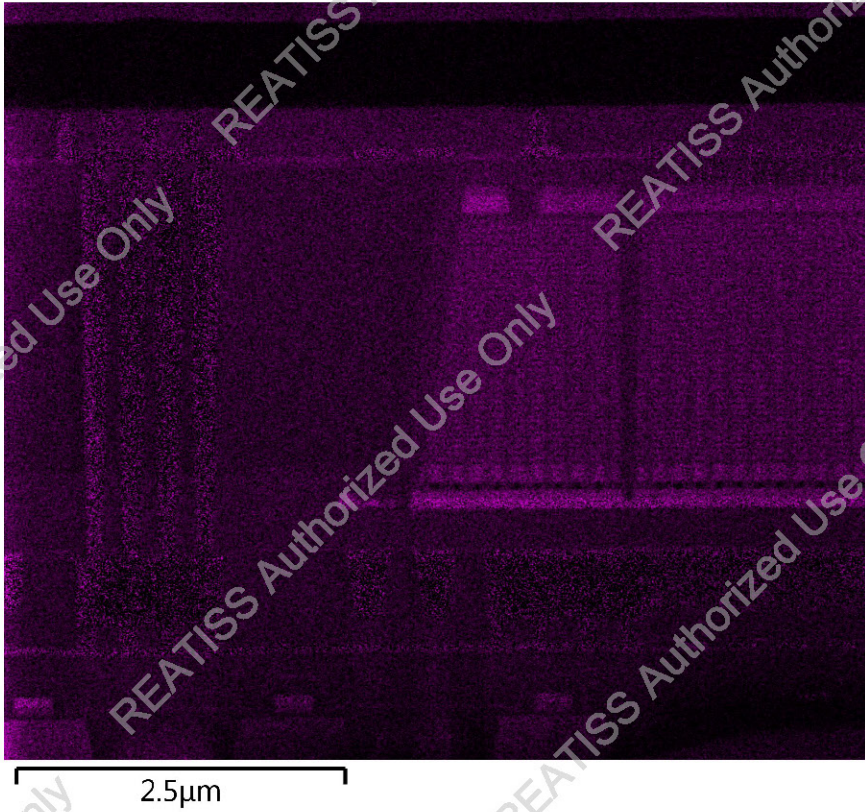


Figure 88. Silicon EDX map layer

O K series

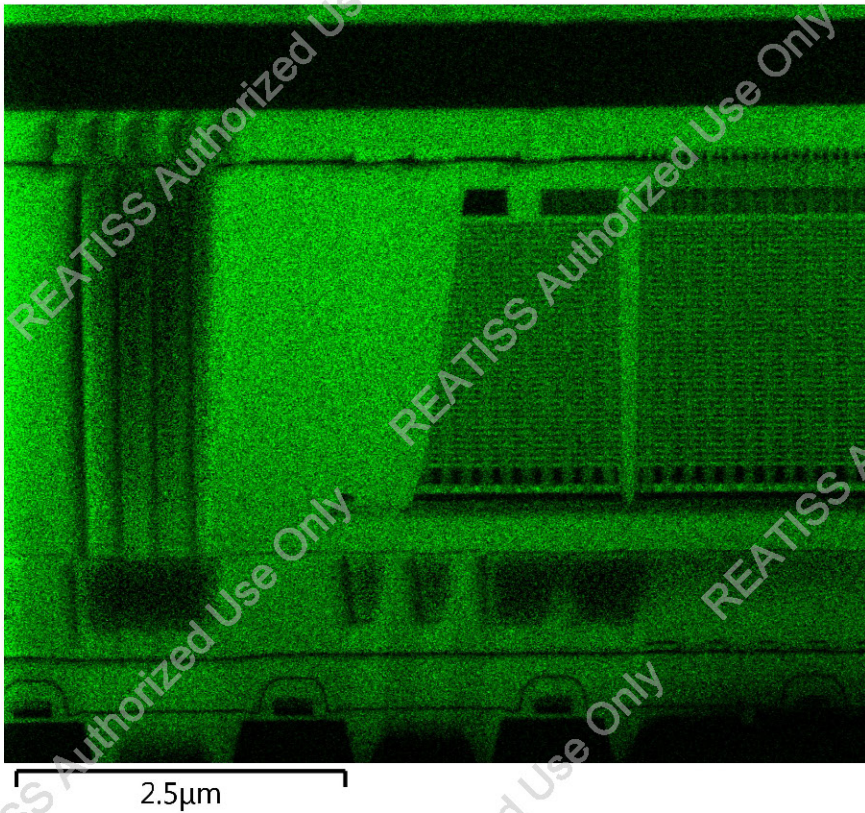


Figure 89. Oxygen EDX map layer

N K series

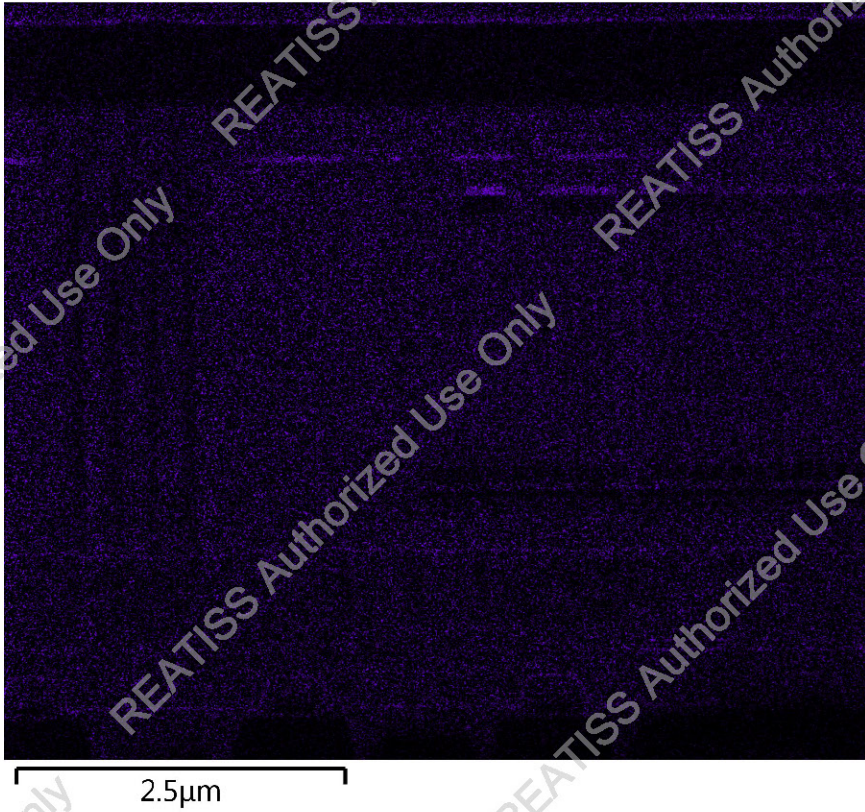


Figure 90. Nitrogen EDX map layer

P K series

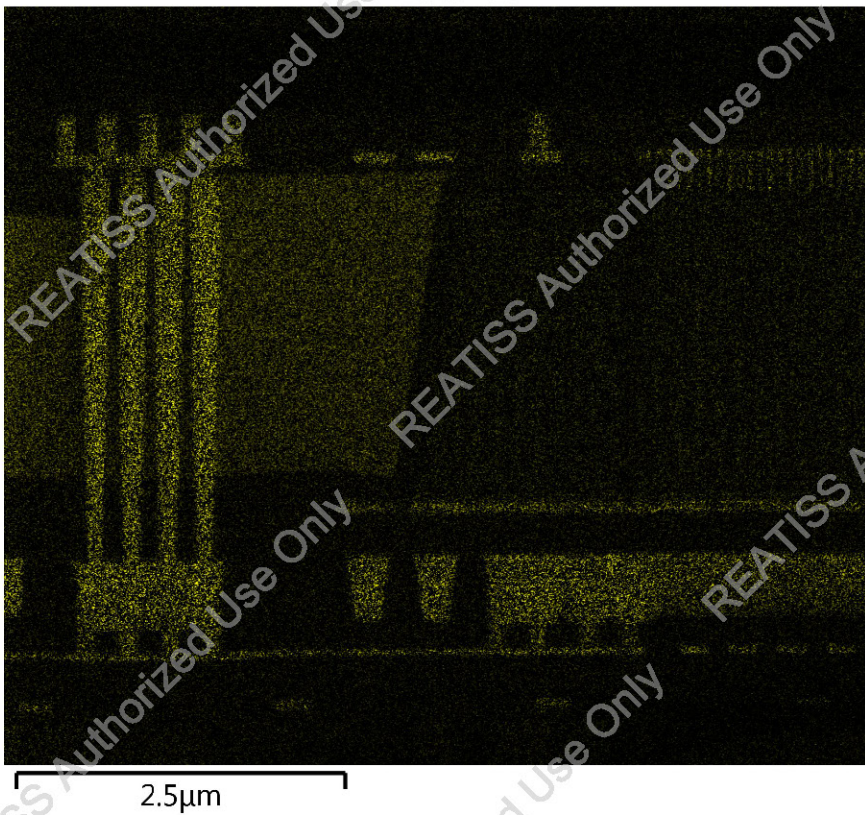


Figure 91. Phosphorus EDX map layer

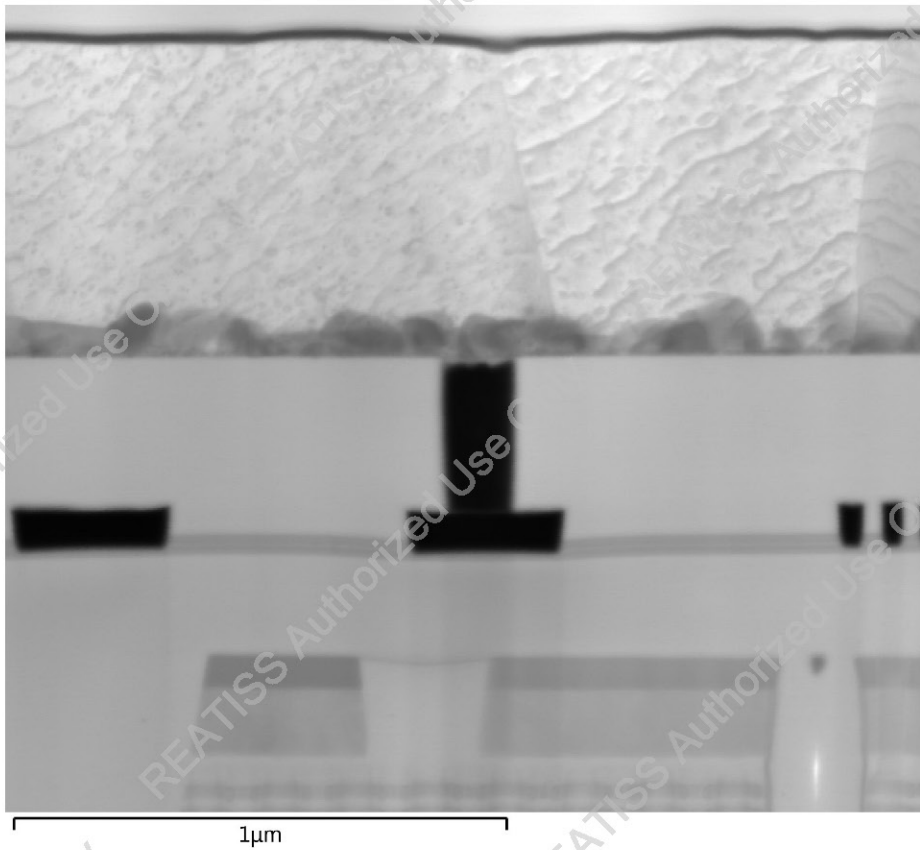


Figure 92. Al M4, W M3 lines, W via

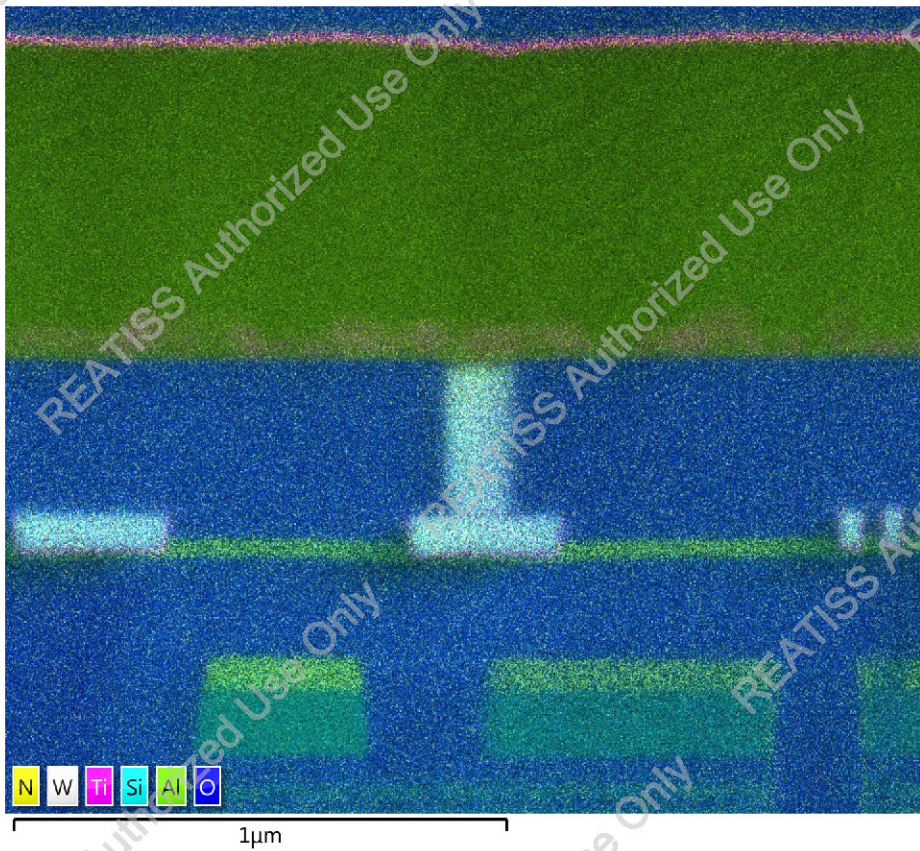


Figure 93. Layered EDX map of Al M4, W M3 lines, W via

Al K series

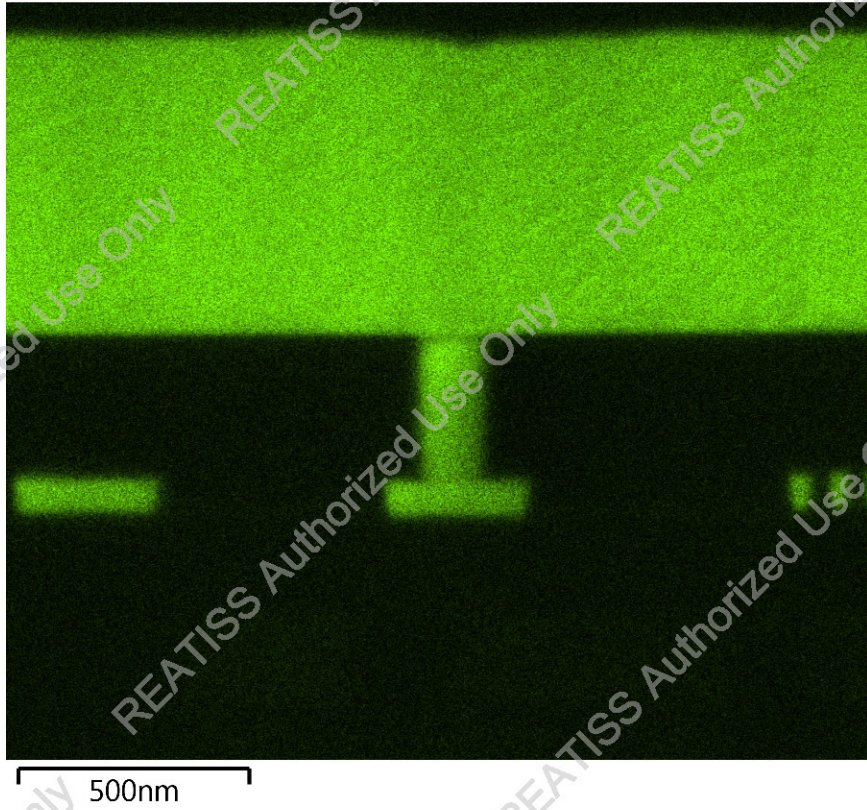


Figure 94. Aluminum EDX map layer

W L series

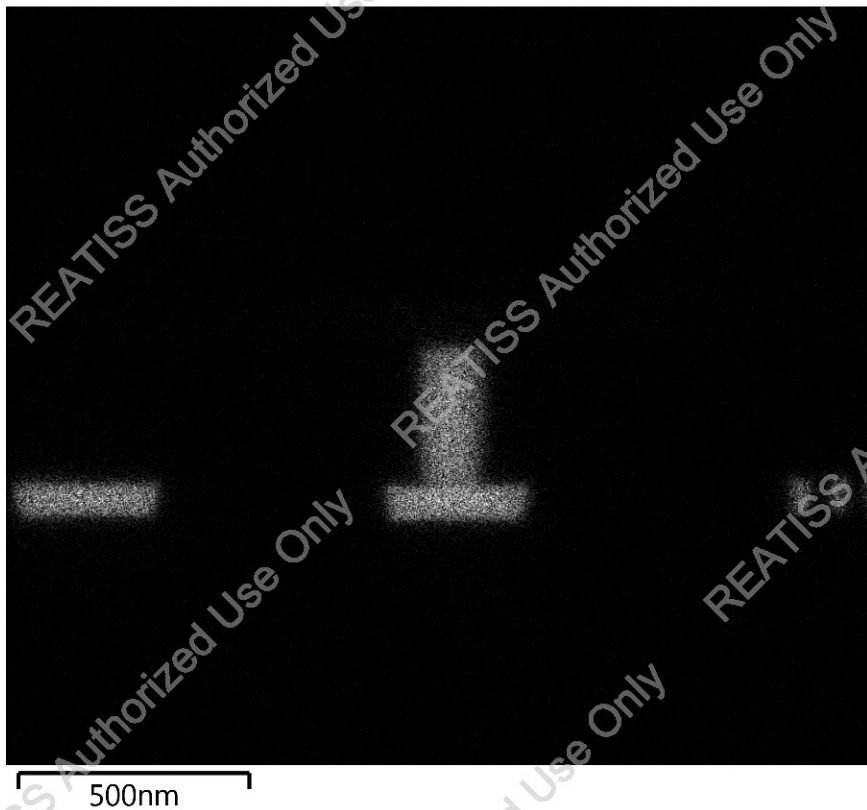


Figure 95. Tungsten EDX map layer

Ti K series

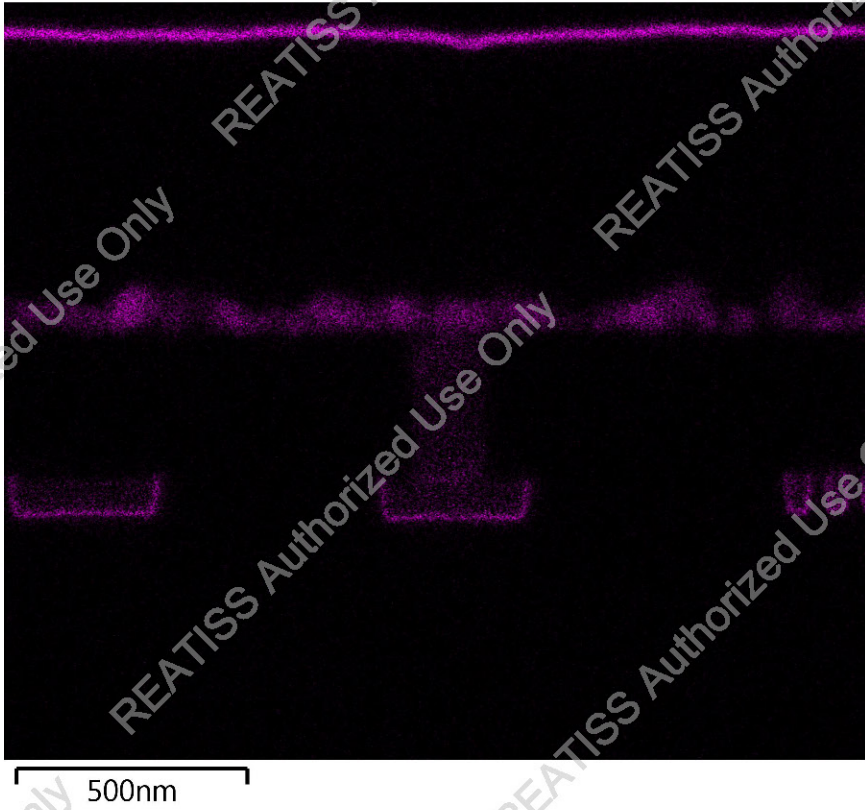


Figure 96. Titanium EDX map layer

Si K series

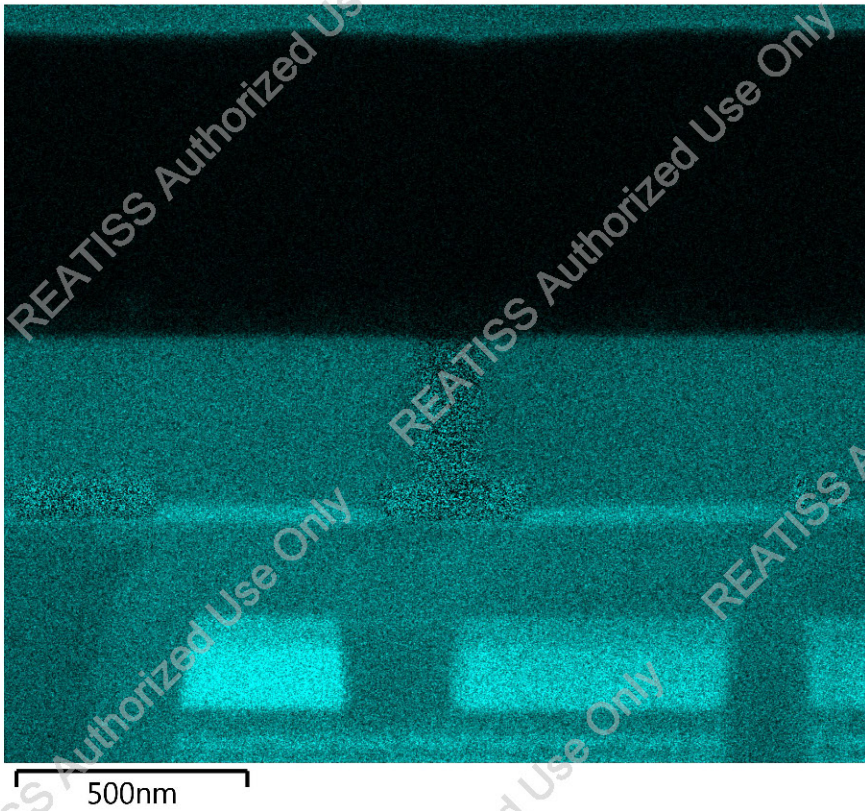


Figure 97. Silicon EDX map layer

O K series

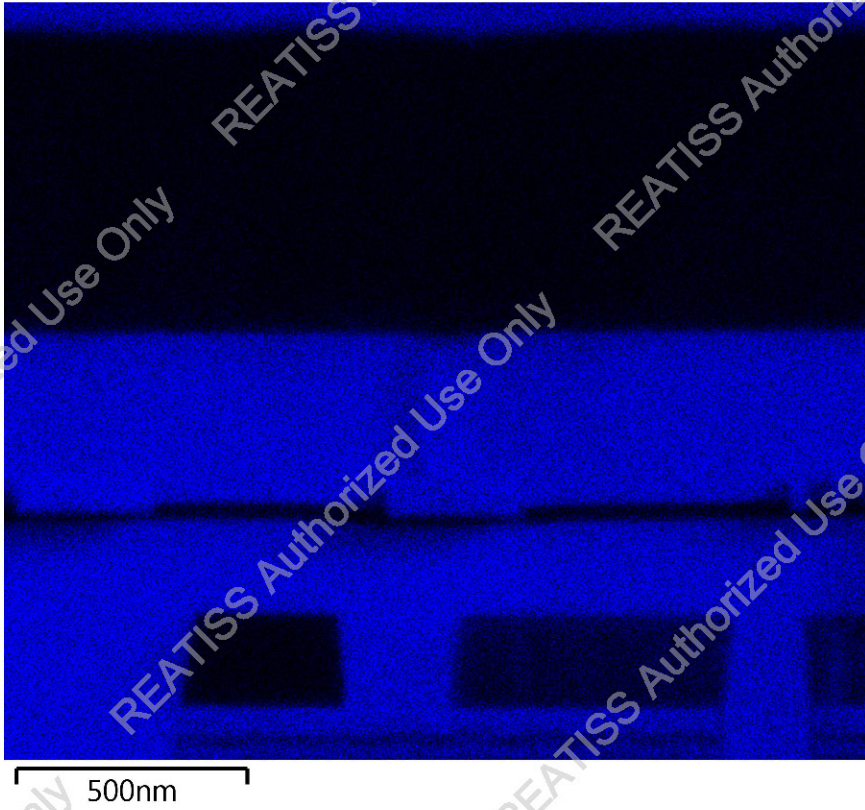


Figure 98. Oxygen EDX map layer

N K series

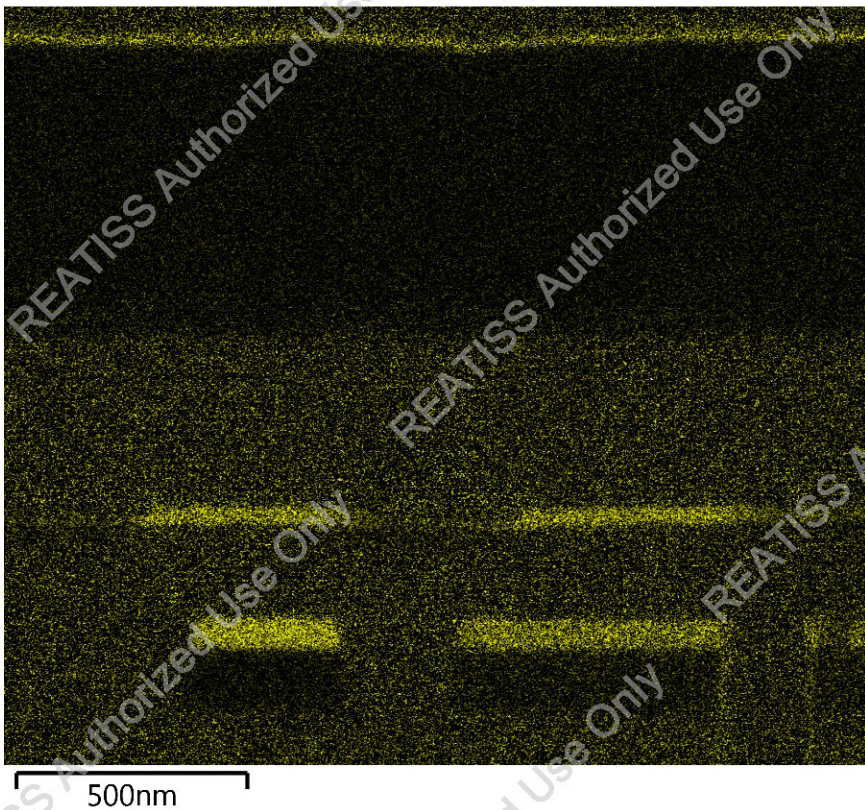


Figure 99. Nitrogen EDX map layer

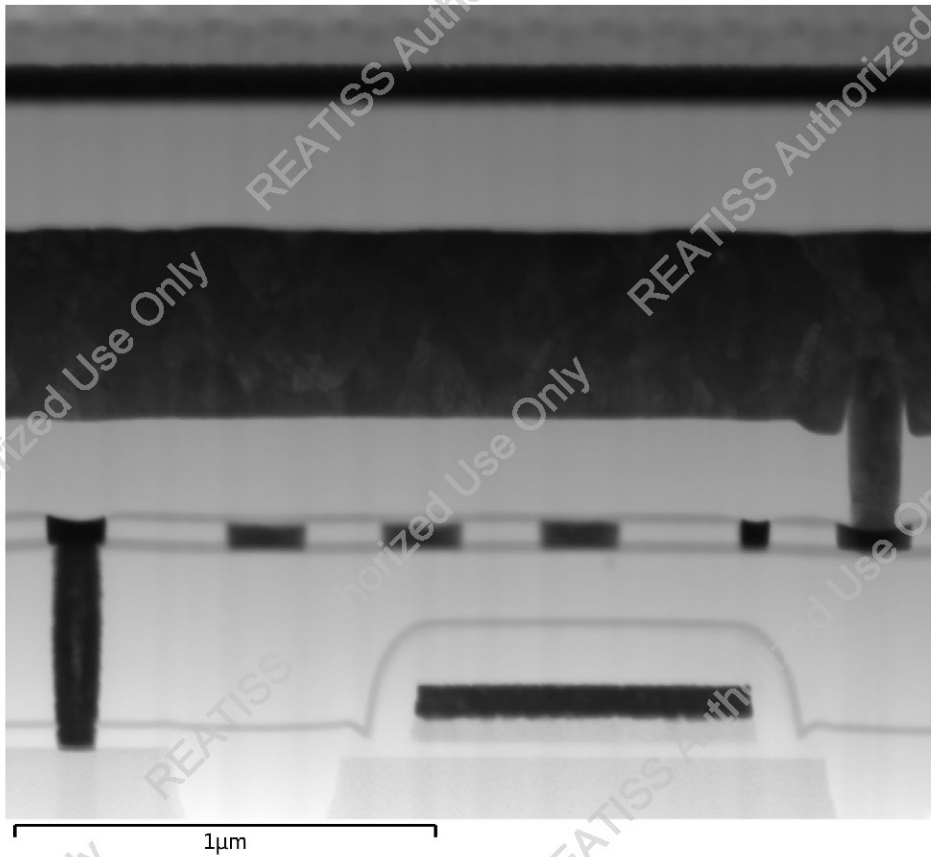


Figure 100. W M1 , M2 lines, W via, W contact, MOS gate

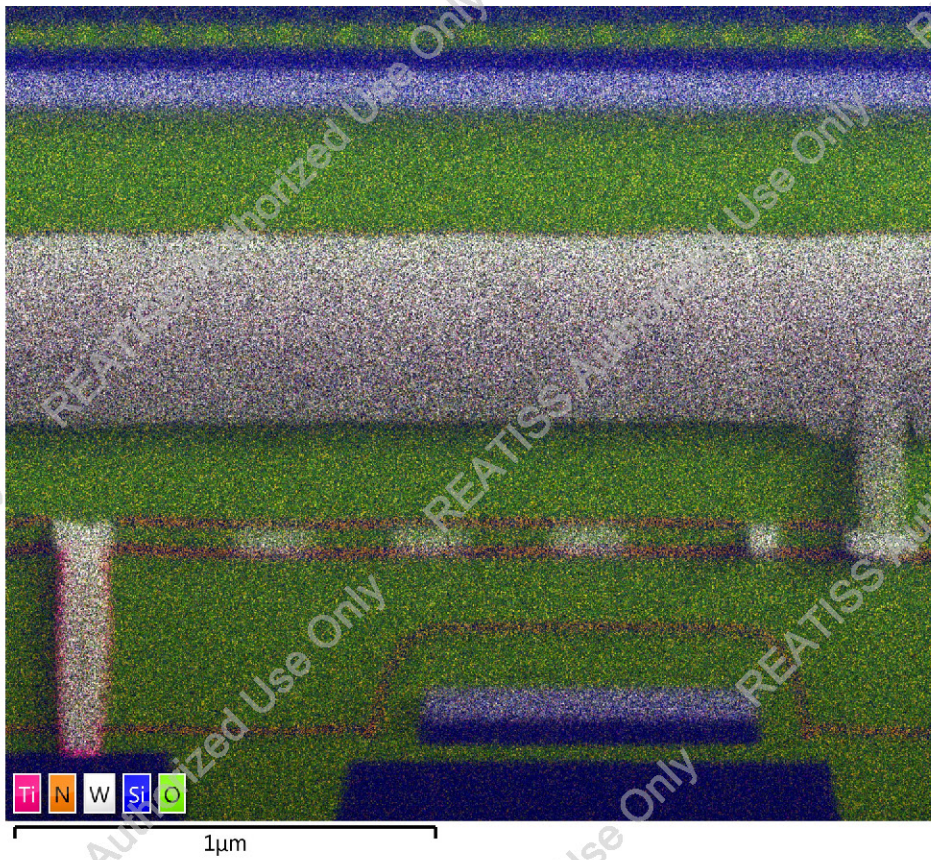


Figure 101. Layered EDX map of W M1 , M2 lines, W via, W contact, MOS gate

W L series

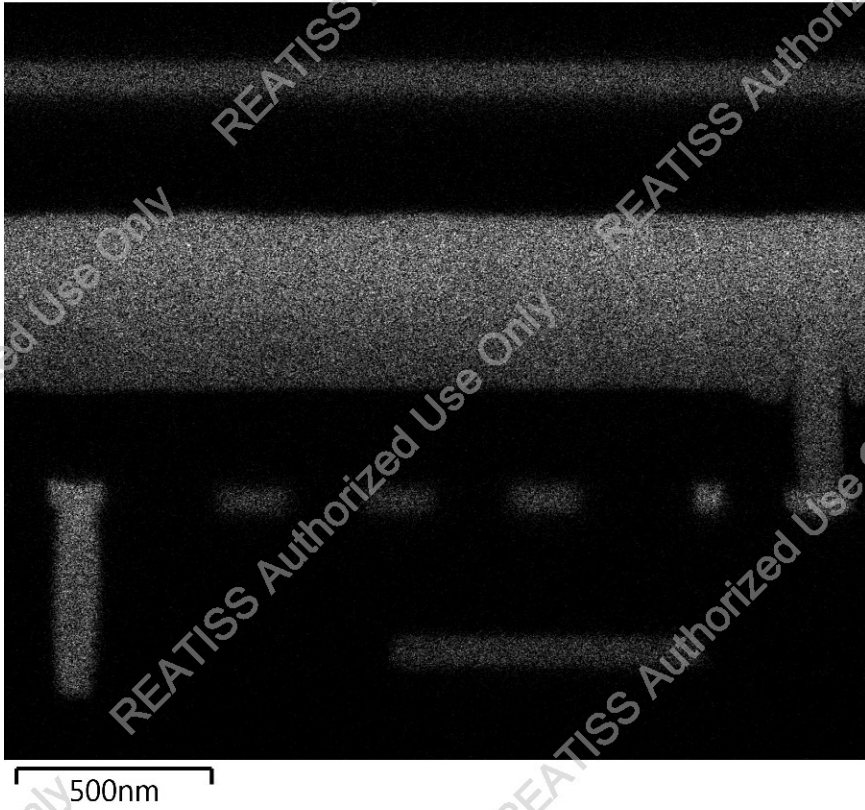


Figure 102. Tungsten EDX map layer

Ti K series

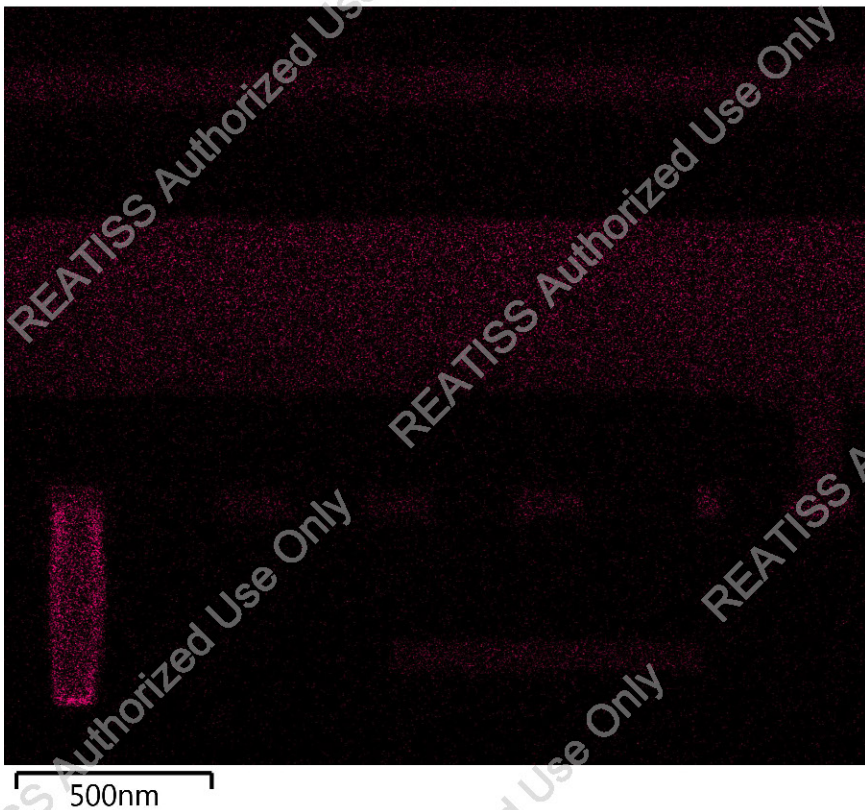


Figure 103. Titanium EDX map layer

Si K series

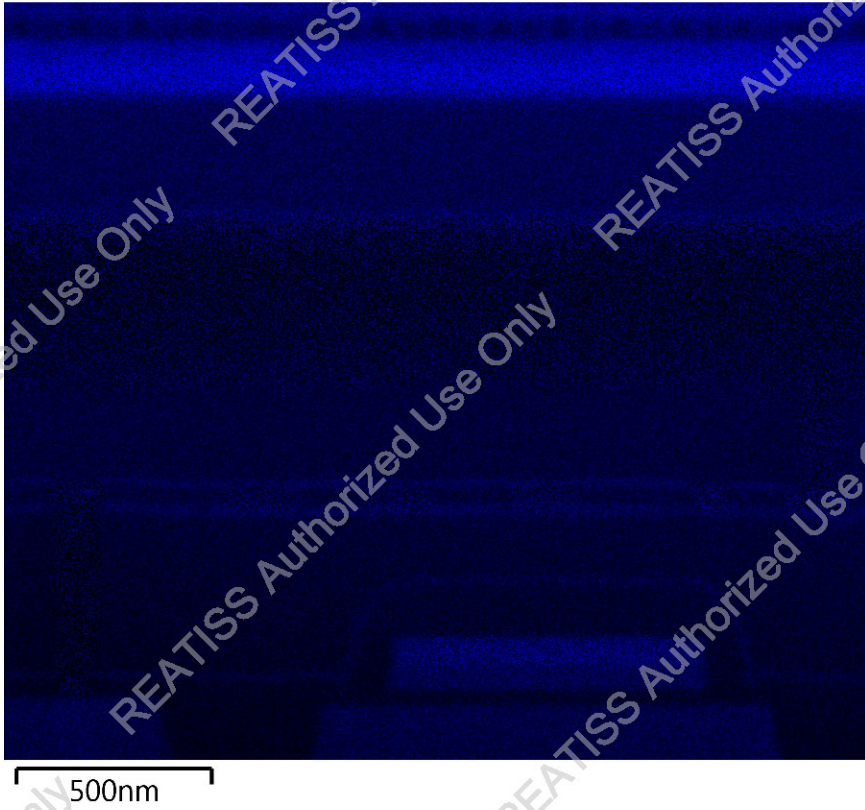


Figure 104. Silicon EDX map layer

O K series

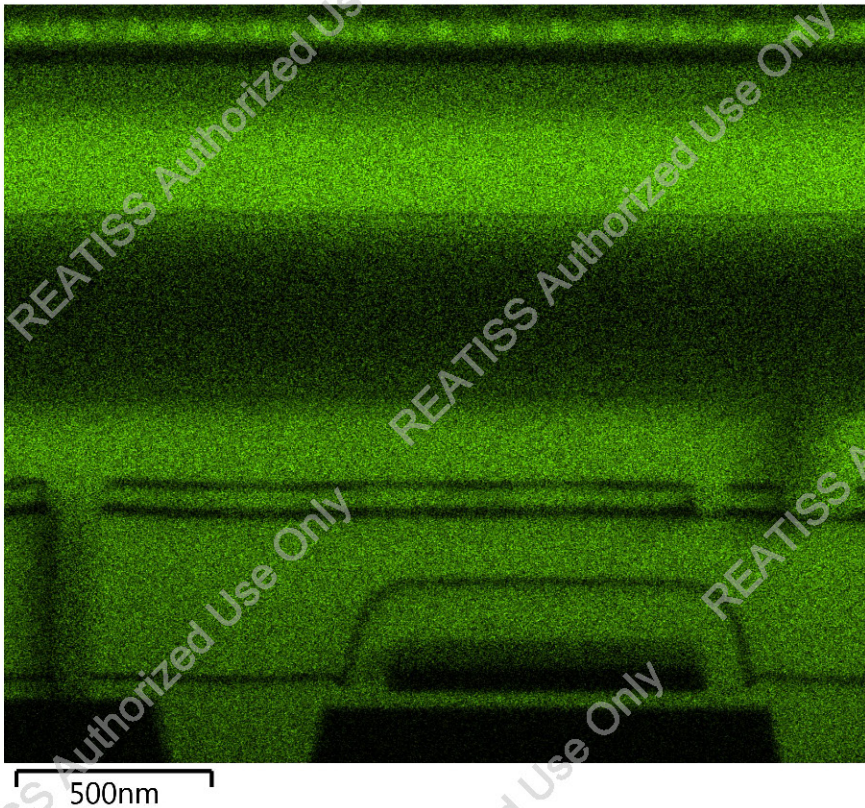


Figure 105. Oxygen EDX map layer

N K series

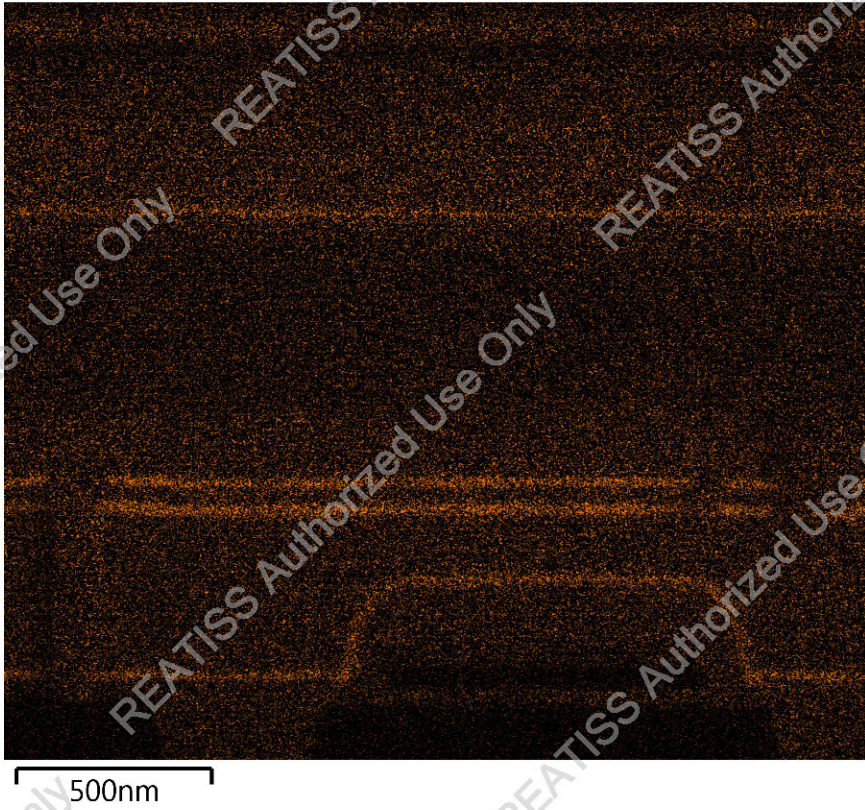


Figure 106. Nitrogen EDX map layer

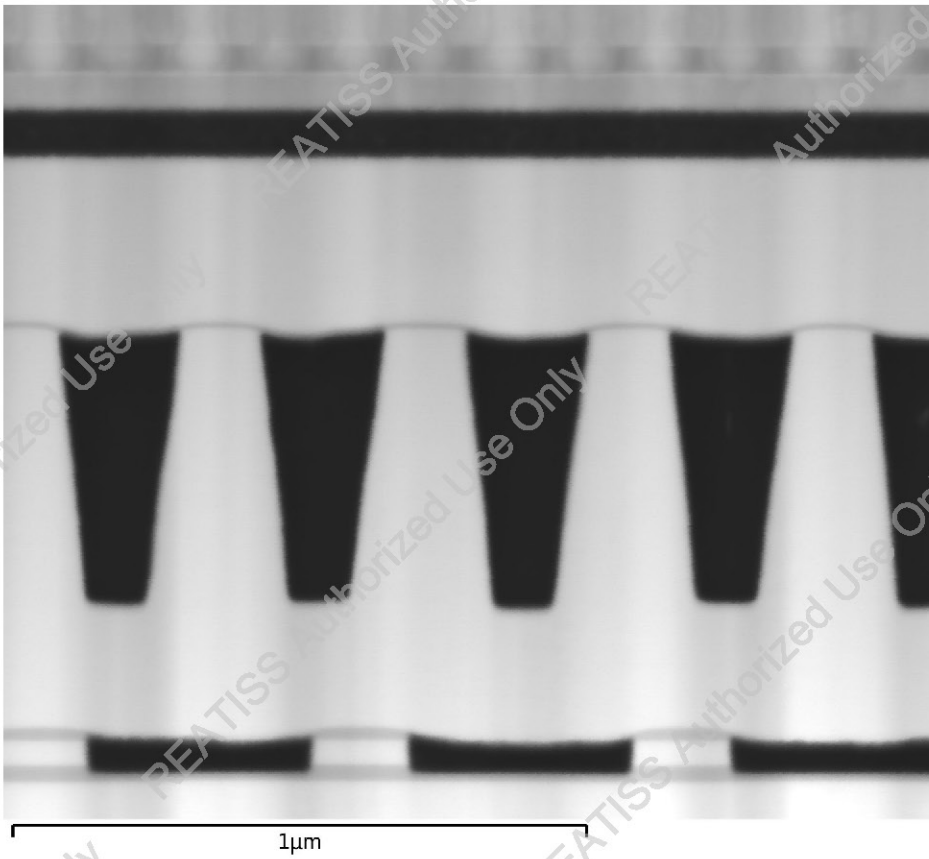


Figure 107. W M1, M2 lines

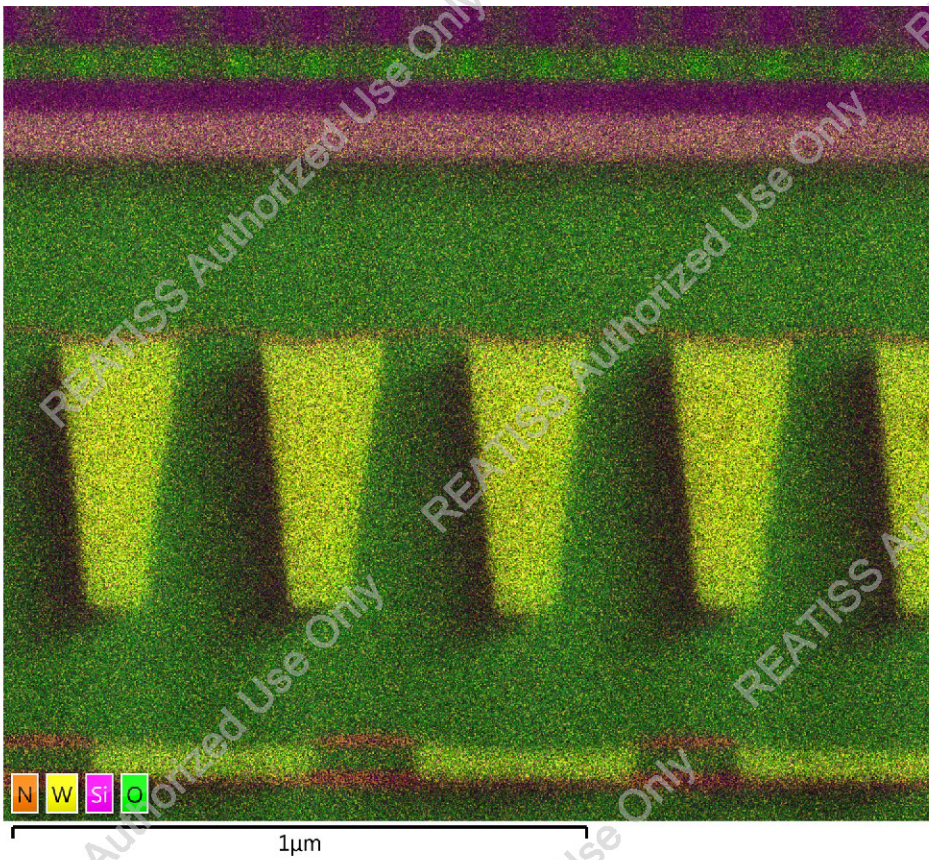


Figure 108. Layered EDX map of W M1, M2 lines

W L series

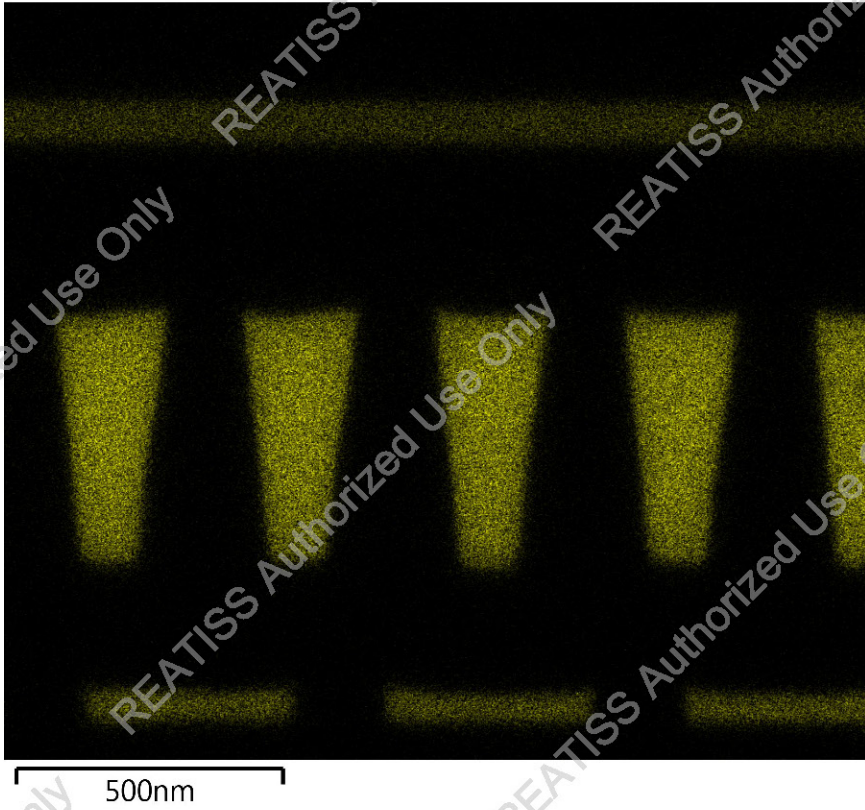


Figure 109. Tungsten EDX map layer

Si K series

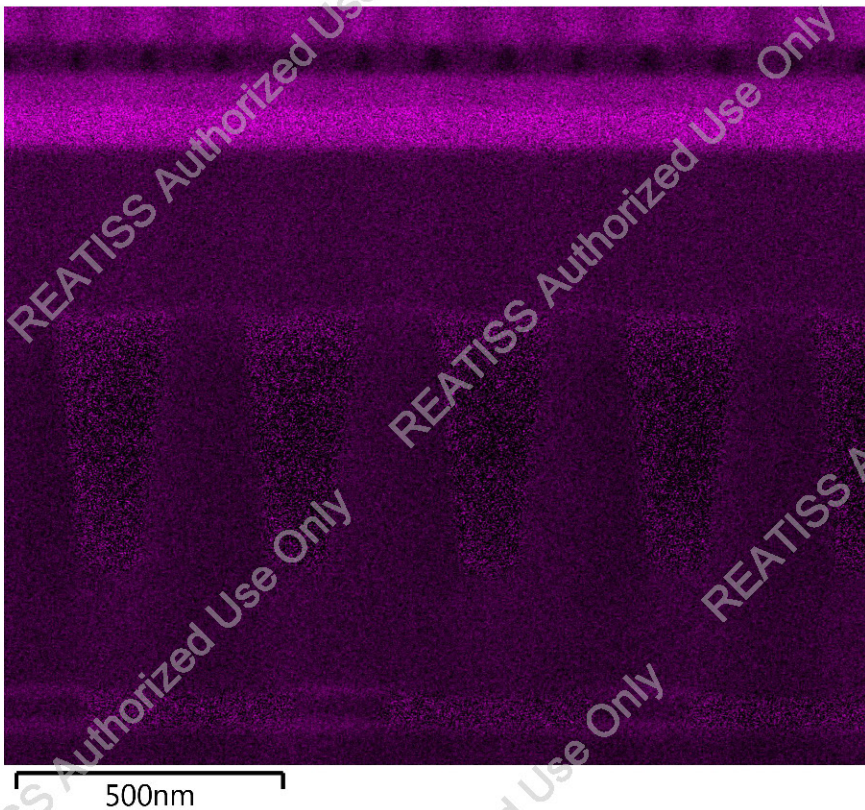


Figure 110. Silicon EDX map layer

O K series

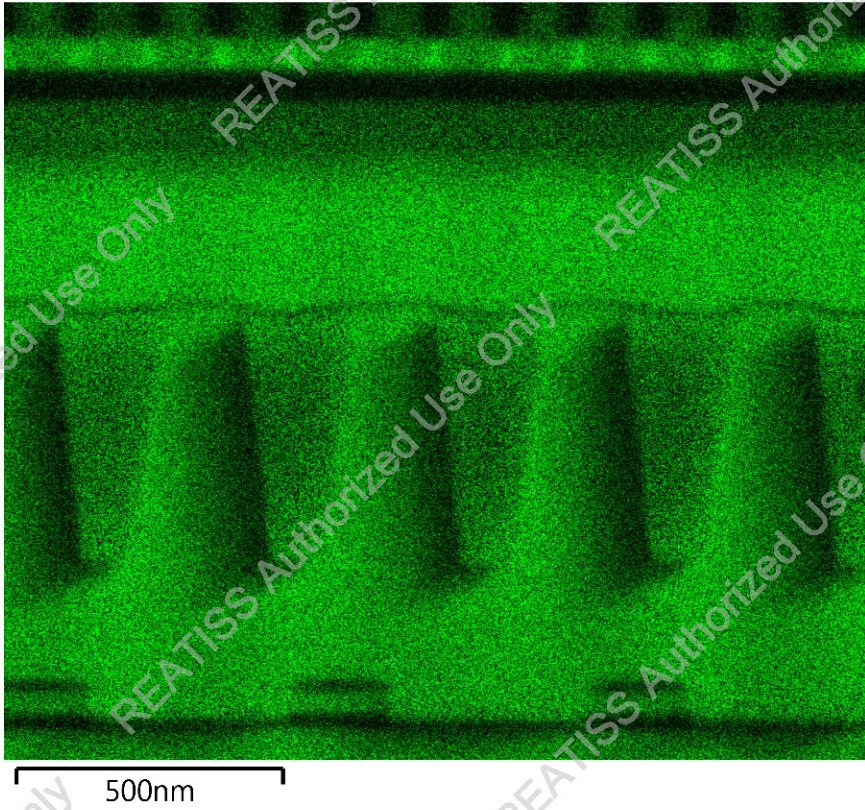


Figure 111. Oxygen EDX map layer

N K series

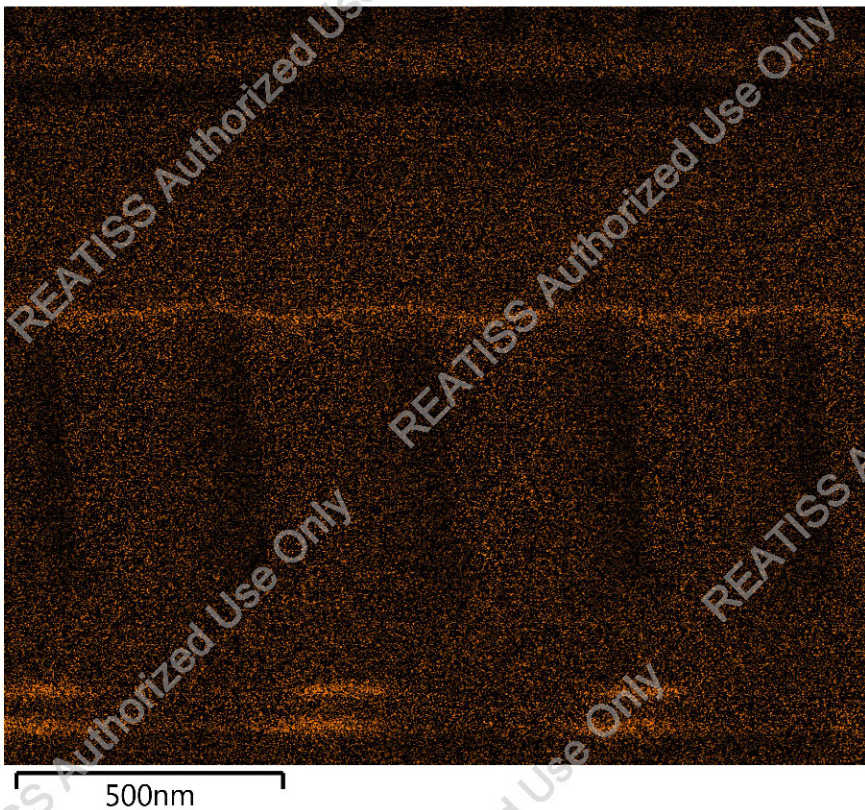


Figure 112. Nitrogen EDX map layer

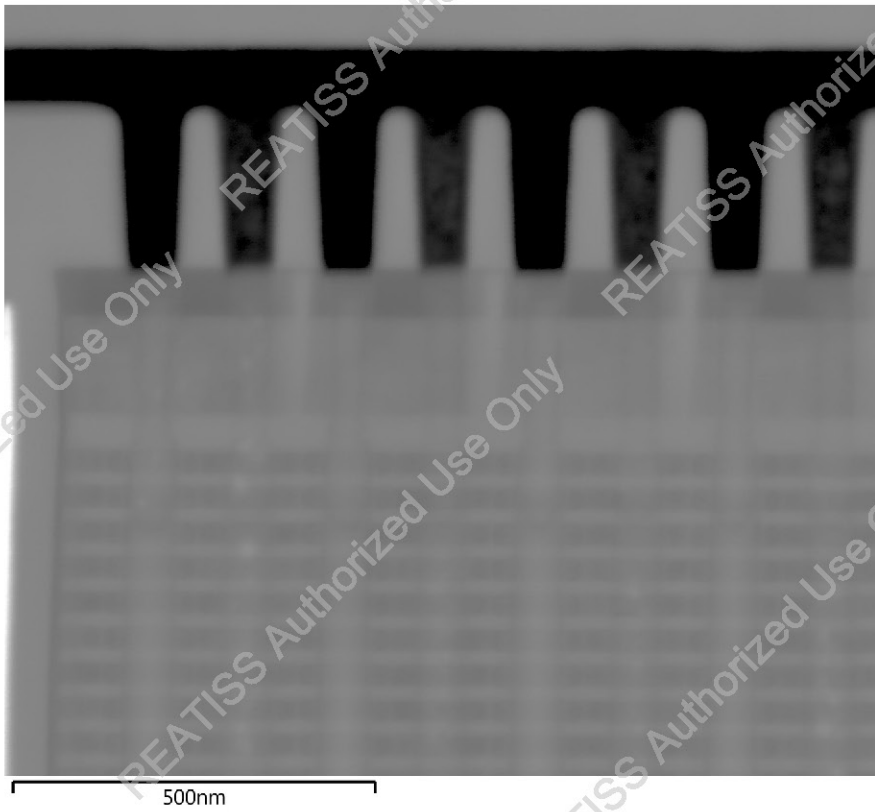


Figure 113. W M3 line, W vias

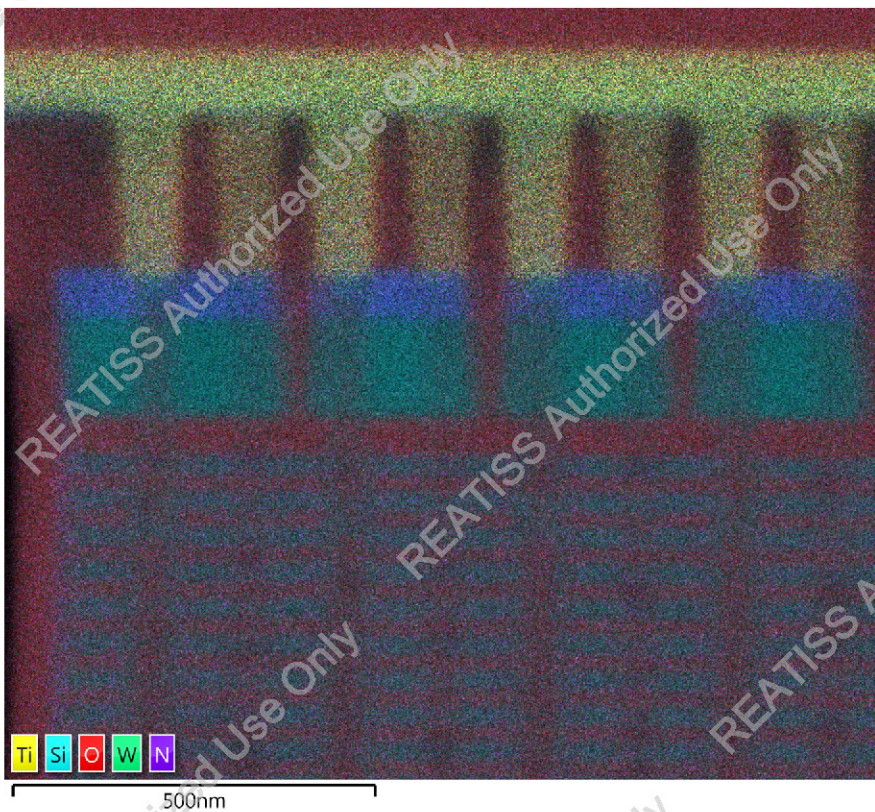


Figure 114. Layered EDX map of W M3 line, W vias

W L series

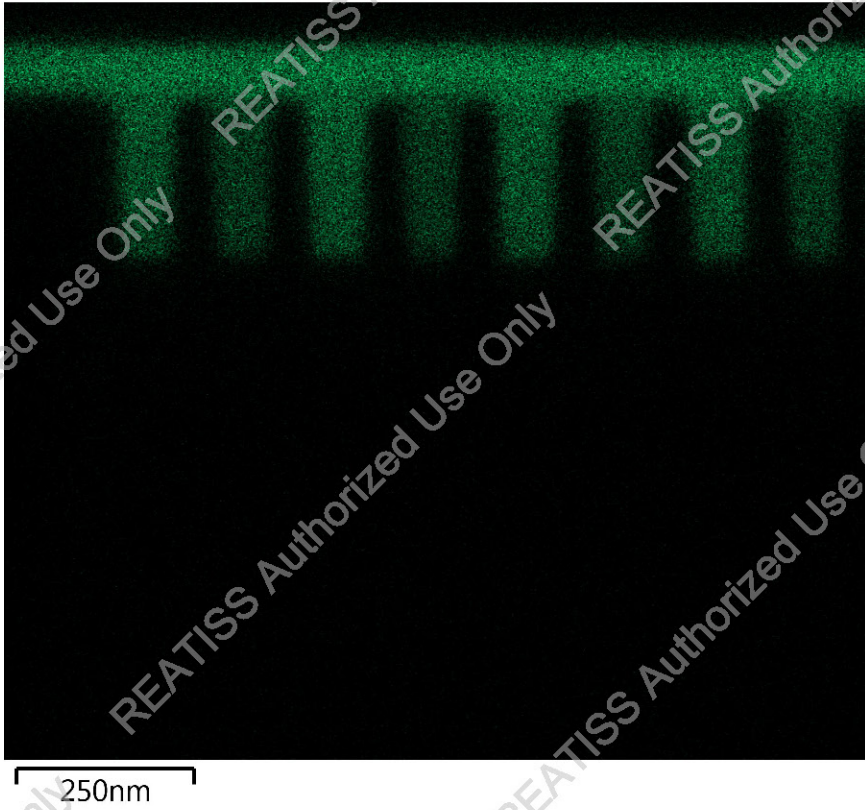


Figure 115. Tungsten EDX map layer

Ti K series

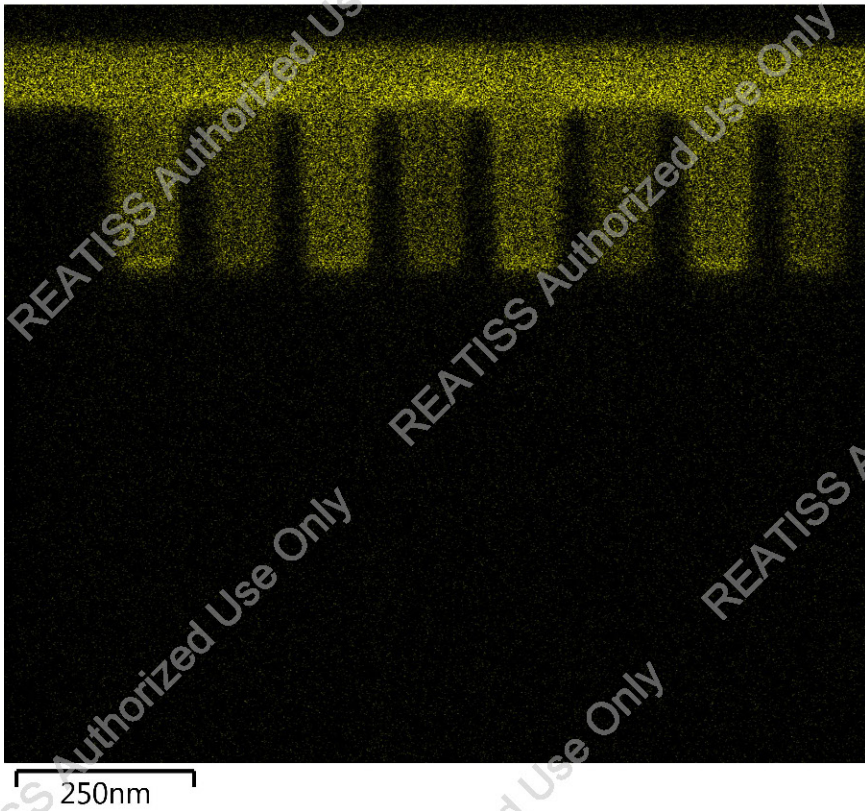


Figure 116. Titanium EDX map layer

Si K series

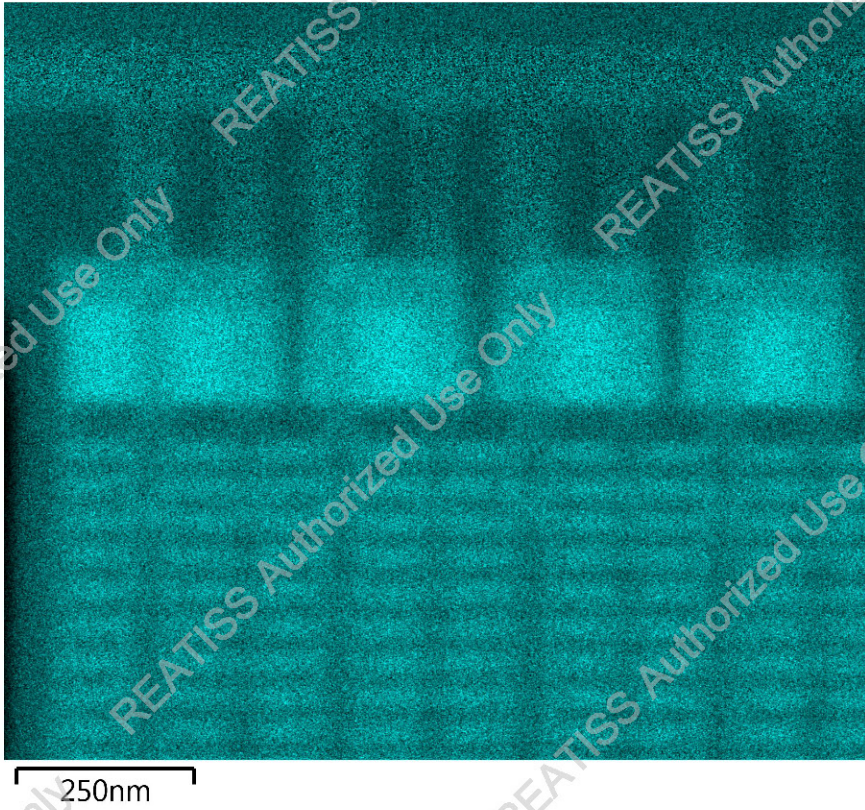


Figure 117. Silicon EDX map layer

O K series

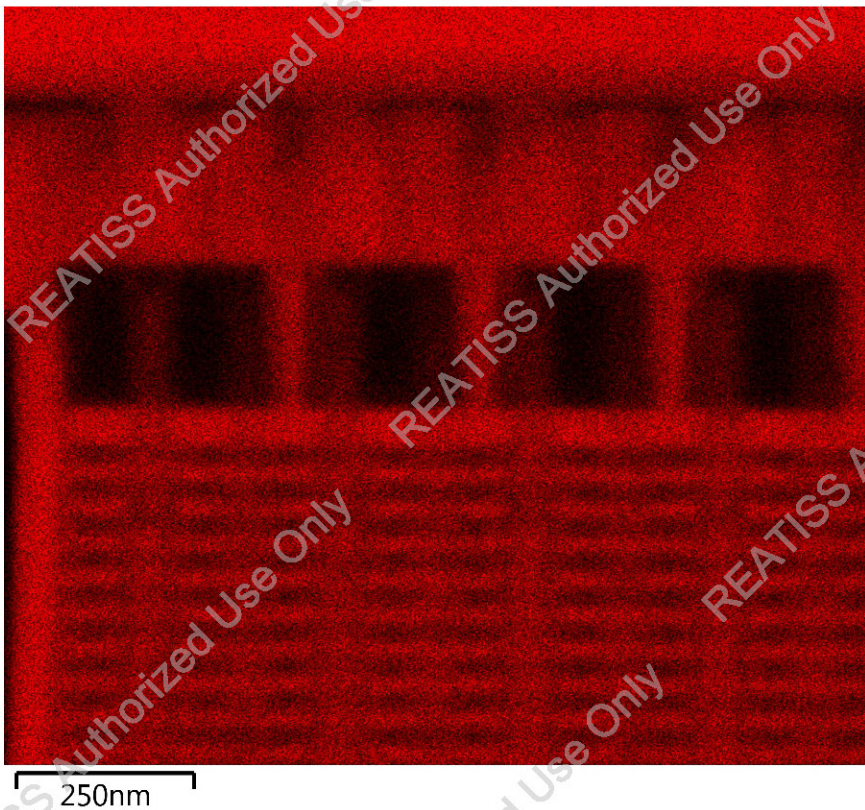


Figure 118. Oxygen EDX map layer

N K series

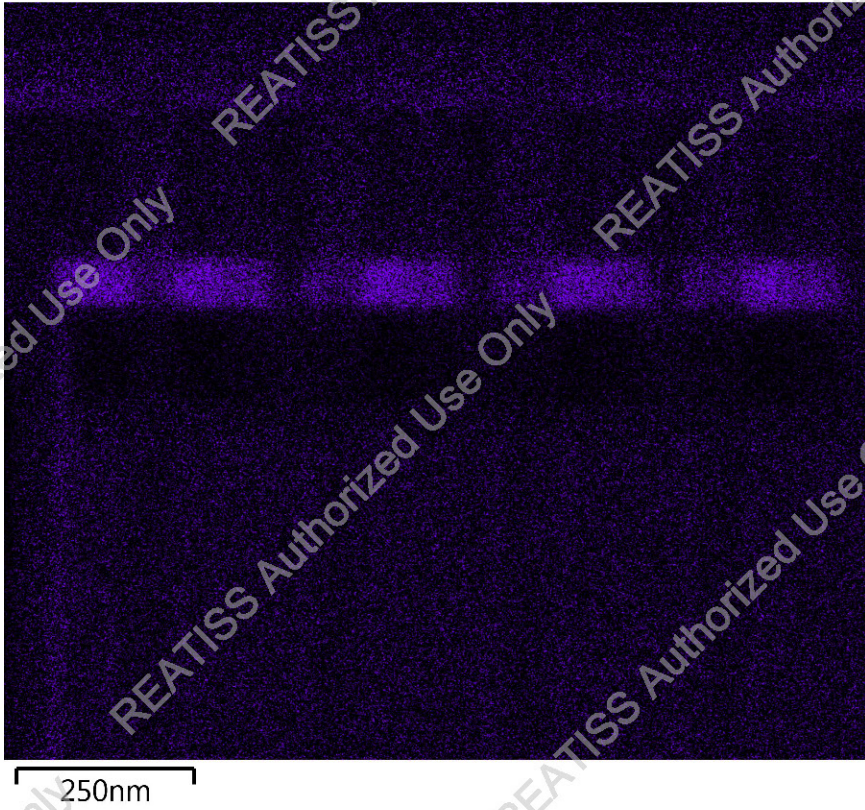


Figure 119. Nitrogen EDX map layer

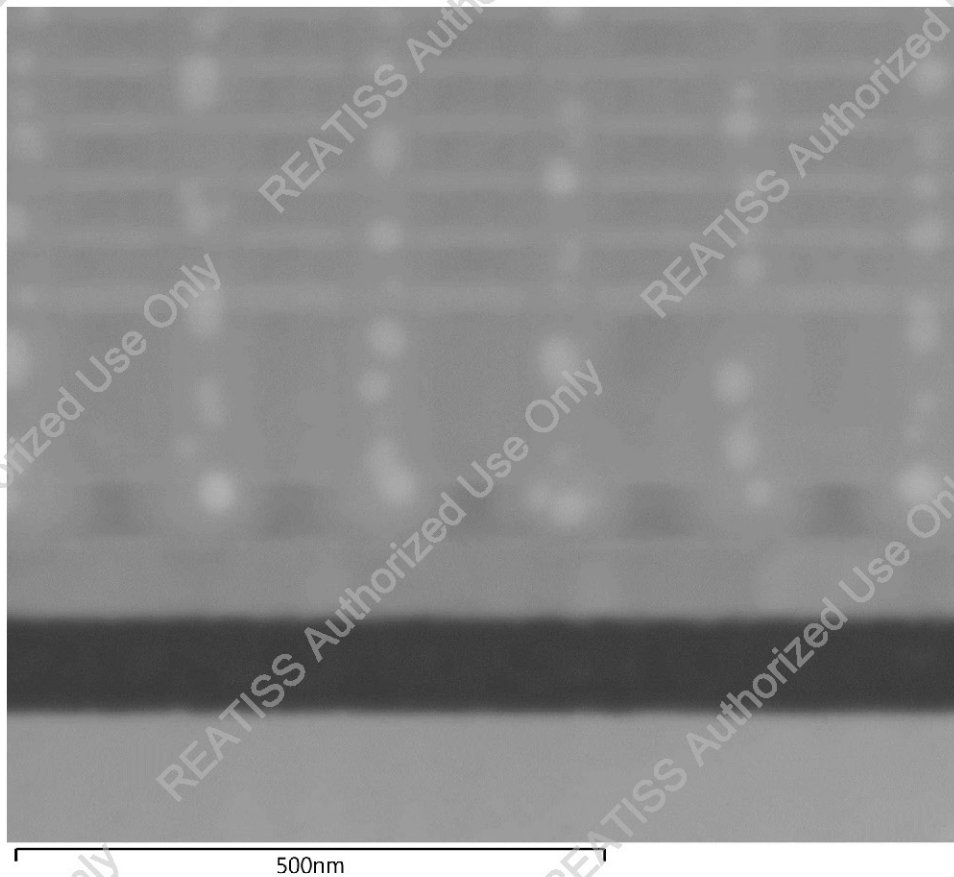


Figure 120. NAND array bottom, select gate



Figure 121. Layered EDX map of NAND array bottom, select gate

W L series

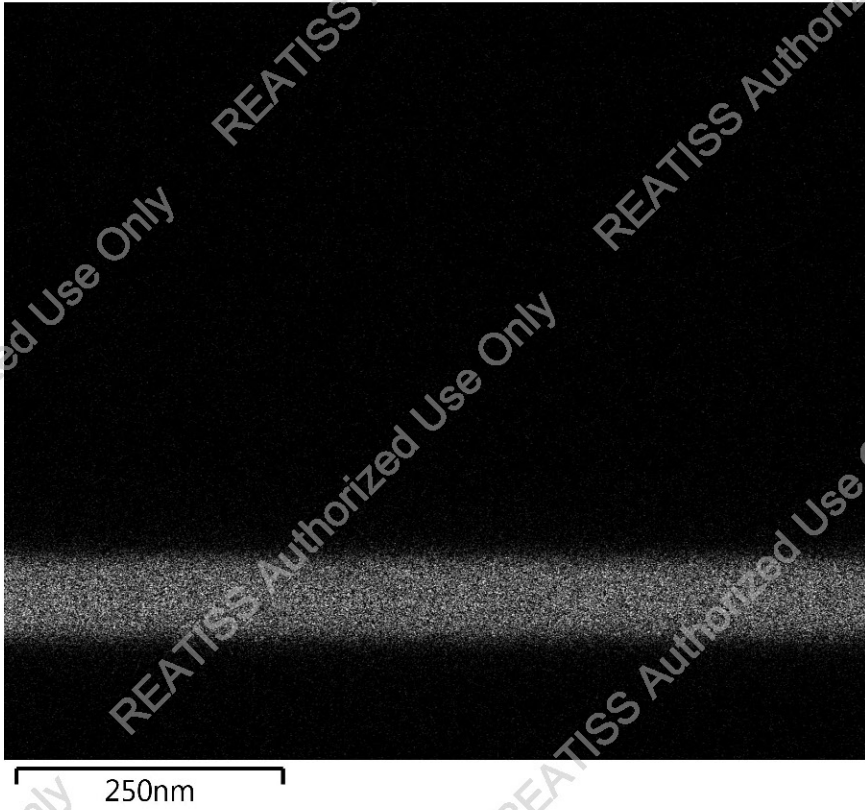


Figure 122. Tungsten EDX map layer

Al K series

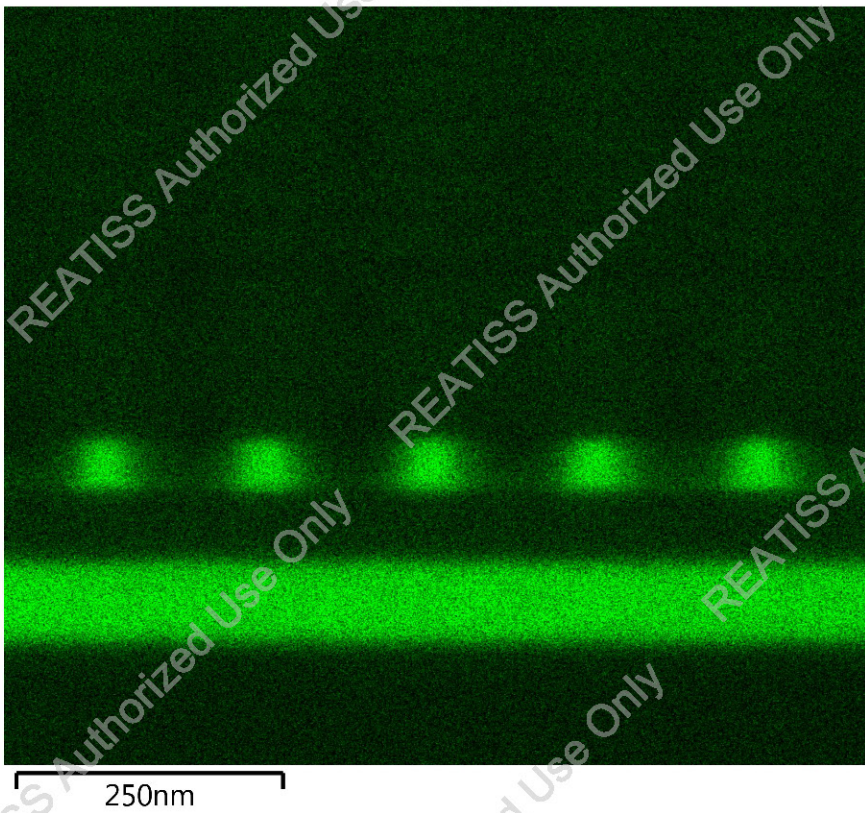


Figure 123. Aluminum EDX map layer

Si K series

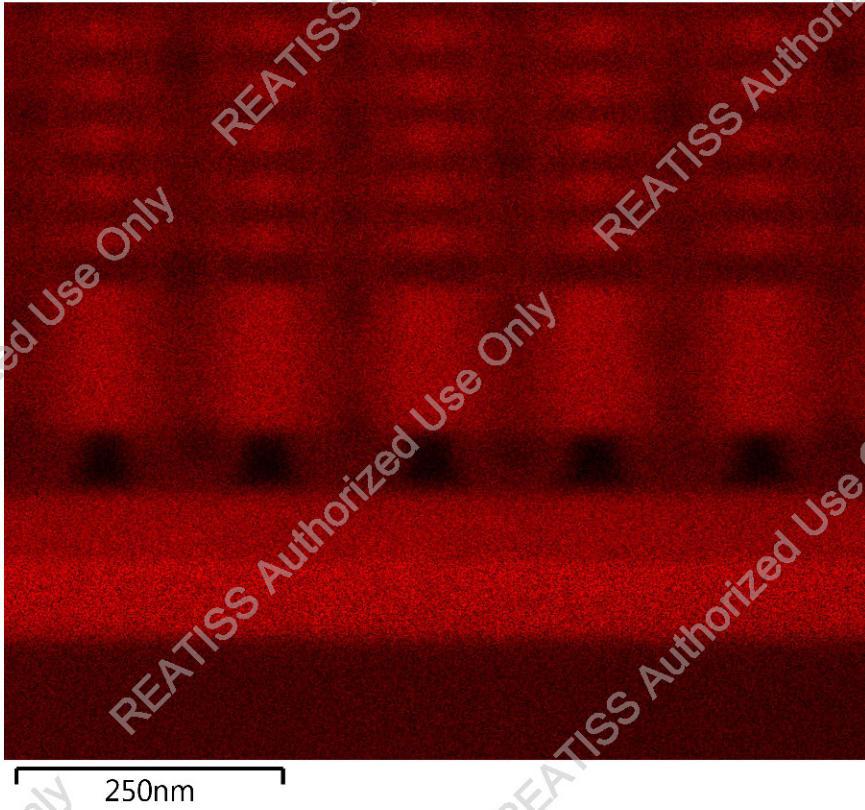


Figure 124. Silicon EDX map layer

O K series

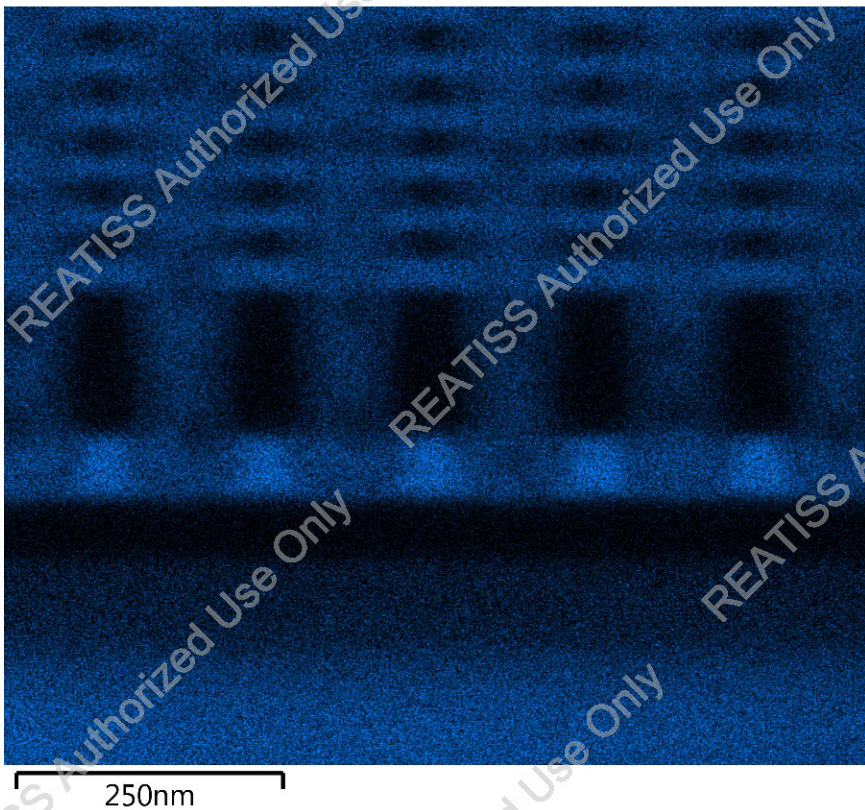


Figure 125. Oxygen EDX map layer

P K series

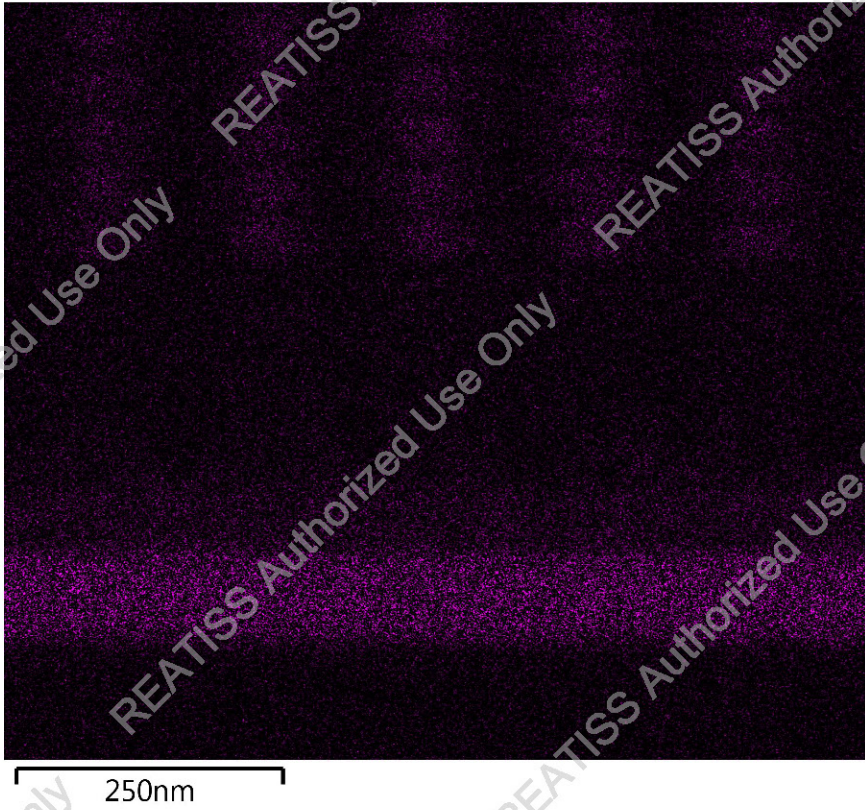


Figure 126. Phosphorus EDX map layer

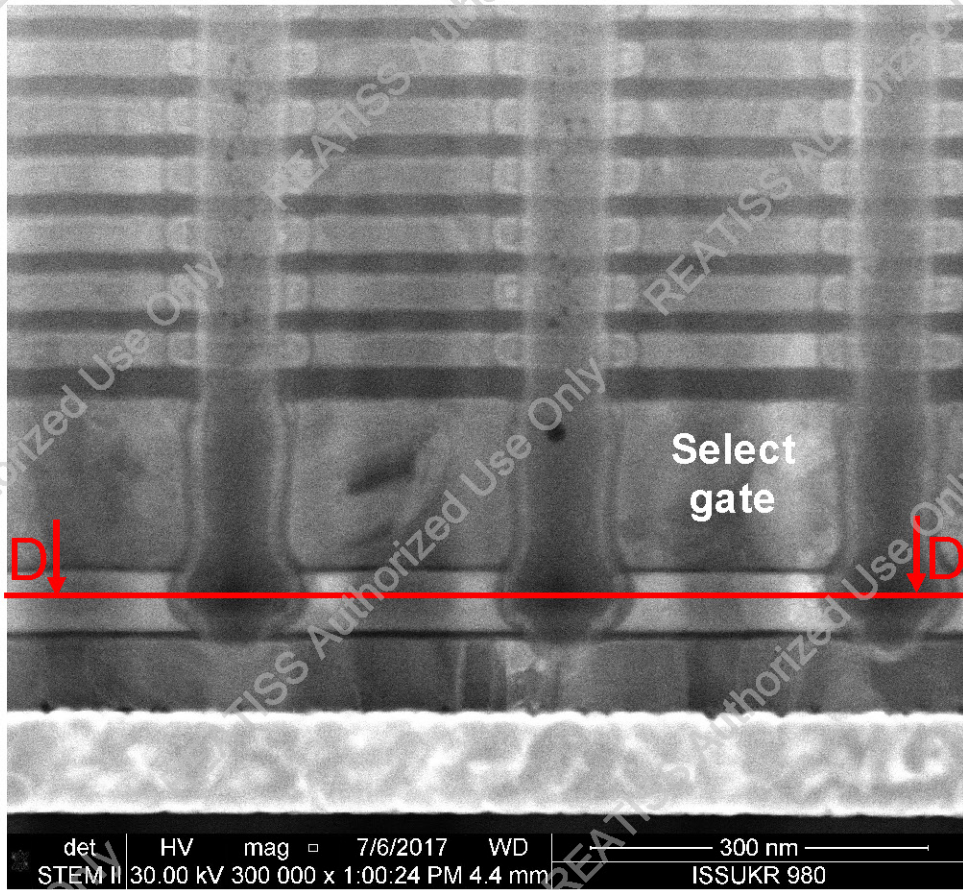


Figure 127. NAND cells array bottom with section D-D marked

Following figures show structures of the section D-D

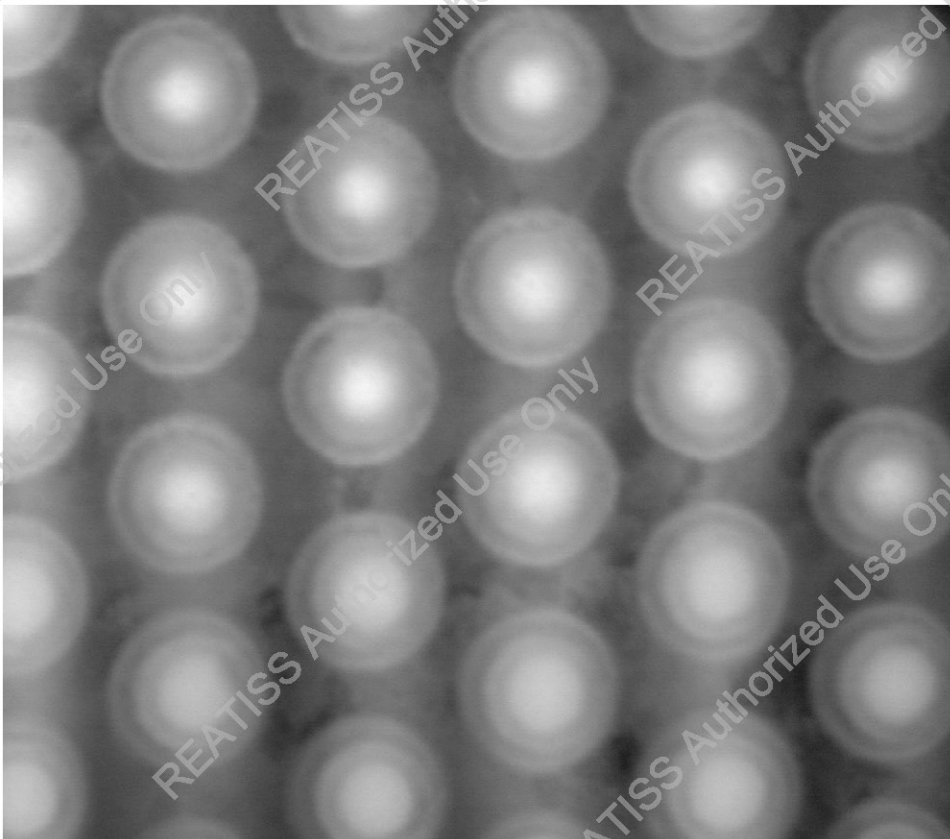


Figure 128. Channels connection (section D-D)

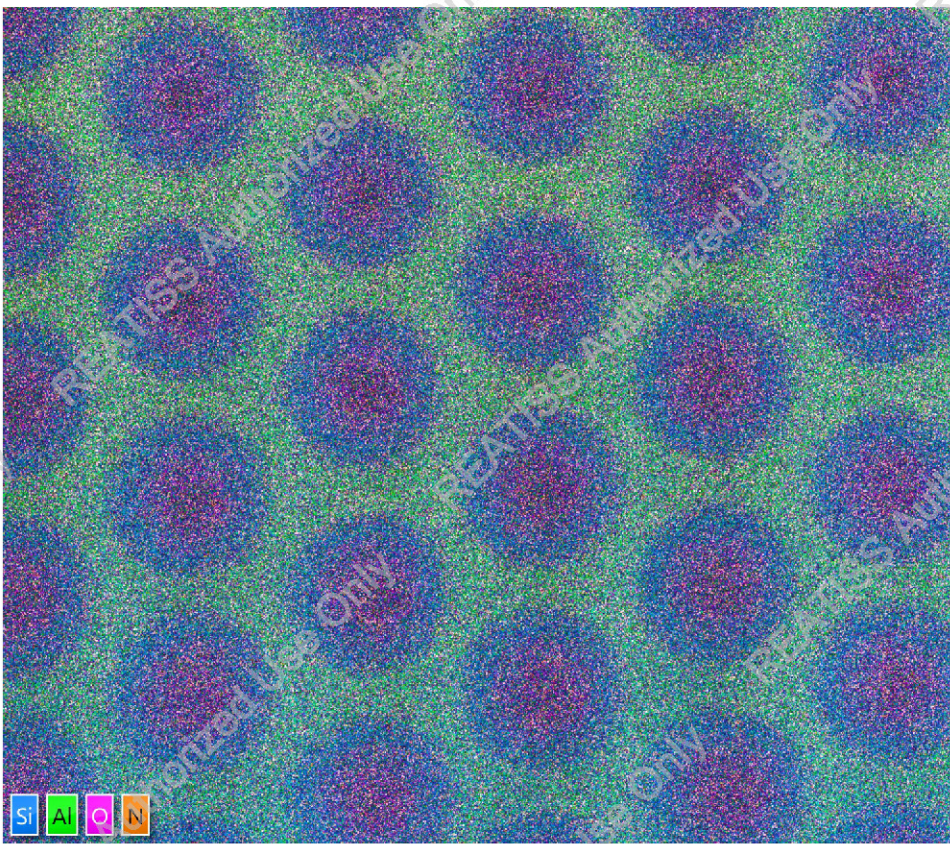


Figure 129. Layered EDX map of channels connection

Al K series

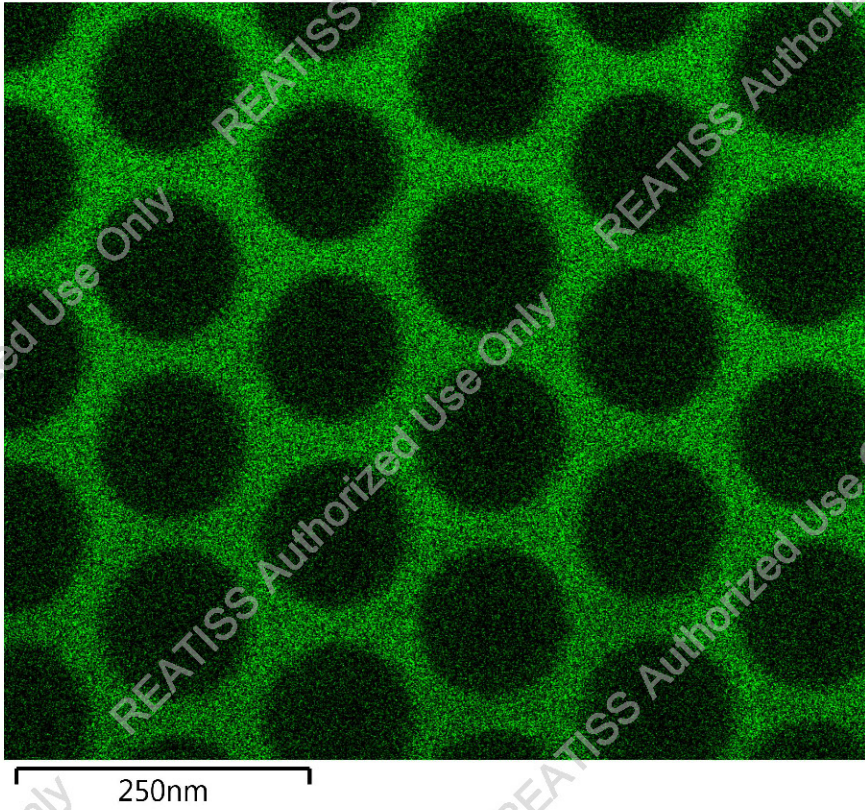


Figure 130. Aluminum EDX map layer

Si K series

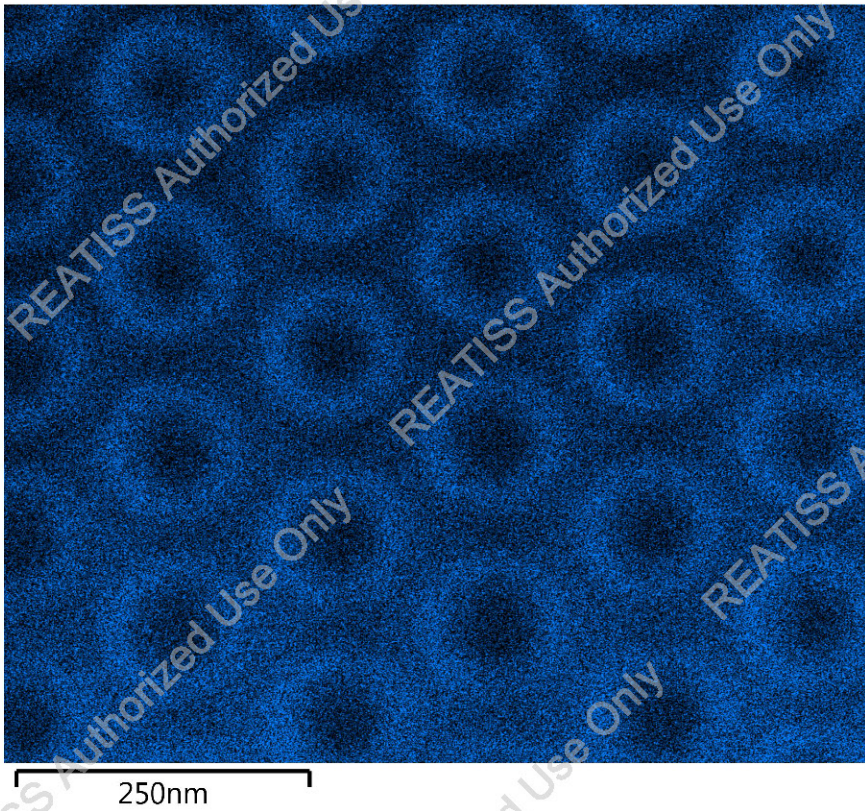


Figure 131. Silicon EDX map layer

O K series



Figure 132. Oxygen EDX map layer

N K series



Figure 133. Nitrogen EDX map layer

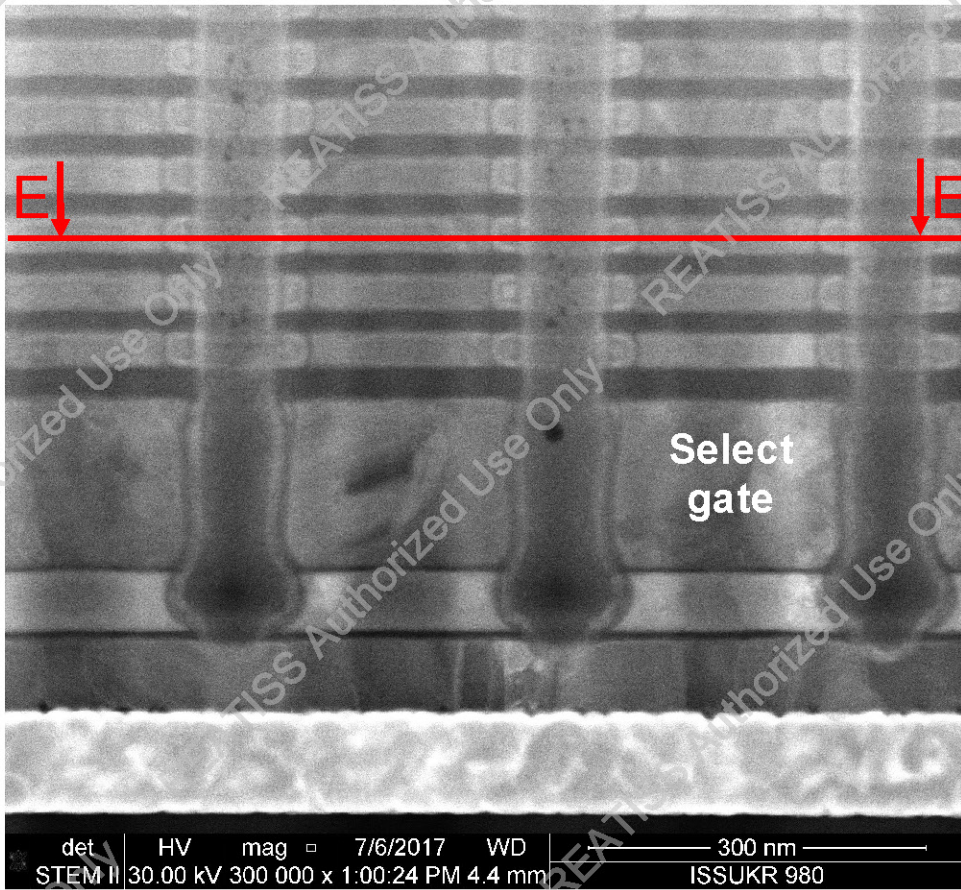


Figure 134. NAND cells array bottom with section E-E marked

Following figures show structures of the section E-E

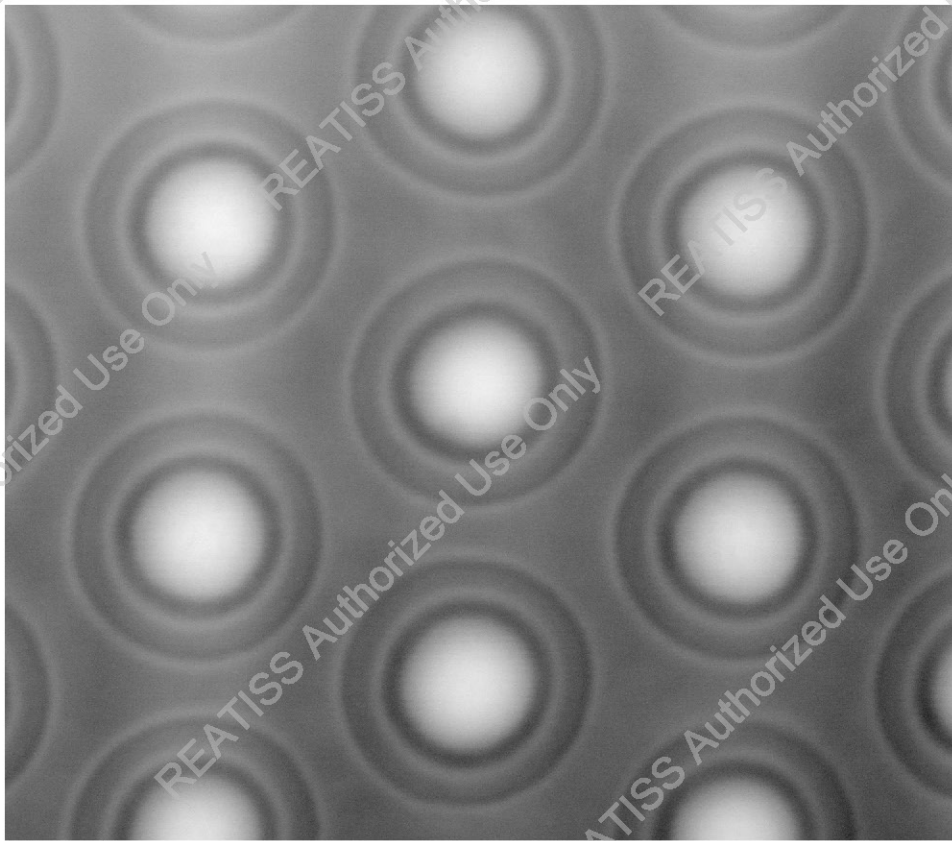


Figure 135. Memory cells top down (section E-E)

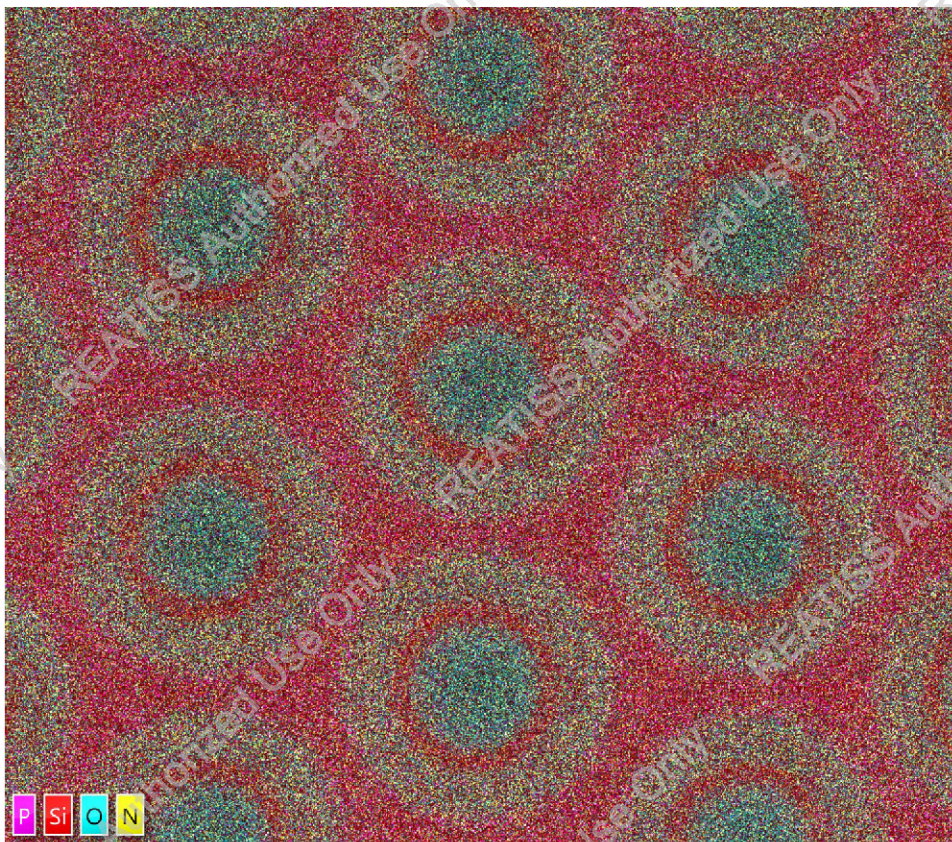


Figure 136. Layered EDX map of memory cells top down

Si K series

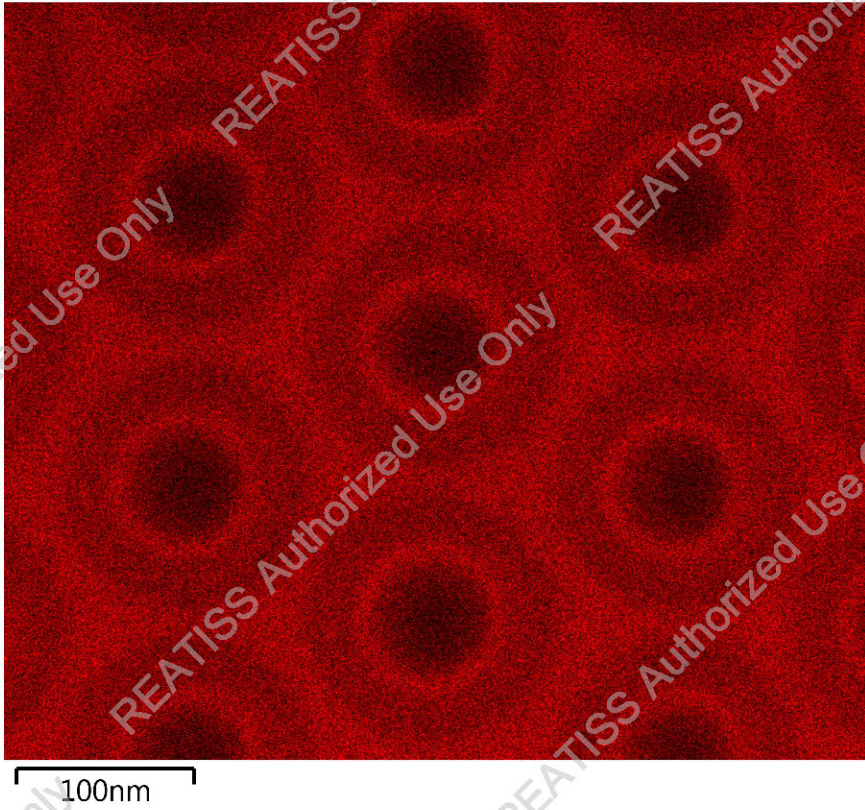


Figure 137. Silicon EDX map layer

O K series



Figure 138. Oxygen EDX map layer

N K series



Figure 139. Nitrogen EDX map layer

P K series

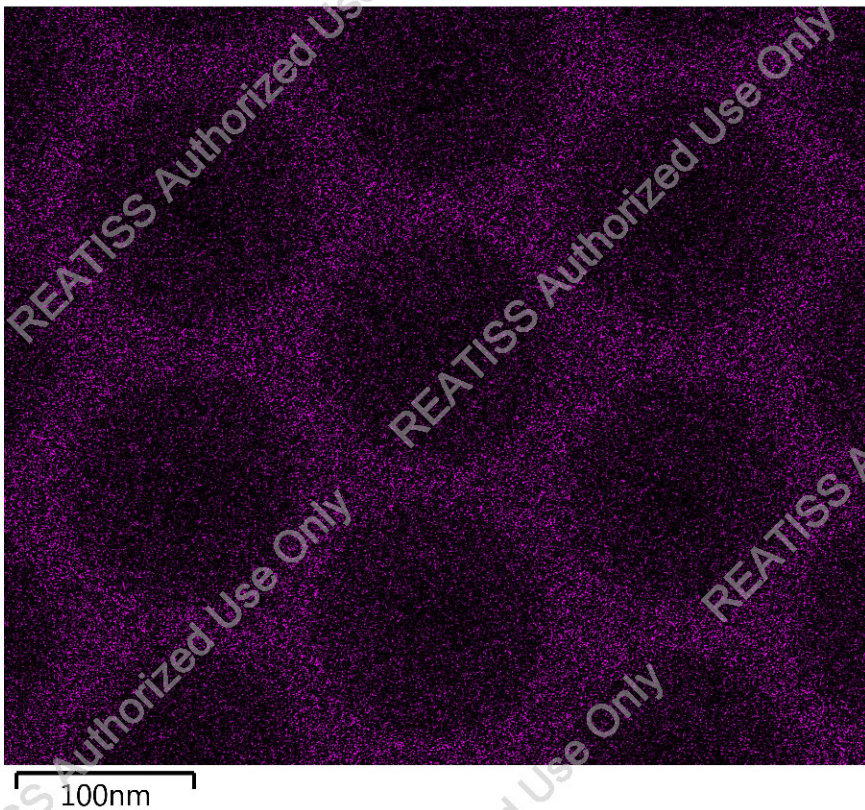


Figure 140. Phosphorus EDX map layer