Intel [redacted]

RF Transceiver

Circuitry Analysis Report

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Introduction

The following report includes focused circuitry analysis of the selected blocks of the **Intel** [redacted] **Transceiver.** The analyzed exemplars were extracted from Apple [redacted] iPhone [redacted] main boards.

The report organized in hierarchical manner with interactive links as follows:

Device Summary Sheet section comprises brief package and technology summary of the die of interest.

Source Device section comprises Apple [redacted] iPhone [redacted] device and PCBs photographs.

Package and Die section comprises Intel [redacted] RF Transceiver package, X-ray and die photographs.

Die Functional Blocks section comprises die photograph with marked blocks under analysis.

1.0 Receiver Block Diagram section comprises schematics of the selected blocks of the receiver part of the die.

2.0 Transmitter Block Diagram section comprises schematics of the selected blocks of the transmitter part of the die.

3.0 ET Interface section comprises schematics of the selected blocks for Envelope Tracking technology of the transmitter RF part.

4.0 TX PLL section comprises schematics of the selected blocks of the Transmitter Phase Locked Loop circuit.

5.0 GNSS Block Diagram section comprises schematics of the selected blocks of the GNSS part of the die.

Appendix section describes device parameters, annotations, and symbol definitions for the schematics.

All information of this report was derived by REATISS from high magnification photographs. All device sizes are measured from photographs in microns.

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Source Device

Package and Die

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3.0 ET Interface

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Figure 3.1 Layout of ET Interface block with analyzed blocks marked (Metal 1 layer)

4.0 TX PLL

5.0 GNSS Block Diagram

Appendix

Device Summary Sheet

Manufacturer: Intel Corporation
Part Number: [redacted]
Date Code: [redacted]
IC Type: RF Transceiver

Technology synopsis

Package Type:	WLCSP
Pin Count:	249
Package Size:	6 mm x 6 mm x 0,4 mm
Die Count:	1
Die Size:	6,06 mm x 5,96 mm (by edge of physical silicon) 6,04 mm x 5,94 mm (by edge of seal)
Number of Metal Layers:	8. One layer of aluminum interconnect, seven layers of copper interconnect
Gate Layer:	One layer of metal gates
Minimum Printed Gate Length[1]:	41 nm
Device Isolation Type:	STI

[1] Measured feature sizes are accurate within 10%

Source Device

Figure 0.1 Apple [redacted] iPhone [redacted] frame with detached display assembly and battery

Figure 0.2 Apple [redacted] iPhone [redacted] back side

Figure 0.3 Apple [redacted] iPhone [redacted] main PCB assembly (side A)

Figure 0.4 Apple [redacted] iPhone [redacted] main PCB assembly (side B)

Figure 0.5 Apple [redacted] iPhone [redacted] main PCB-I (side A)

Figure 0.6 Apple [redacted] iPhone [redacted] main PCB-I (side B)

Figure 0.7 Apple [redacted] iPhone [redacted] main PCB-II (side A)

Intel [redacted] Transceiver

Figure 0.8 Apple [redacted] iPhone [redacted] main PCB-II (side B)

Package and Die

Figure 0.9 Intel [redacted] Transceiver package top

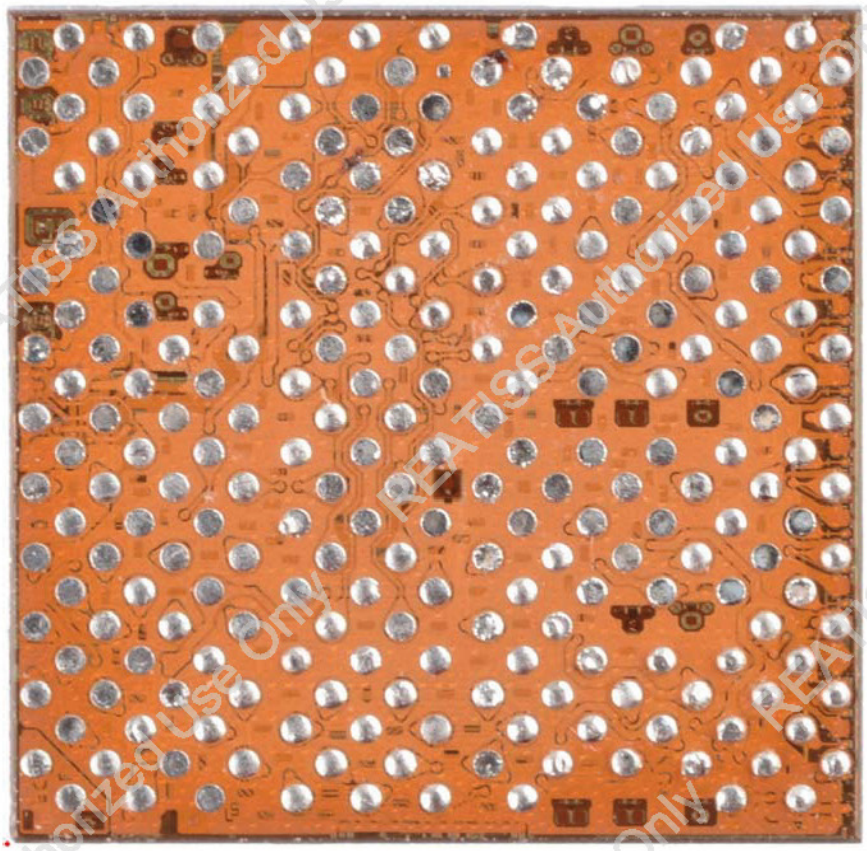


Figure 0.10 Intel [redacted] Transceiver package bottom

Figure 0.11 Intel [redacted] Transceiver package bottom with balls marked

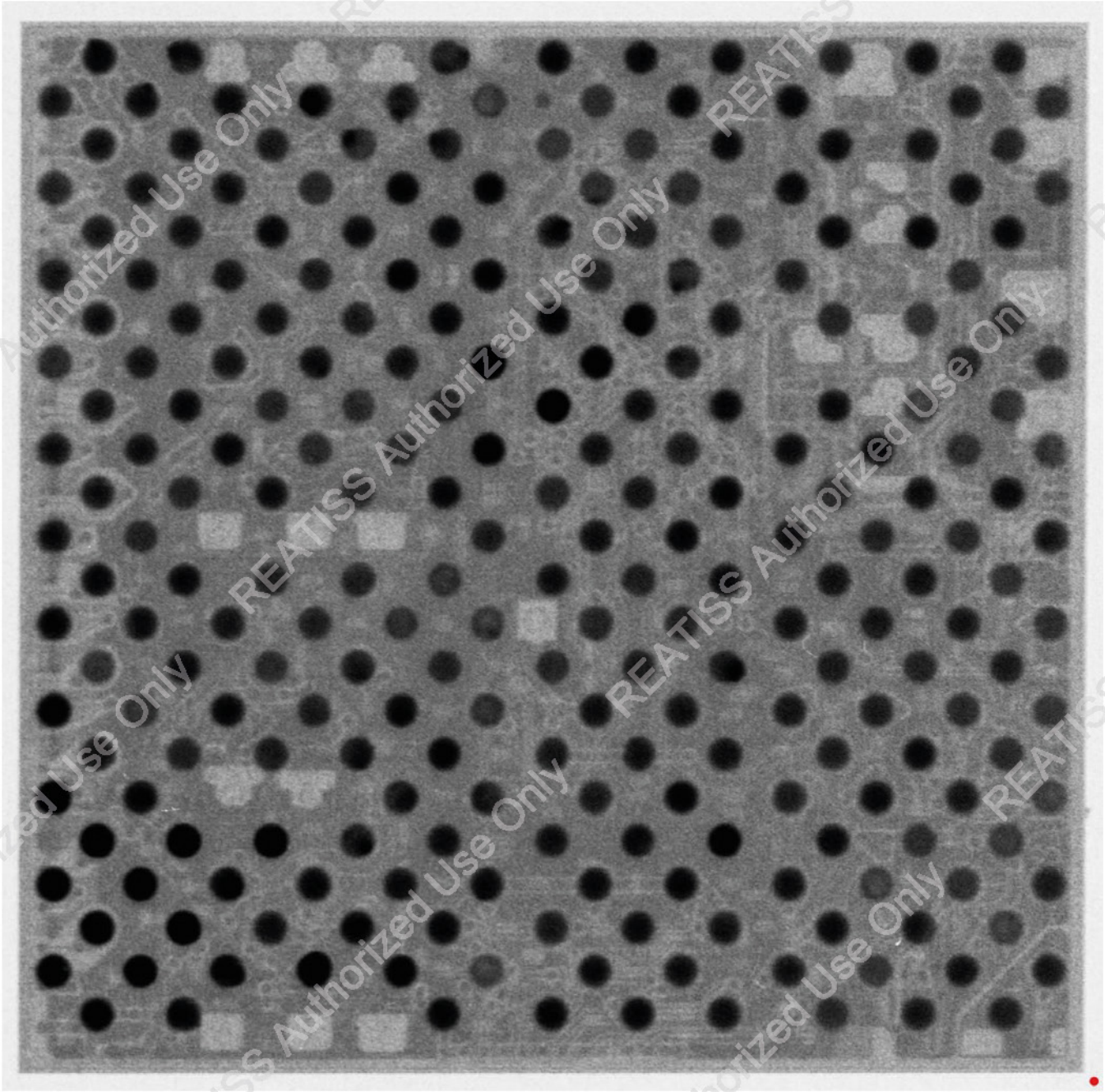


Figure 0.12 Intel [redacted] Transceiver package X-ray

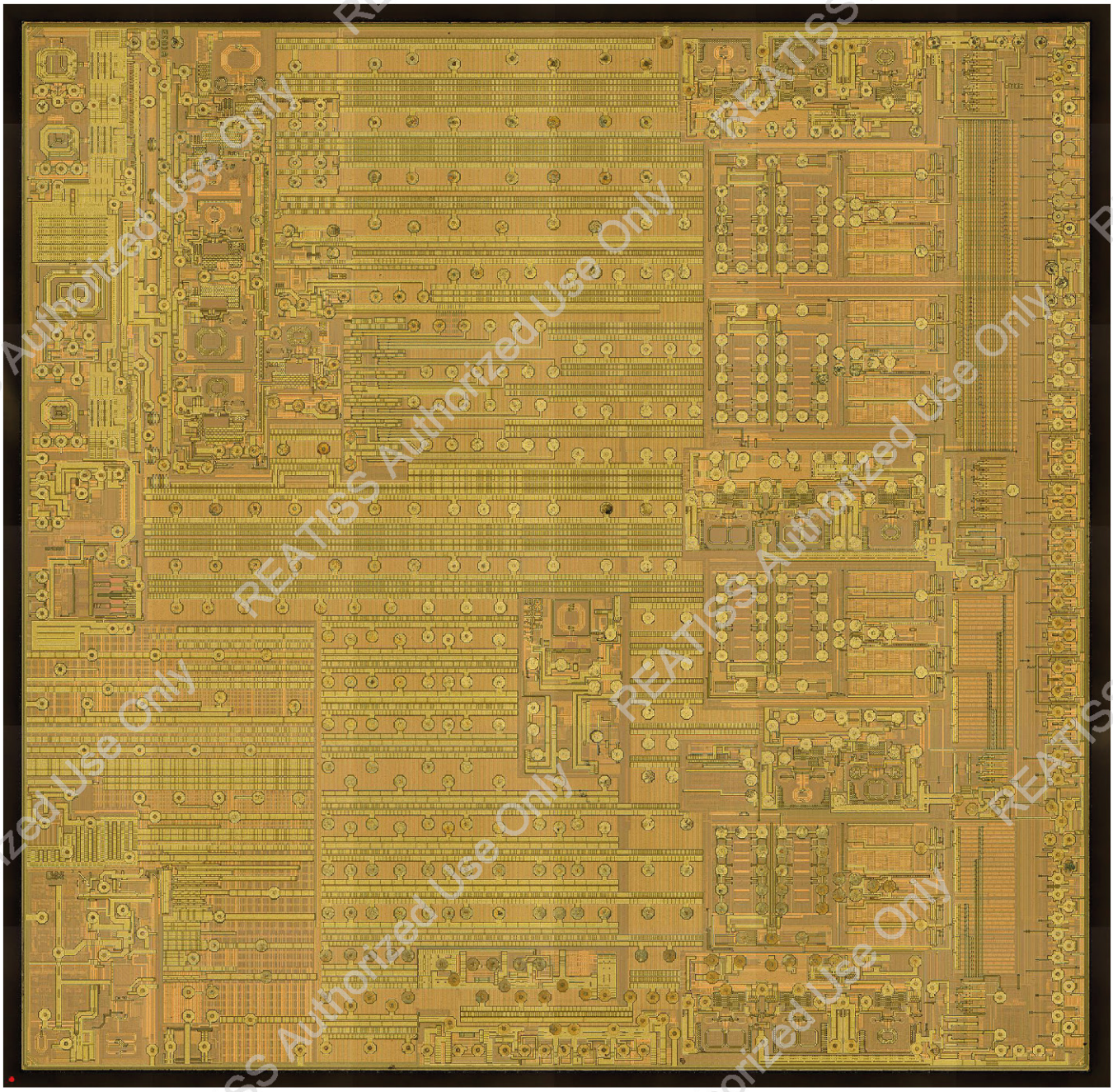


Figure 0.13 Die photo (top metal)

Figure 0.14 Die markings A

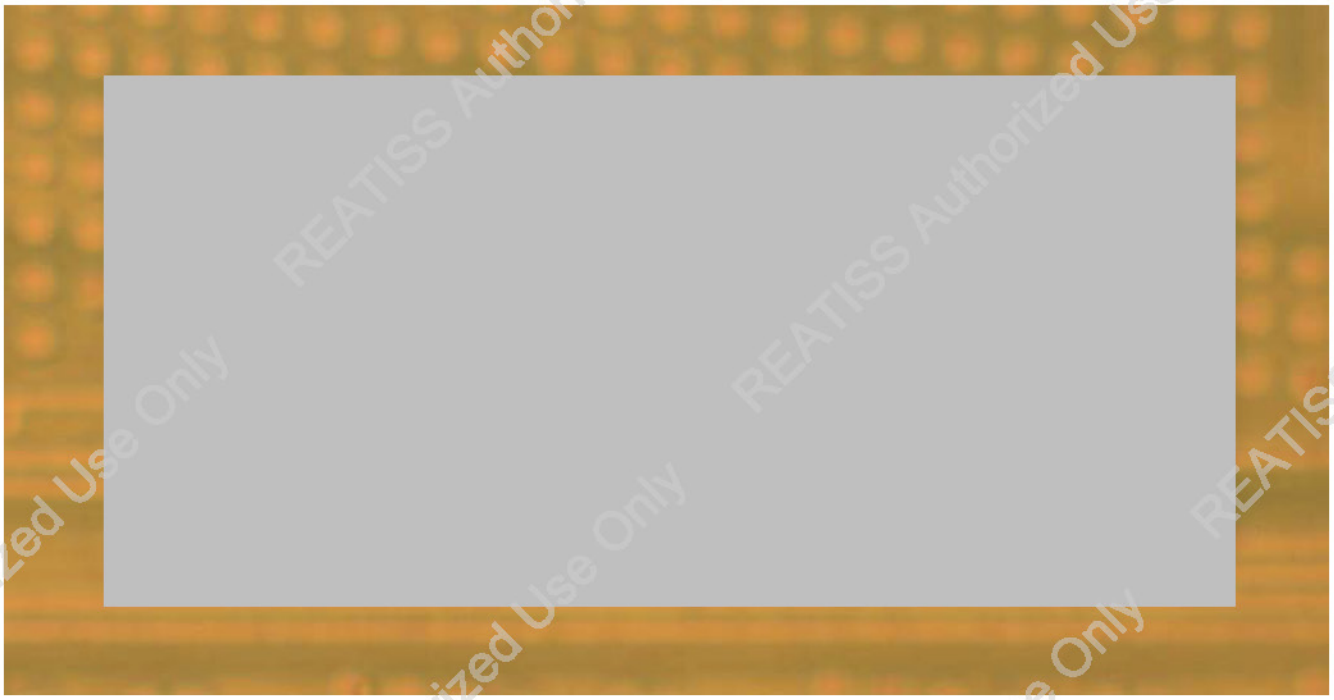


Figure 0.15 Die markings B

Figure 0.16 Die markings C

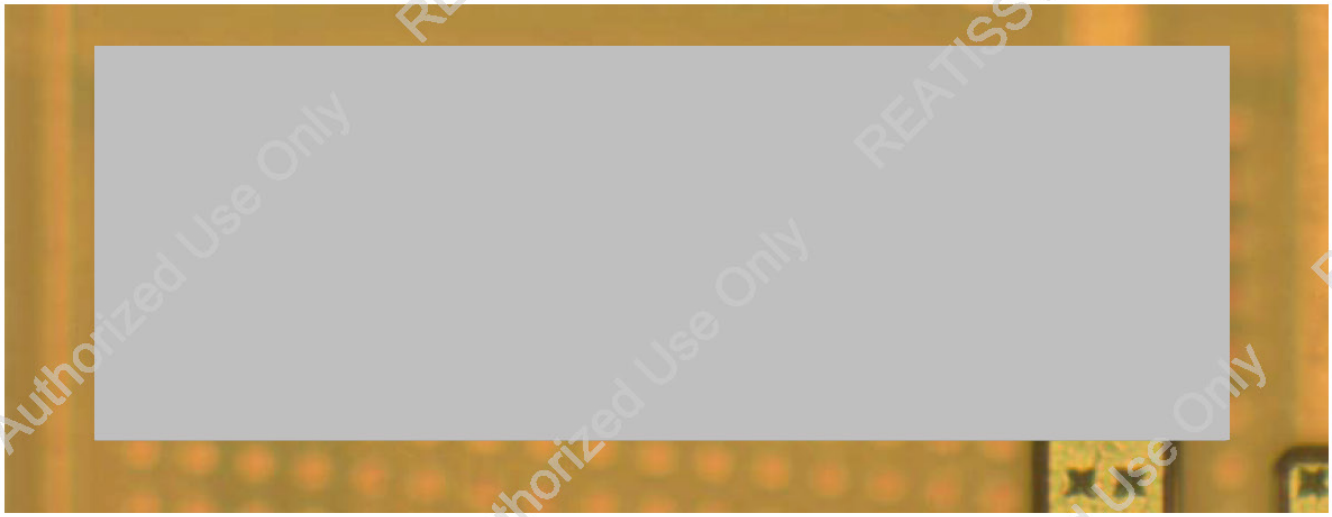


Figure 0.17 Die markings D

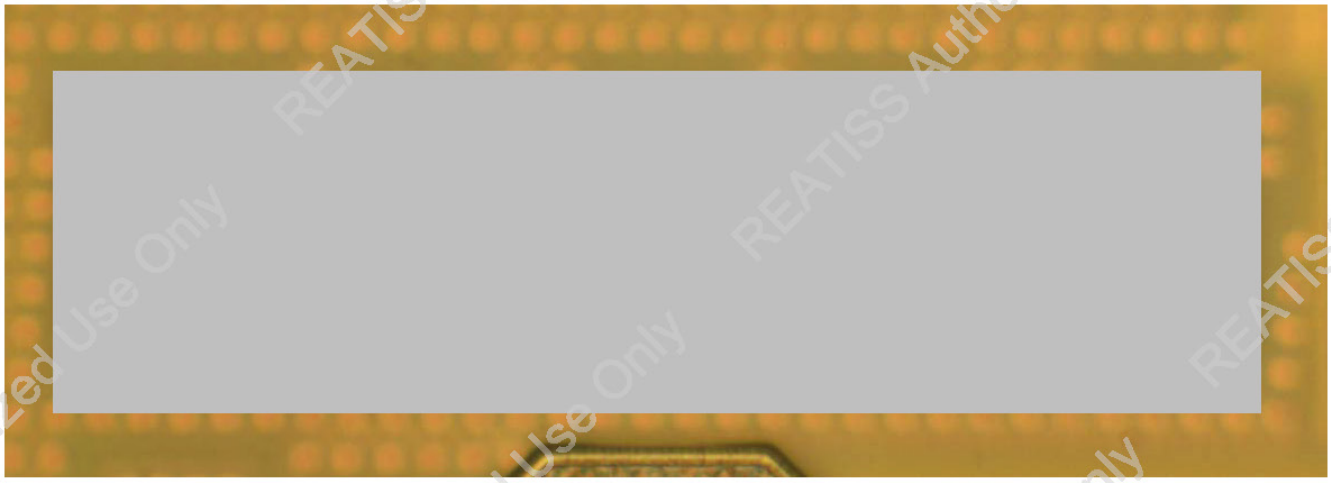


Figure 0.18 Die markings E

Figure 0.19 Die photo (Active layer)

Die Functional Blocks

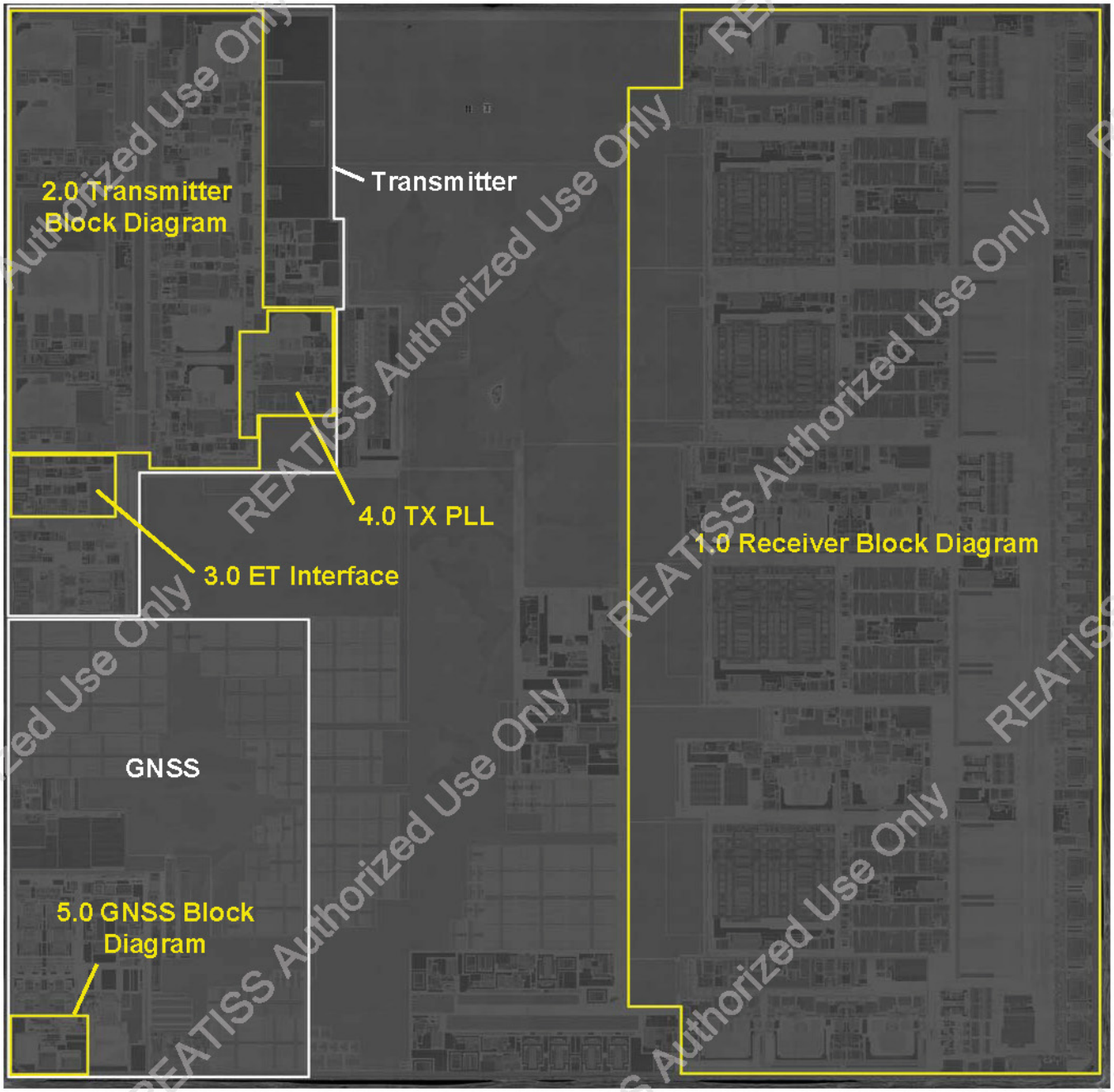


Figure 0.20 Intel [redacted] Transceiver die functional blocks (Active layer)

1.0 Receiver Block Diagram

Figure 1.0 Layout of 1.0 RECEIVER_BLOCK_DIAGRAM (RDL2 layer)

Figure 1.1 Layout of 1.0 RECEIVER_BLOCK_DIAGRAM (Active layer)

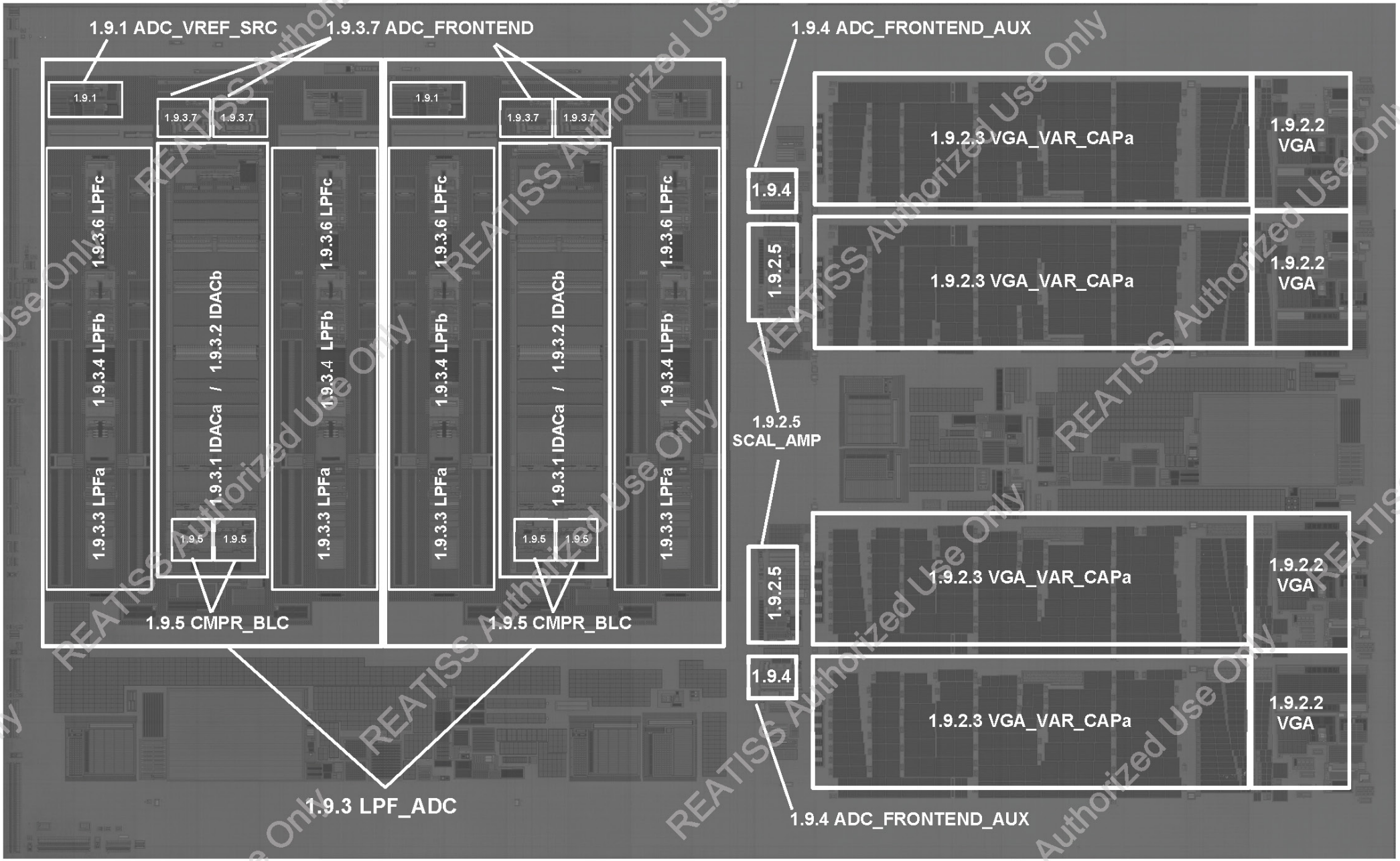
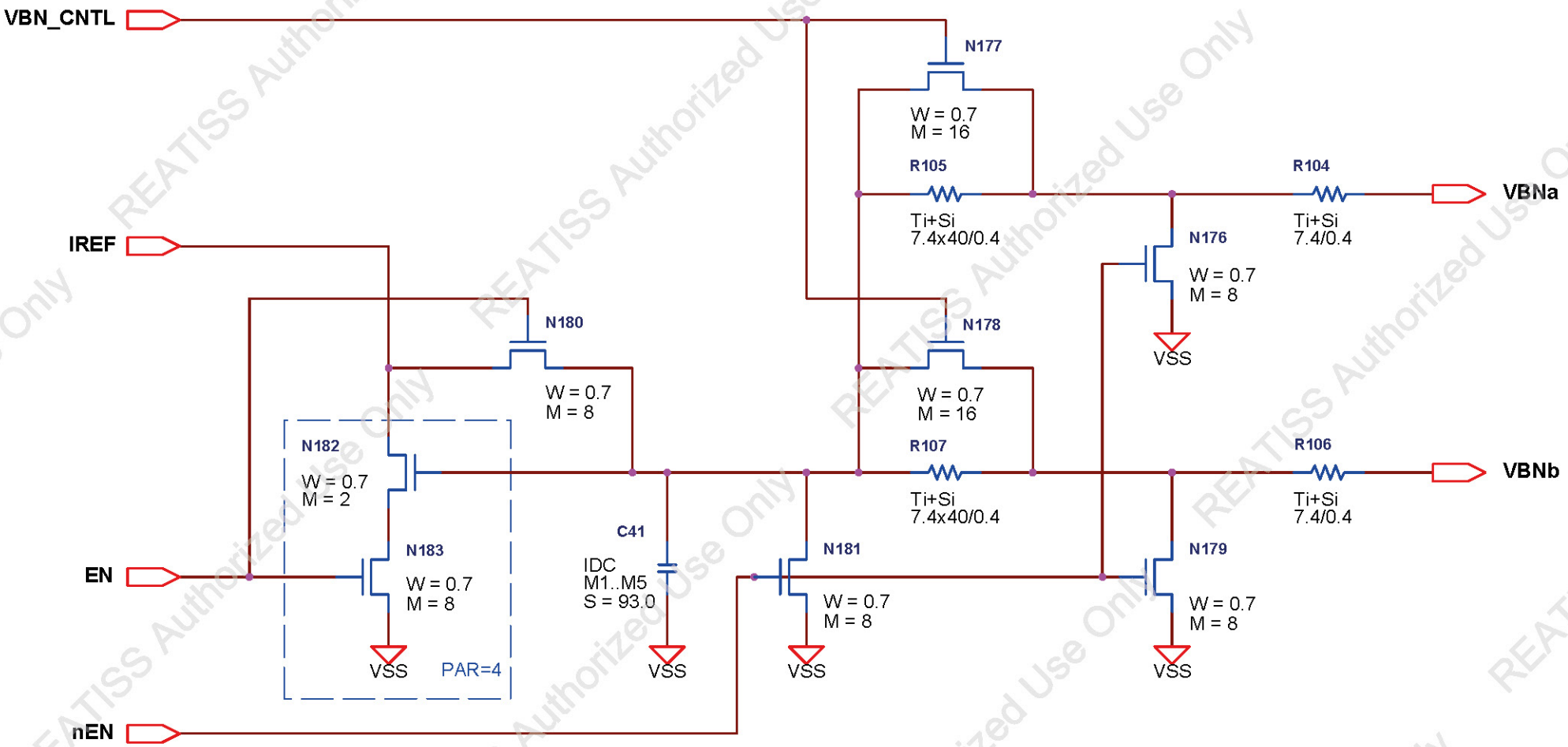


Figure 1.2 Layout of 1.9 RX_ADC (Gate layer)



VSS

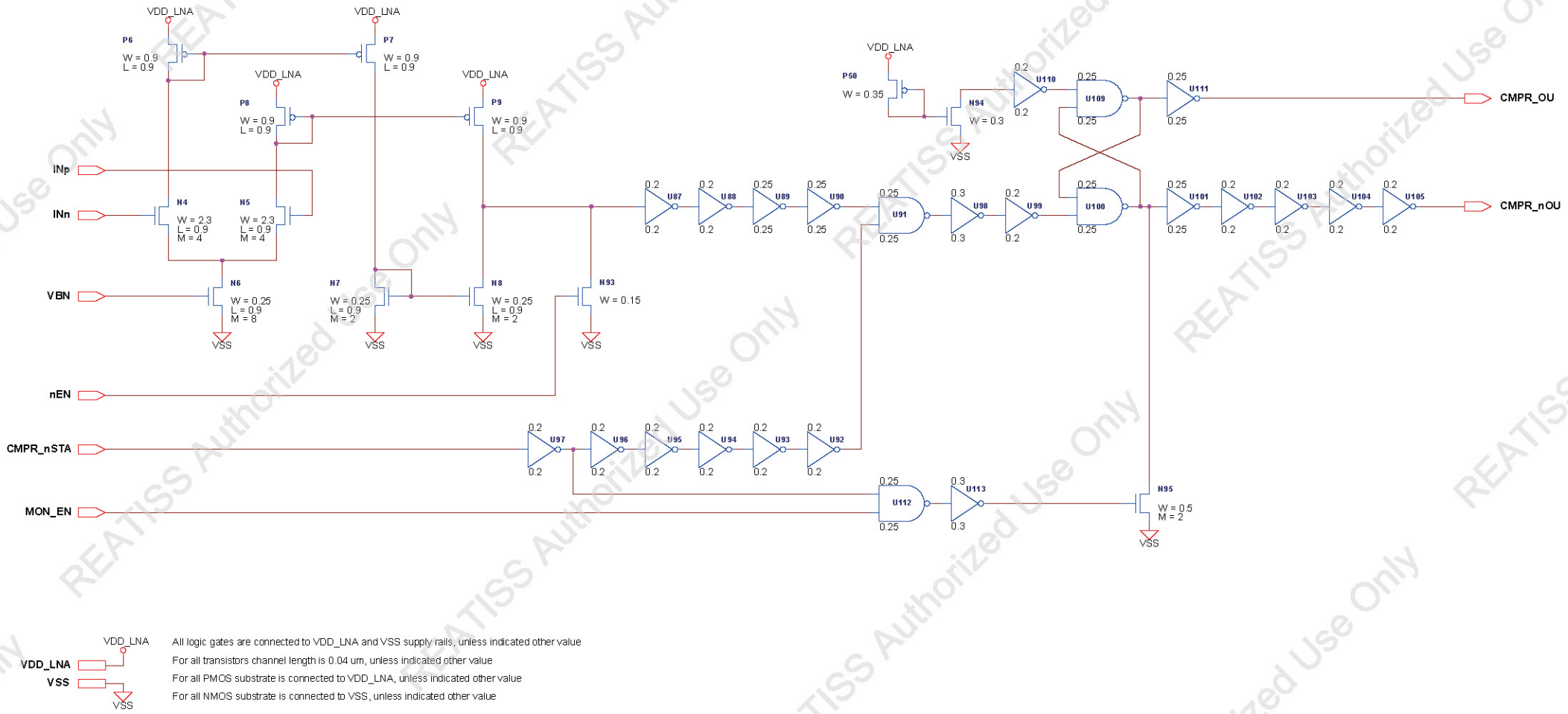
VSS

For all transistors channel length is 0.04 um, unless indicated other value

For all NMOS substrate is connected to VSS, unless indicated other value

1.1.1.4.1 BIAS_SRCa

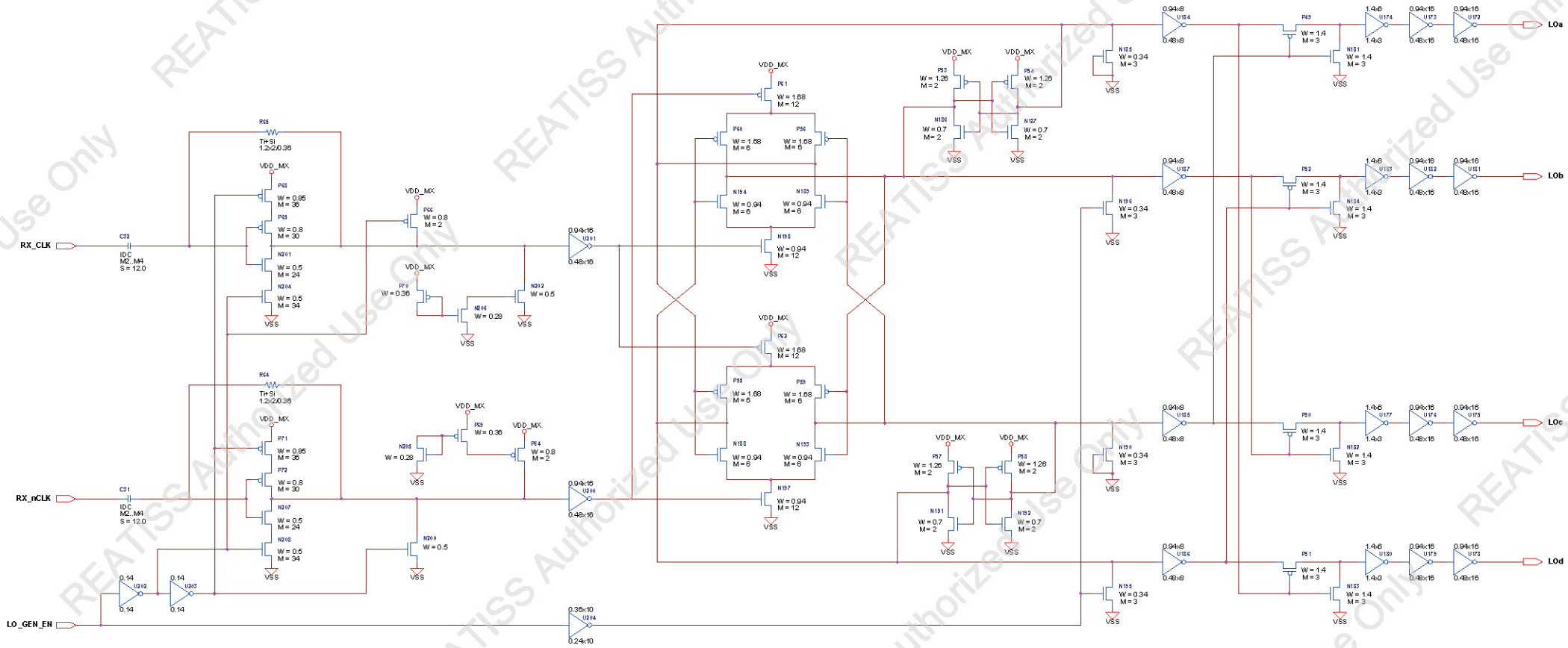
Bias Source A



All logic gates are connected to VDD_LNA and VSS supply rails, unless indicated other value
For all transistors channel length is 0.04 um, unless indicated other value
For all PMOS substrate is connected to VDD_LNA, unless indicated other value
For all NMOS substrate is connected to VSS, unless indicated other value

1.1.1.5.3 CMPRa

Comparator A



1.3.1 LO_GENb

LO Generator B

2.0 Transmitter Block Diagram

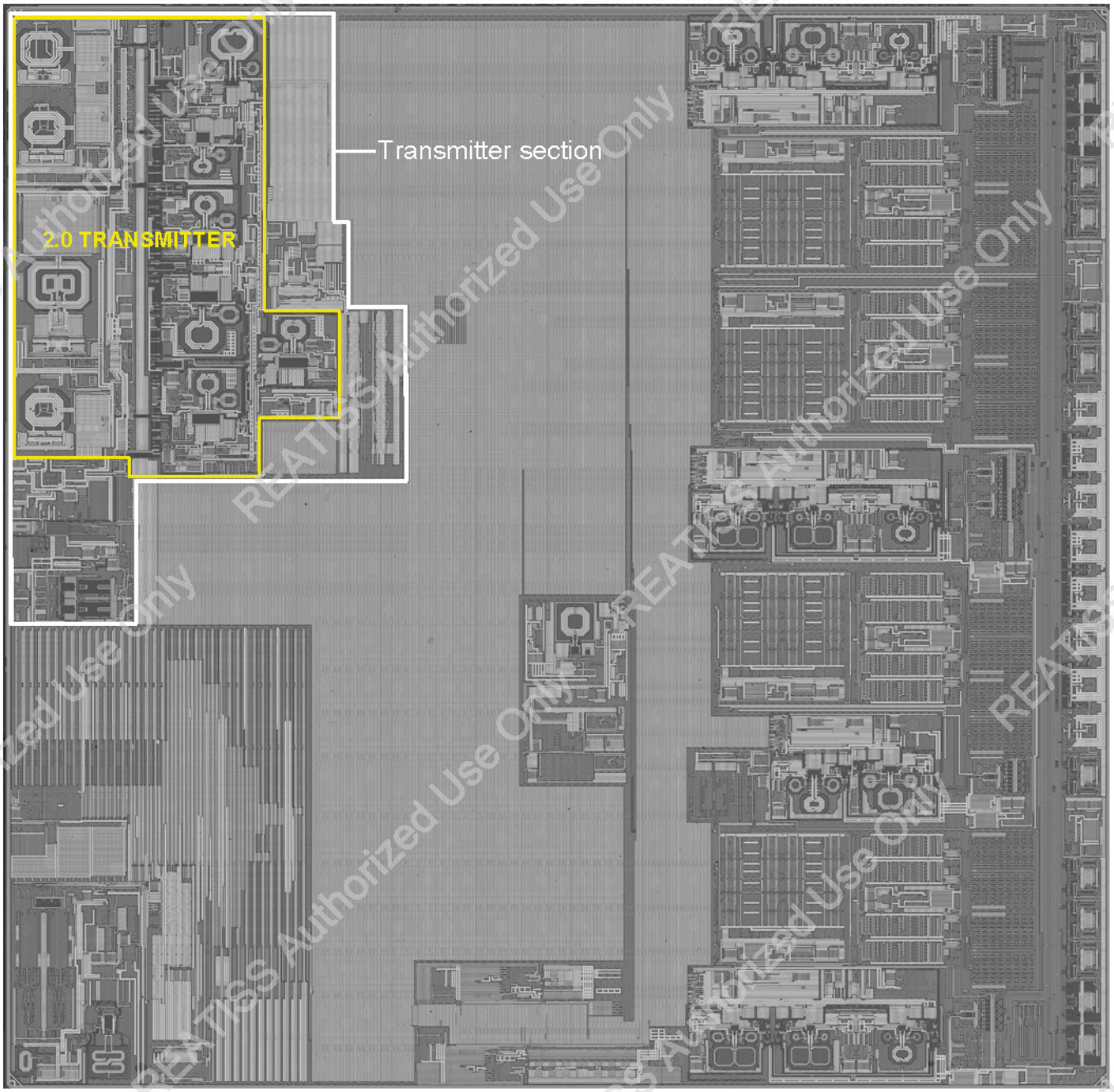


Figure 2.0 Die photo with Transmitter section and Transmitter block marked (Metal 7 layer)

Figure 2.1 Layout of Transmitter section with analyzed blocks marked[2] (Active layer)

[2] Analyzed blocks highlighted in yellow

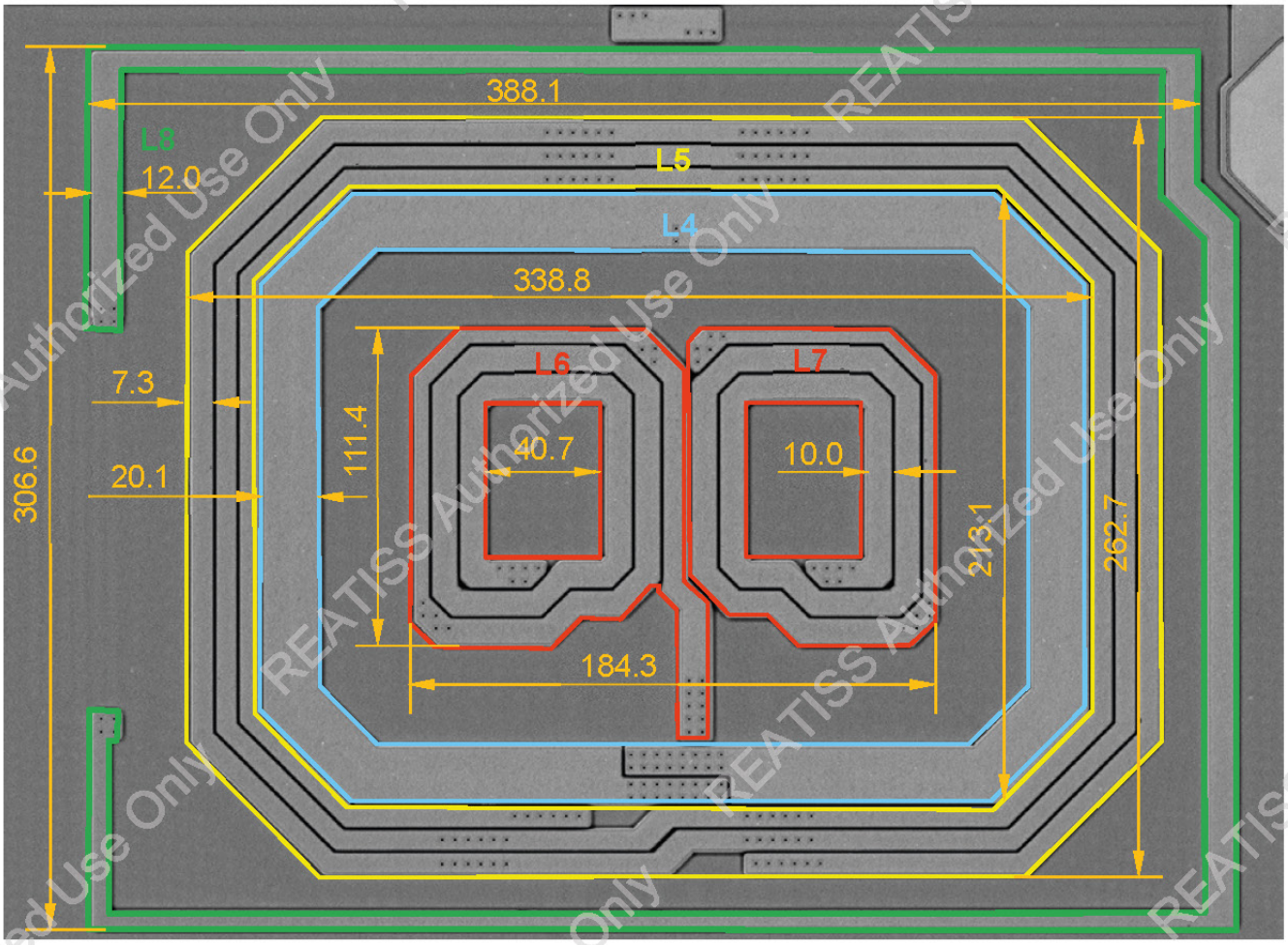
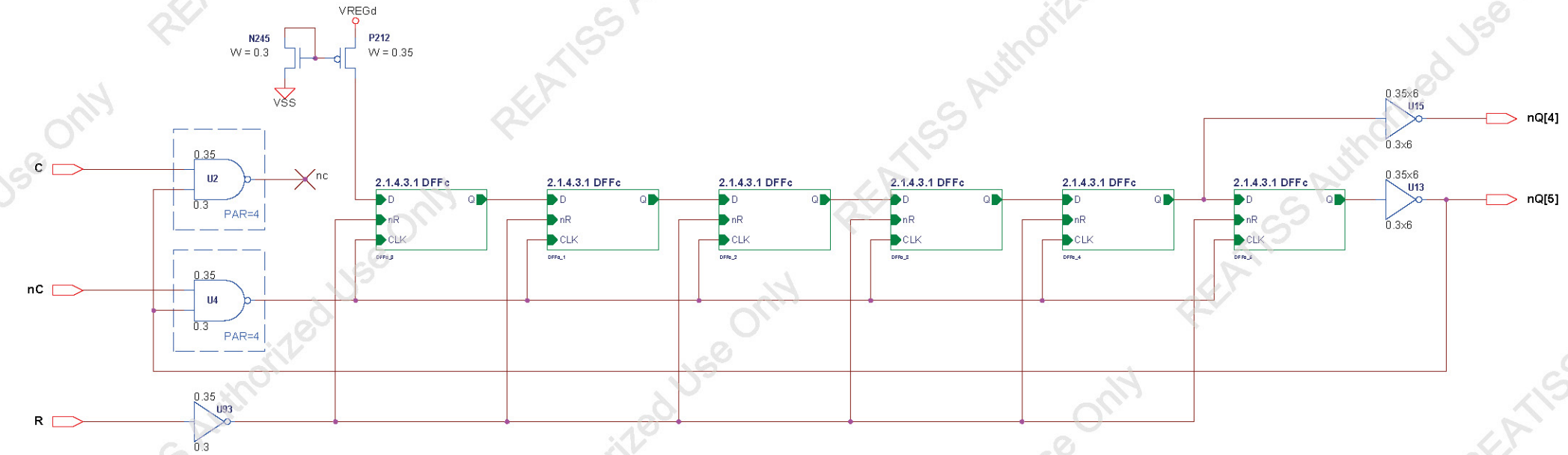
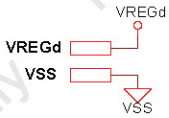


Figure 2.5 Layout of inductors L4, L5, L6, L7 and L8 of schematic 2.6 TRANSFORMERc (Metal 8 layer)





All logic gates are connected to VREGd and VSS supply rails, unless indicated other value

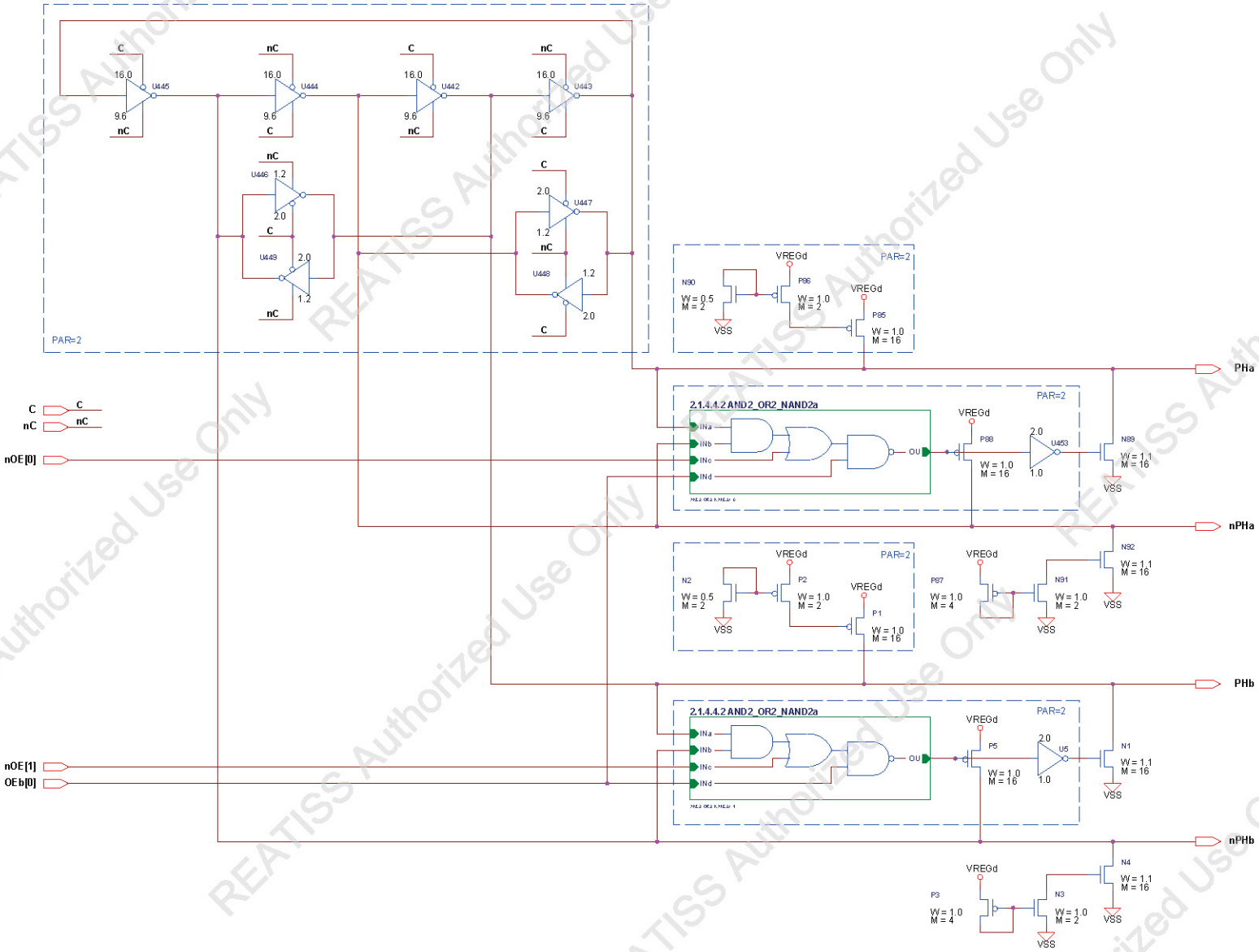
For all transistors channel length is 0.04 um, unless indicated other value

For all PMOS substrate is connected to VREGd, unless indicated other value

For all NMOS substrate is connected to VSS, unless indicated other value

2.1.4.3 SHIFT_RGa

Shift Register A



VREGd
VSS

All logic gates are connected to VREGd and VSS supply rails, unless indicated other value
For all transistors channel length is 0.04 um, unless indicated other value
For all PMOS substrate is connected to VREGd, unless indicated other value
For all NMOS substrate is connected to VSS, unless indicated other value

2.1.6.5 PH_SPLITTERf

Phase Splitter F

3.0 ET Interface

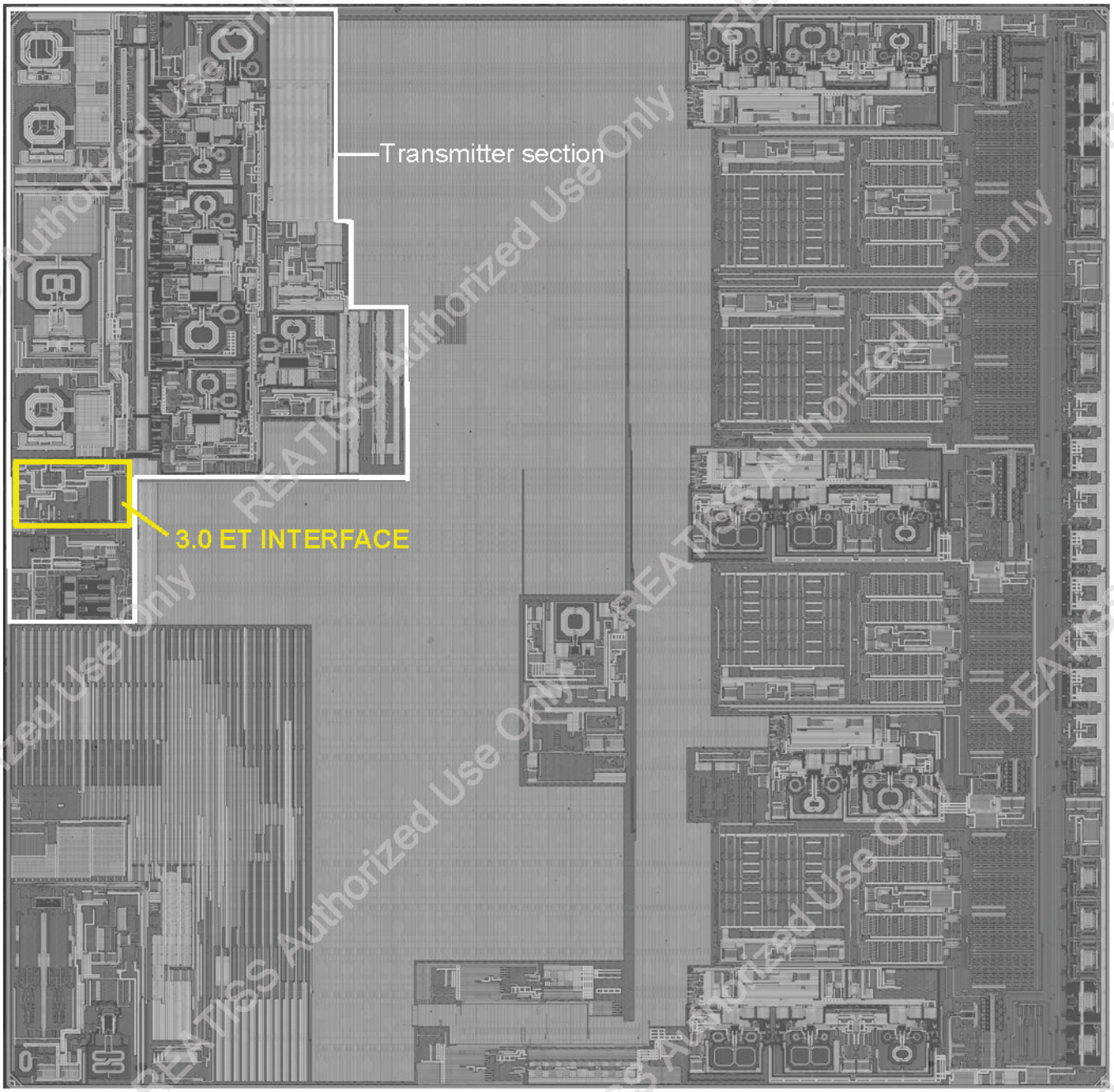
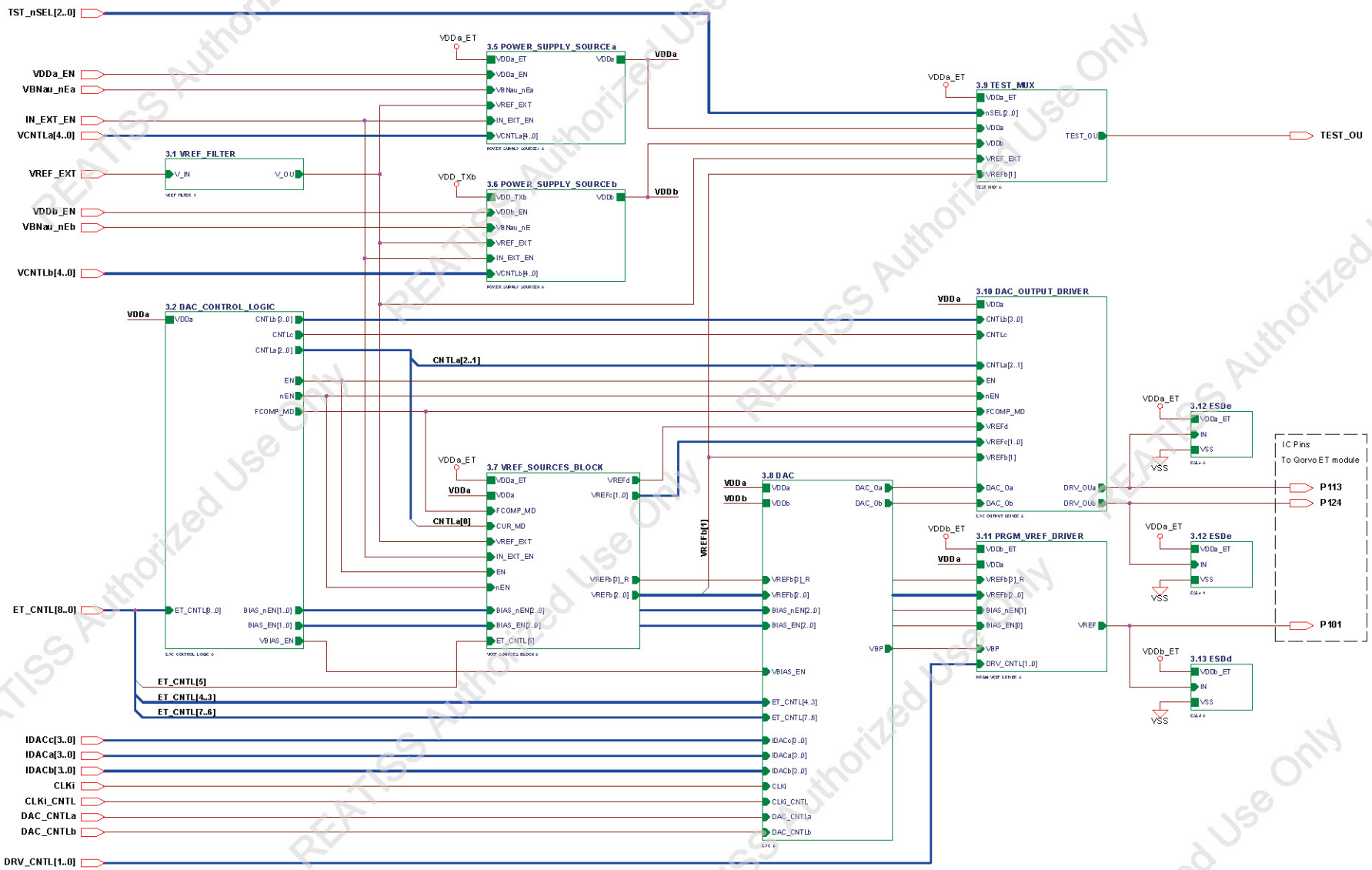
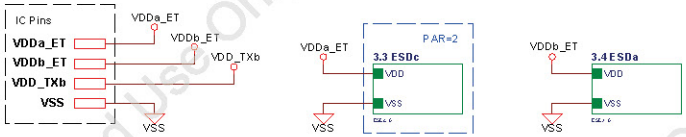


Figure 3.0 Die photo with Transmitter section and ET Interface block marked (Metal 7 layer)

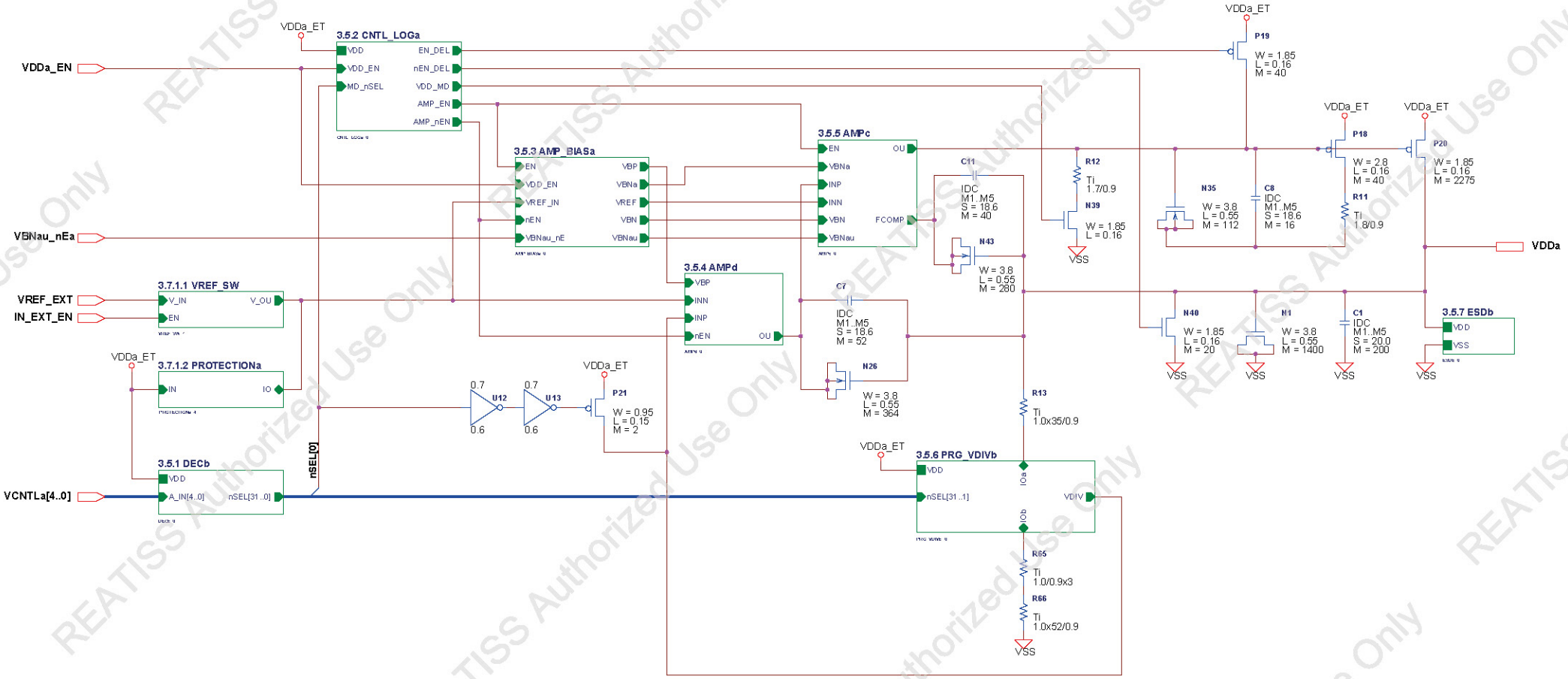
Figure 3.1 Layout of ET Interface block with analyzed blocks marked (Metal 1 layer)





3.0 ET_INTERFACE

Envelope Tracker Interface. A Part of Circuits.



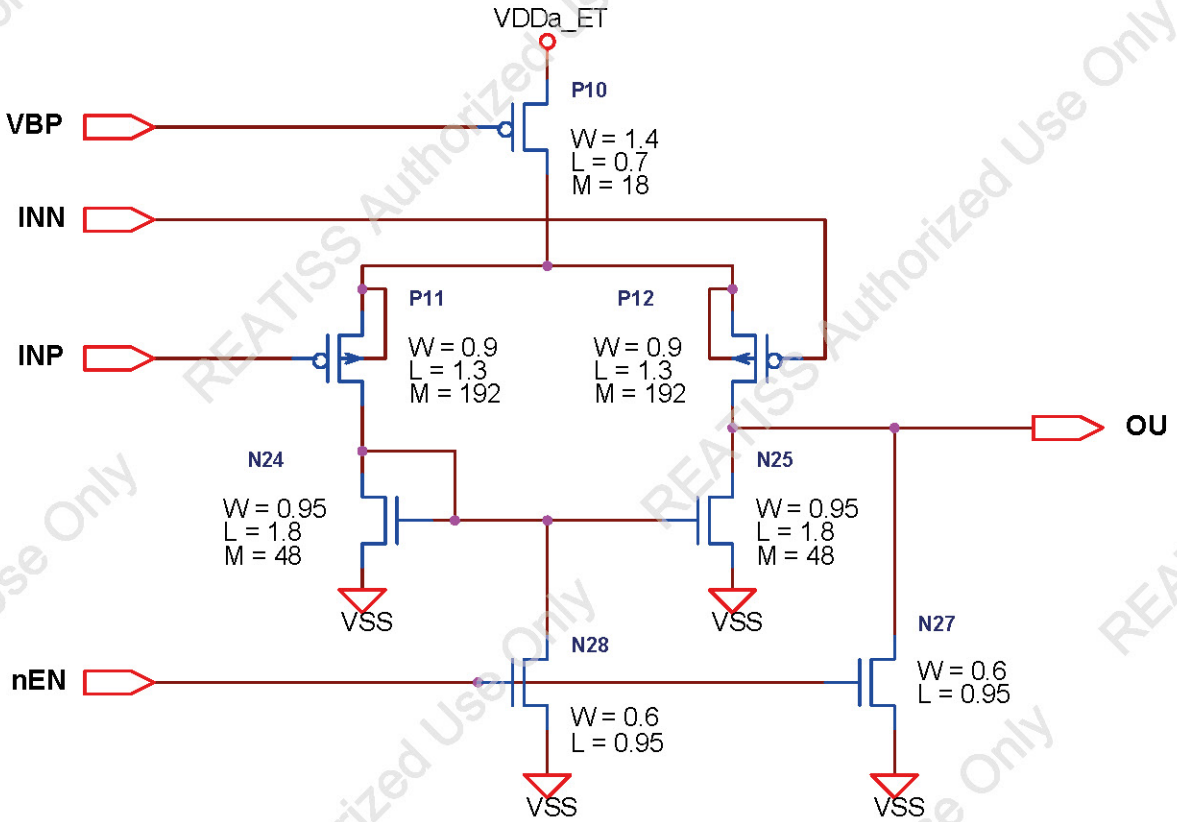
VDDa_ET — All logic gates are connected to VDDa_ET and VSS supply rails, unless indicated other value

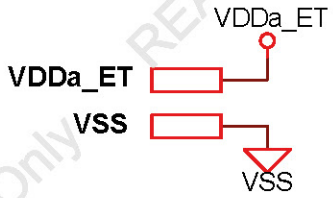
VDDa_ET — For all transistors channel length is 0.15 um, unless indicated other value

VSS — For all PMOS substrate is connected to VDDa_ET, unless indicated other value

For all NMOS substrate is connected to VSS, unless indicated other value

3.5 POWER_SUPPLY_SOURCEa





For all PMOS substrate is connected to VDDa_ET, unless indicated other value

For all NMOS substrate is connected to VSS, unless indicated other value

3.5.4 AMPd

Amplifier D

5.0 GNSS Block Diagram

Figure 5.0 Die photo with GNSS section marked (Active layer)

Figure 5.1 Layout of GNSS section with analyzed blocks marked (Active layer)

Figure 5.2 Layout of 5.0 GNSS_BLOCK_DIAGRAM (Active layer)

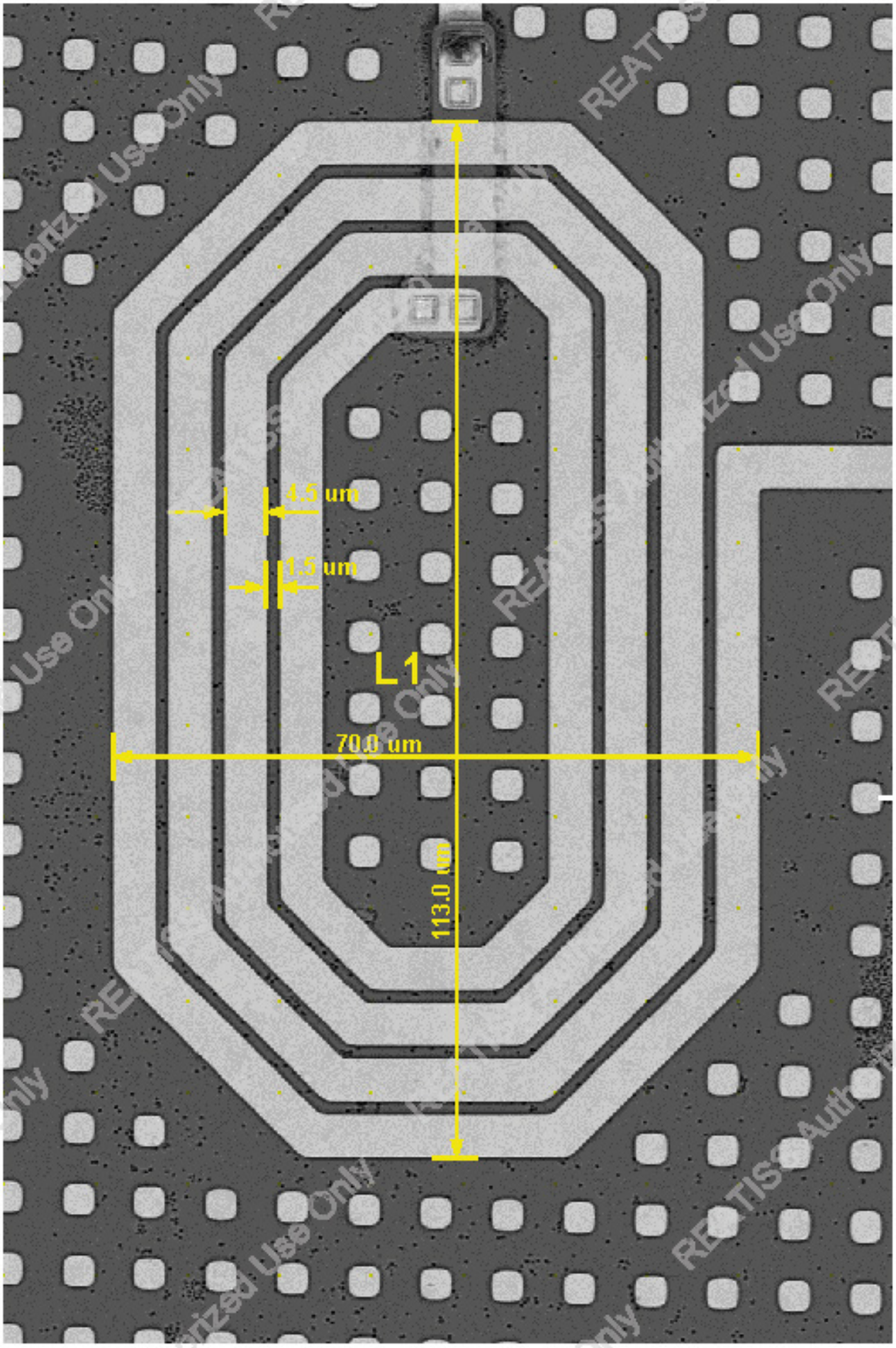
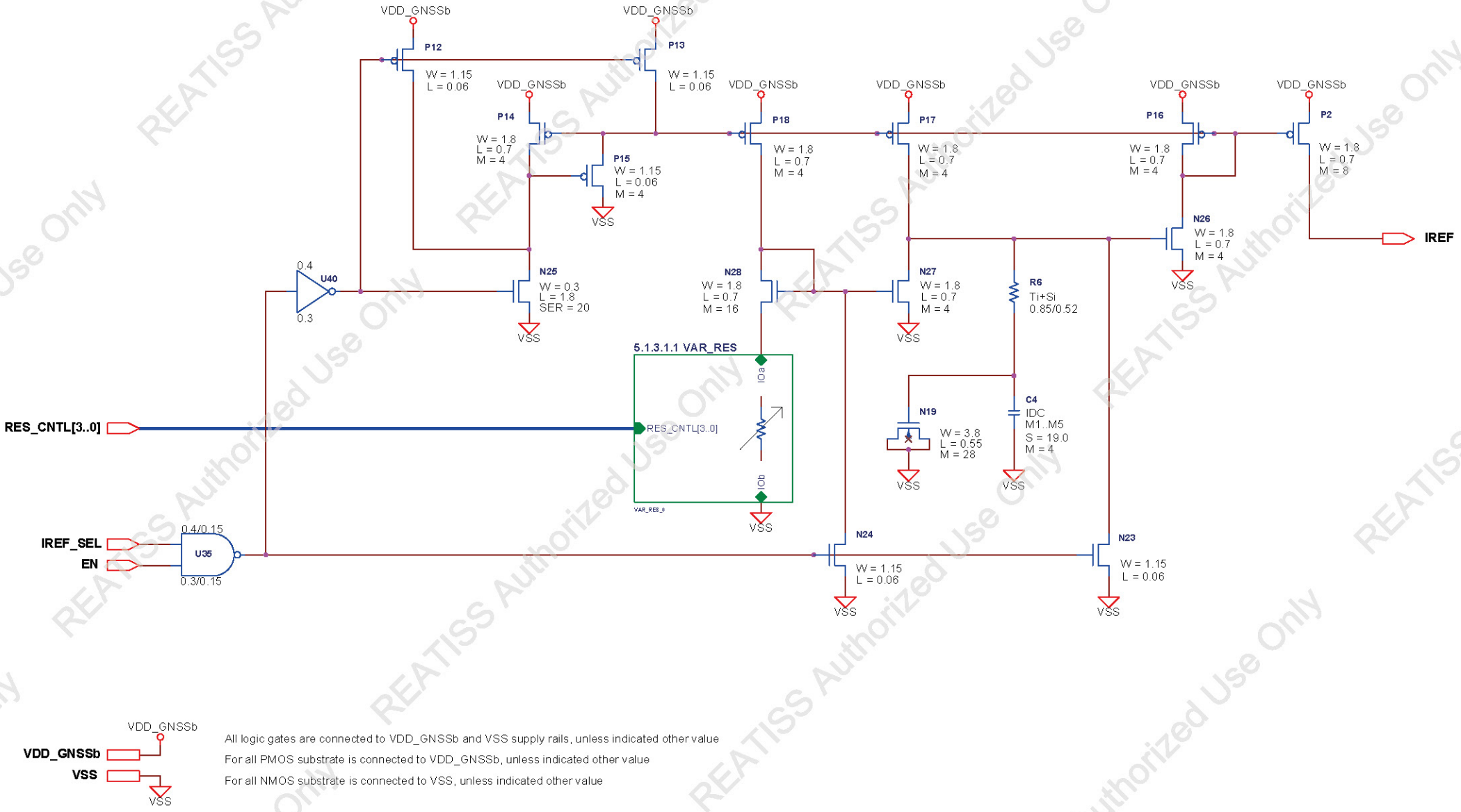


Figure 5.3 Layout of inductor L1 of schematic 5.1 GNSS_LNA (Metal 7 layer)



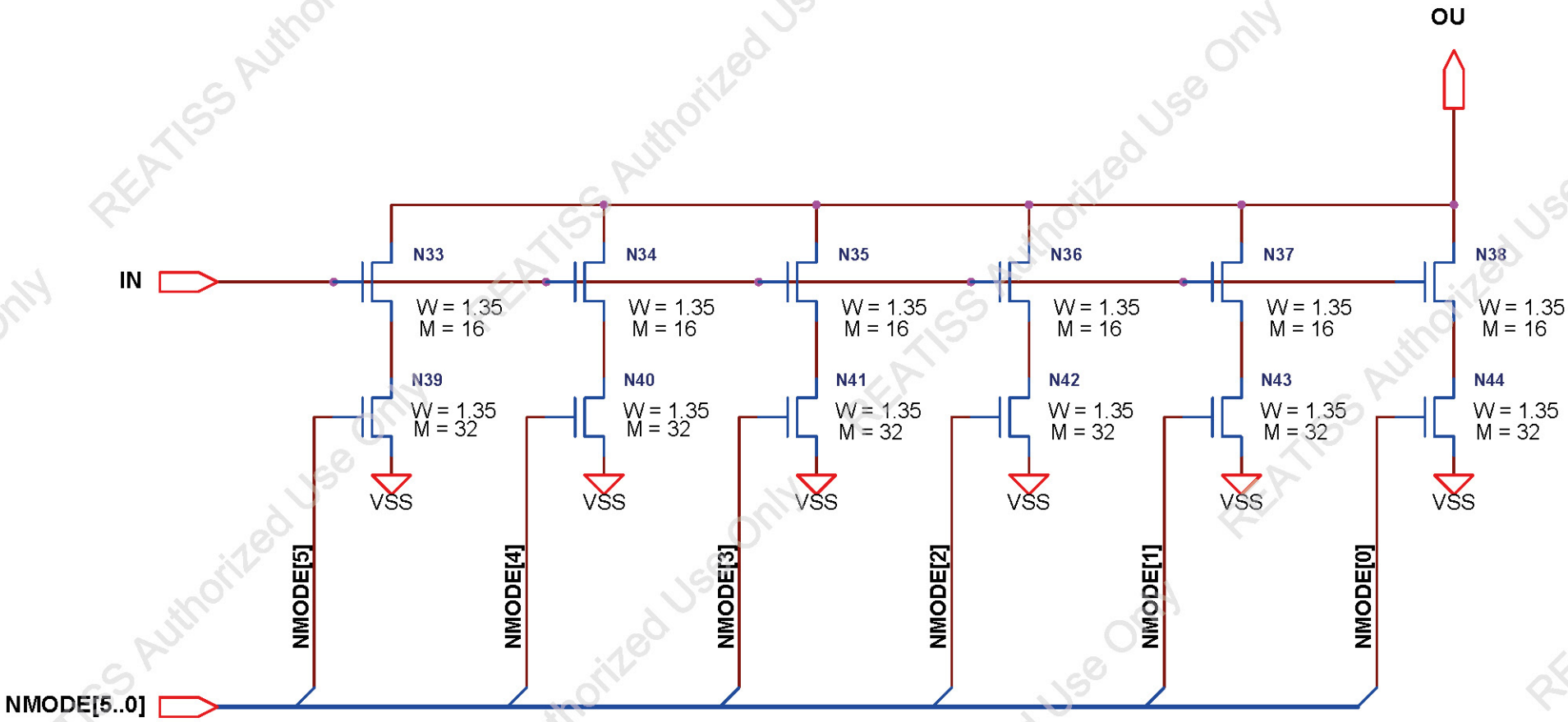
All logic gates are connected to VDD_GNSSb and VSS supply rails, unless indicated other value

For all PMOS substrate is connected to VDD_GNSSb, unless indicated other value

For all NMOS substrate is connected to VSS, unless indicated other value

5.1.3.1 IREF_SRCa

Reference Current Source A



VSS

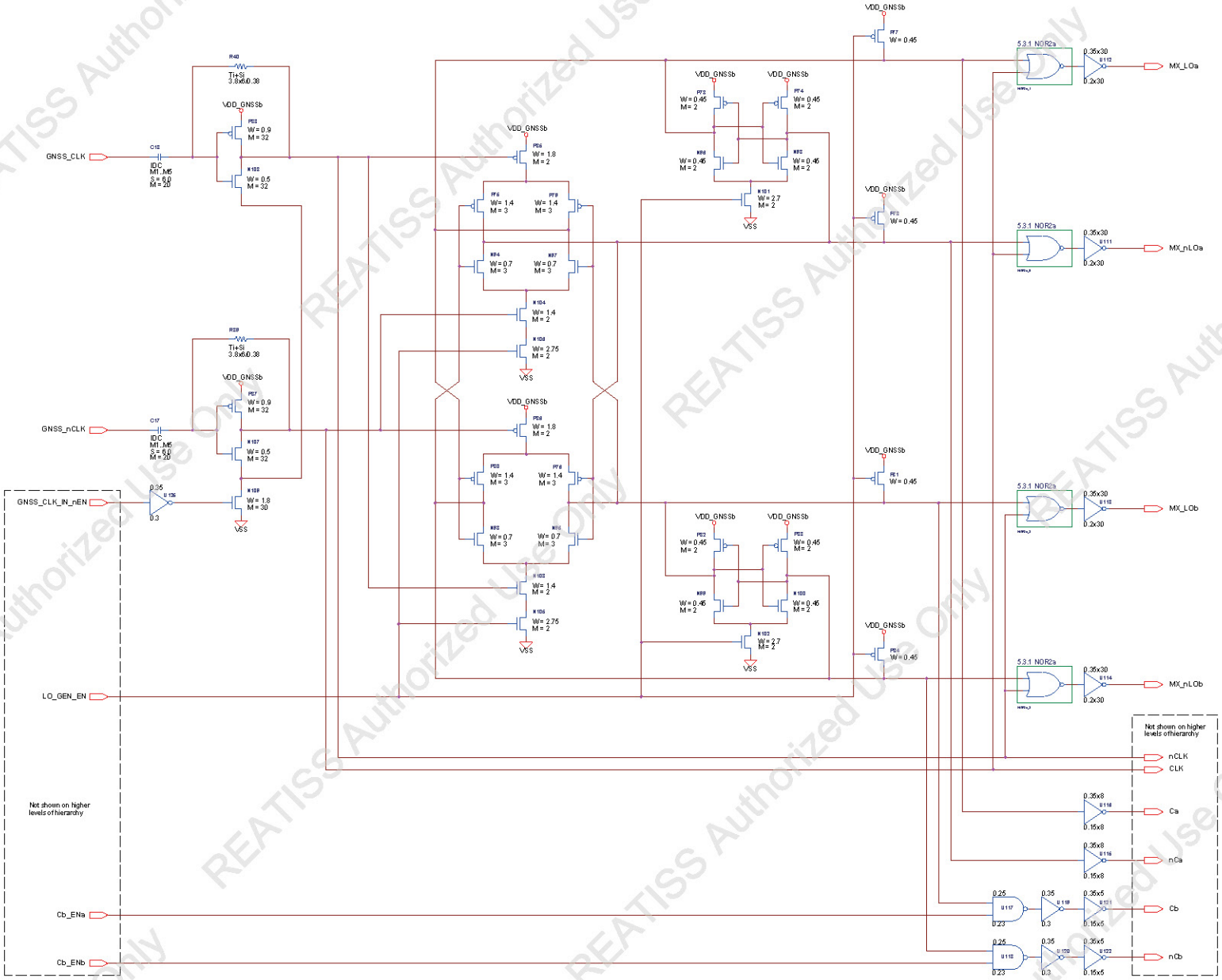
VSS

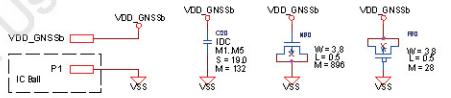
For all transistors channel length is 0.06 um, unless indicated other value

For all NMOS substrate is connected to VSS, unless indicated other value

5.1.9 NMOSa

Programmable NMOS Stack A





All logic gates are connected to VDD_GNSSb and VSS supply rails, unless indicated other value
For all transistors channel length is 0.03 um, unless indicated other value
For all PMOS substrate is connected to VDD_GNSSb, unless indicated other value
For all NMOS substrate is connected to VSS, unless indicated other value

5.3 LO_GENERATOR