

Intel 

RF Transceiver

Circuitry Analysis Report

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# Introduction

The following report includes focused circuitry analysis of the selected blocks of the Intel [REDACTED] [REDACTED] Transceiver. The analyzed exemplars were extracted from Apple [REDACTED] iPhone [REDACTED] main boards.

The report organized in hierarchical manner with interactive links as follows:

**Device Summary Sheet** section comprises brief package and technology summary of the die of interest.

**Source Device** section comprises Apple [REDACTED] iPhone [REDACTED] device and PCBs photographs.

**Package and Die** section comprises Intel [REDACTED] RF Transceiver package, X-ray and die photographs.

**Die Functional Blocks** section comprises die photograph with marked blocks under analysis.

**1.0 Receiver Block Diagram** section comprises schematics of the selected blocks of the receiver part of the die.

**2.0 Transmitter Block Diagram** section comprises schematics of the selected blocks of the transmitter part of the die.

**3.0 ET Interface** section comprises schematics of the selected blocks for Envelope Tracking technology of the transmitter RF part.

**4.0 TX PLL** section comprises schematics of the selected blocks of the Transmitter Phase Locked Loop circuit.

**5.0 GNSS Block Diagram** section comprises schematics of the selected blocks of the GNSS part of the die.

















**Appendix** section describes device parameters, annotations, and symbol definitions for the schematics.

All information of this report was derived by REATISS from high magnification photographs. All device sizes are measured from photographs in microns.





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  - 3.11.2 BIAS\_SOURCEa
  - 3.11.3 AMPb
  - 3.11.4 V\_DIVa
- 3.12 ESDe
- 3.13 ESDd

## 4.0 TX PLL

**Figure 4.0** Die photo with Transmitter section marked (Metal 7 layer)

**Figure 4.1** Layout of Transmitter section with analyzed blocks marked (Metal 7 layer)

**Figure 4.2** Layout of 4.0 TX\_PLL (Metal 2 layer)

### 4.0 TX\_PLL

- 4.1 DIVIDED\_CLOCK\_MUX
  - 4.1.1 DLYm
  - 4.1.2 PWR\_ON\_RSTc
  - 4.1.3 MUXf
  - 4.1.4 LSb
- 4.2 TDC\_BLOCK
  - 4.2.1 CLOCK\_ROUTER
    - 4.2.1.1 REF\_CLOCK\_DRIVER
      - 4.2.1.1.1 DLYd
        - 4.2.1.1.1.1 DLYd\_CELL

**4.2.1.1.2** FOUR\_CH\_MUX  
**4.2.1.1.3** XORd  
**4.2.1.2** MUXm  
**4.2.1.3** CMD\_RG\_DEC  
**4.2.1.3.1** XNORa  
**4.2.1.3.2** DFFg  
**4.2.1.3.3** CMD\_DEC  
**4.2.1.4** PRGM\_DLYa  
**4.2.1.4.1** L\_SRCa  
**4.2.1.4.2** MUXk  
**4.2.1.4.3** DLYf  
**4.2.1.5** PRGM\_DLYb  
**4.2.1.5.1** PDLYb\_CELL  
**4.2.1.6** MUXe  
**4.2.2** TDC\_EN\_DRIVER  
**4.2.2.1** DLYi  
**4.2.2.1.1** V\_DIVa  
**4.2.2.2** PWR\_ON\_RESa  
**4.2.2.3** V\_DIVb  
**4.2.2.4** V\_DET  
**4.2.2.5** LSa  
**4.2.3** TDC\_VREG  
**4.2.3.1** FB\_VDIVIDER  
**4.2.3.2** VREG\_BIAS  
**4.2.3.3** VREF\_FILTER  
**4.2.3.3.1** INPUT\_PROT  
**4.2.3.4** CAP\_BANK  
**4.2.3.4.1** CAP\_DRV  
**4.2.3.5** L\_SRCb  
**4.2.4** TDC\_CNTL  
**4.2.4.1** PWR\_ON\_RSTb  
**4.2.4.1.1** LSd  
**4.2.4.2** TDC\_CLK\_DRIVER  
**4.2.4.2.1** MUXg  
**4.2.4.3** DLYg  
**4.2.4.4** DLYo  
**4.2.4.5** DLYb

**4.2.4.5.1** INVb

**4.2.4.6** DLYj

**4.2.4.7** DLYn

**4.2.4.8** MUXh

**4.2.4.9** DLYh

**4.2.4.9.1** DLYa

**4.2.4.10** DLYe

**4.2.4.11** H\_SRCa

**4.2.4.12** DFFi

**4.2.5** TDC

**4.2.5.1** MPRO

**4.2.5.2** CLK\_DLY

**4.2.5.3** TDC\_LATCHa

**4.2.5.4** TDC\_LATCHb

**4.2.6** TDC\_OUTPUT\_REG

**4.2.6.1** XNORc

**4.2.6.2** XNORe

**4.2.6.3** DFFm

**4.2.6.4** DFFn

**4.2.6.5** LSc

**4.3** MMD\_FEEDBACK\_LOGIC

**4.3.1** DLYk

**4.3.2** LSe

**4.3.3** DLYI

**4.3.4** DEMUXa

**4.4** DCO\_MMD\_BLOCK

**4.4.1** LC\_DCO

**4.4.1.1** VOLTAGE\_REGa

**4.4.1.1.1** BIASa

**4.4.1.1.1.1** AMPb

**4.4.1.1.2** AMPd

**4.4.1.2** VOLTAGE\_REGb

**4.4.1.2.1** AMPa

**4.4.1.2.2** DIVIDERa

**4.4.1.2.2.1** DECa

**4.4.1.3** ESD

**4.4.1.4** RC\_CNTL

- 4.4.1.5 DIVIDERb**
  - 4.4.1.5.1 DECb**
- 4.4.1.6 RC\_VARa**
- 4.4.1.7 OSCa\_ACTIVE\_CIRCUIT**
  - 4.4.1.7.1 CAPACITOR\_BANKa**
  - 4.4.1.7.2 CAPACITOR\_BANKb**
- 4.4.1.8 CAPACITOR\_BANKc**
  - 4.4.1.8.1 CAP\_CELLa**
  - 4.4.1.8.2 CAP\_CELLc**
  - 4.4.1.8.3 CAP\_CELLb**
  - 4.4.1.8.4 CAP\_CELLd**
  - 4.4.1.8.5 CAP\_CELLE**
  - 4.4.1.8.6 CAP\_CELLf**
- 4.4.1.9 SQW\_CONV\_BLOCK**
  - 4.4.1.9.1 SQW\_CONVa**
  - 4.4.1.9.2 SQW\_CONVb**
- 4.4.2 CLOCK\_DIVIDER**
  - 4.4.2.1 XNORb**
  - 4.4.2.2 DFFb**
  - 4.4.2.3 MUXa**
  - 4.4.2.4 TWO\_CH\_SHFT\_REG**
    - 4.4.2.4.1 DFFa**
  - 4.4.2.5 TSPC\_DIVa**
  - 4.4.2.6 DFFc**
  - 4.4.2.7 XORa**
  - 4.4.2.8 CLOCK\_DIVIDERa**
    - 4.4.2.8.1 DFFf**
  - 4.4.2.9 DFFd**
  - 4.4.2.10 DFFe**
- 4.4.3 MULTIMODULUS\_CLOCK\_DIVIDER**
  - 4.4.3.1 MMD\_CNTL**
    - 4.4.3.1.1 XORc**
    - 4.4.3.1.2 DFFj**
  - 4.4.3.2 TSPC\_DIVb**
  - 4.4.3.3 MMD\_STGc**
    - 4.4.3.3.1 NAND2b**
    - 4.4.3.3.2 NAND3a**



- 4.4.3.3.3 DFFk
- 4.4.3.4 MMD\_STGb
  - 4.4.3.4.1 NAND2a
  - 4.4.3.4.2 DFFh
- 4.4.3.5 MMD\_STGa
  - 4.4.3.5.1 MUXb
- 4.4.3.6 MUXd
- 4.4.3.7 MMD\_OU\_LOGIC
  - 4.4.3.7.1 DLYc
    - 4.4.3.7.1.1 INVa
  - 4.4.3.7.2 XORb
  - 4.4.3.7.3 MUXc

## 5.0 GNSS Block Diagram

**Figure 5.0** Die photo with GNSS section marked (Active layer)

**Figure 5.1** Layout of GNSS section with analyzed blocks marked (Active layer)

**Figure 5.2** Layout of 5.0 GNSS\_BLOCK\_DIAGRAM (Active layer)

**Figure 5.3** Layout of inductor L1 of schematic 5.1 GNSS\_LNA (Metal 7 layer)

### 5.0 GNSS\_BLOCK\_DIAGRAM

#### 5.1 GNSS\_LNA

- 5.1.1 VREF\_SRC
- 5.1.2 BIAS\_SRCa
  - 5.1.2.1 BIAS\_SRCa\_CNTL
- 5.1.3 BIAS\_SRCb
  - 5.1.3.1 IREF\_SRCa
    - 5.1.3.1.1 VAR\_RES
- 5.1.4 AMP\_CNTL
- 5.1.5 ESDa
- 5.1.6 ESDb
- 5.1.7 AMPa
- 5.1.8 PMOSa
- 5.1.9 NMOSa
- 5.1.10 TST\_SWa

#### 5.2 GNSS\_MIXER

- 5.2.1 MX\_REF\_SRC
- 5.2.2 TST\_SWb

#### 5.3 LO\_GENERATOR

## Appendix

**A.1** Symbol Conventions

**A.2** Transistor Parameters Definition

**A.3** Logic Gates Parameters Definition

**A.4** Resistor Parameters Definition

**A.5** Connection of Groups of Elements

**A.6** Logic Gates Power Supply and Substrate Connection Definition

**A.7** Signal Annotations

**A.8** Capacitor Structures

**A.9** Symbol Definitions

# Device Summary Sheet

**Manufacturer:** Intel Corporation

**Part Number:** 

**Date Code:** 

**IC Type:** RF Transceiver

## Technology synopsis

**Package Type:** WLCSP

**Pin Count:** 249

**Package Size:** 6 mm x 6 mm x 0,4 mm

**Die Count:** 1

**Die Size:** 6,06 mm x 5,96 mm (by edge of physical silicon)  
6,04 mm x 5,94 mm (by edge of seal)

**Number of Metal Layers:** 8. One layer of aluminum interconnect, seven layers of copper interconnect

**Gate Layer:** One layer of metal gates

**Minimum Printed Gate Length<sup>1</sup>:** 41 nm

**Device Isolation Type:** STI

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<sup>1</sup> Measured feature sizes are accurate within 10%

# Source Device



Figure 0.1 Apple iPhone frame with detached display assembly and battery



Figure 0.2 Apple iPhone back side



**Figure 0.3** Apple [redacted] iPhone [redacted] main PCB assembly (side A)



**Figure 0.4** Apple [redacted] iPhone [redacted] main PCB assembly (side B)



**Figure 0.5** Apple [redacted] iPhone [redacted] main PCB-I (side A)



**Figure 0.6** Apple [redacted] iPhone [redacted] main PCB-I (side B)





**Figure 0.7** Apple iPhone main PCB-II (side A)

Intel Transceiver



**Figure 0.8** Apple [redacted] iPhone [redacted] main PCB-II (side B)

# Package and Die



Figure 0.9 Intel  Transceiver package top

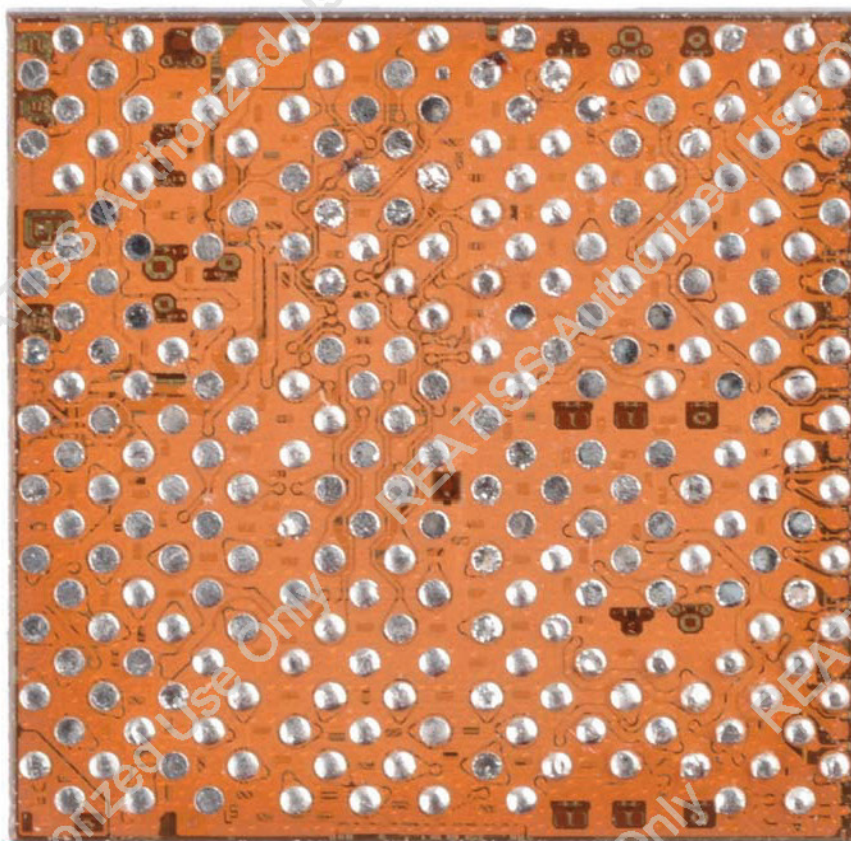



Figure 0.10 Intel  Transceiver package bottom



**Figure 0.11** Intel  Transceiver package bottom with balls marked

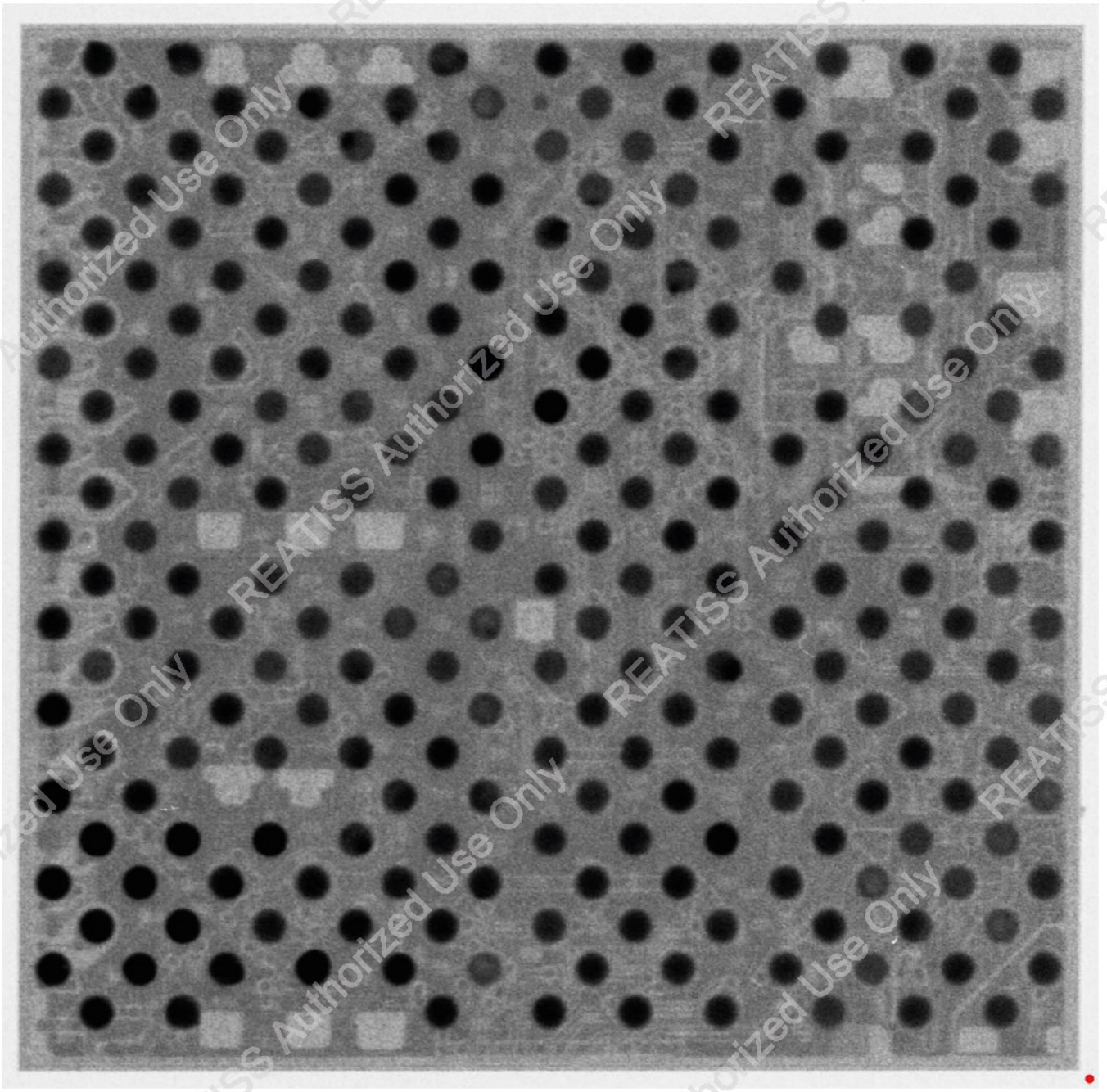
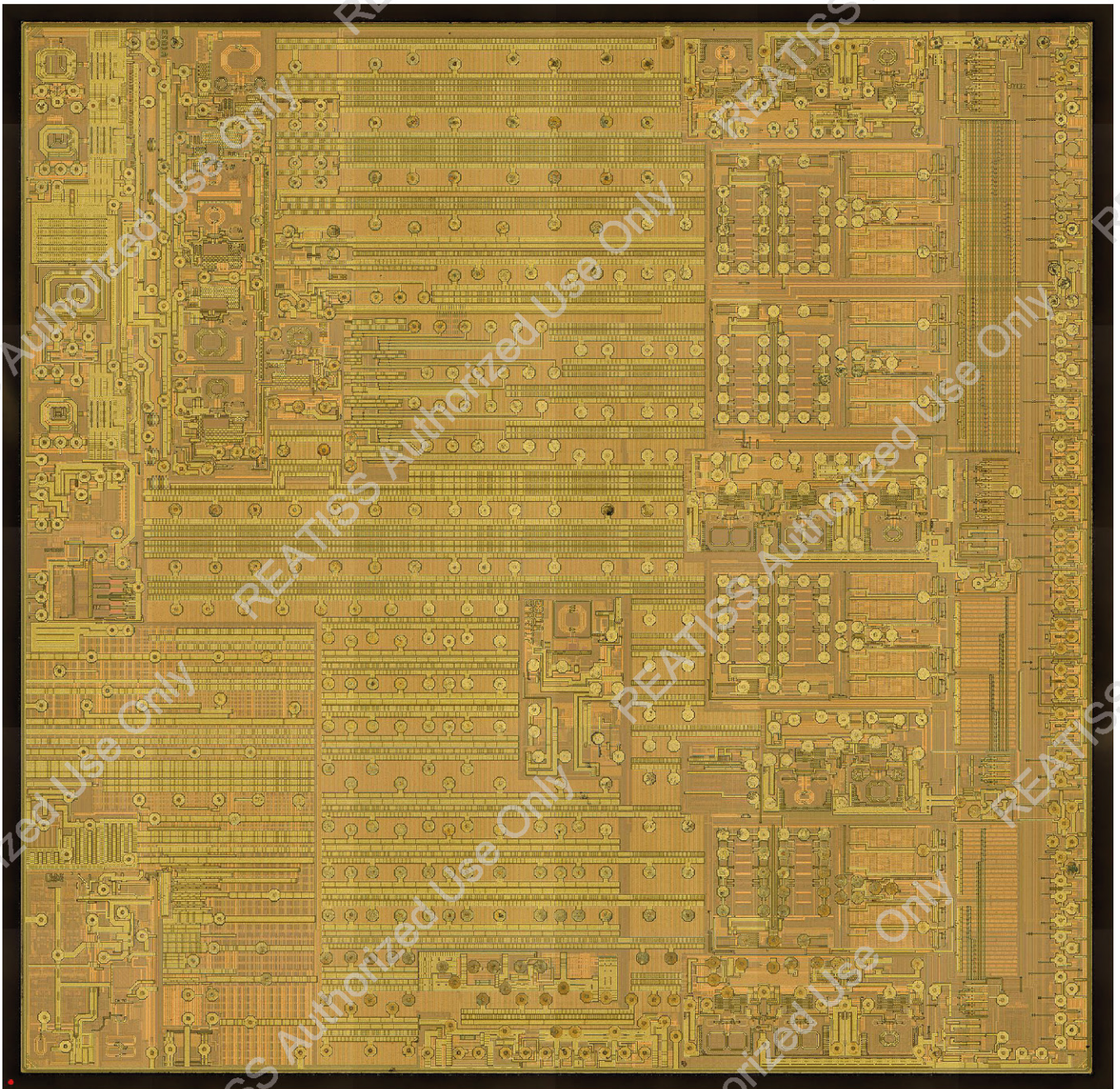


Figure 0.12 Intel  Transceiver package X-ray



**Figure 0.13** Die photo (top metal)



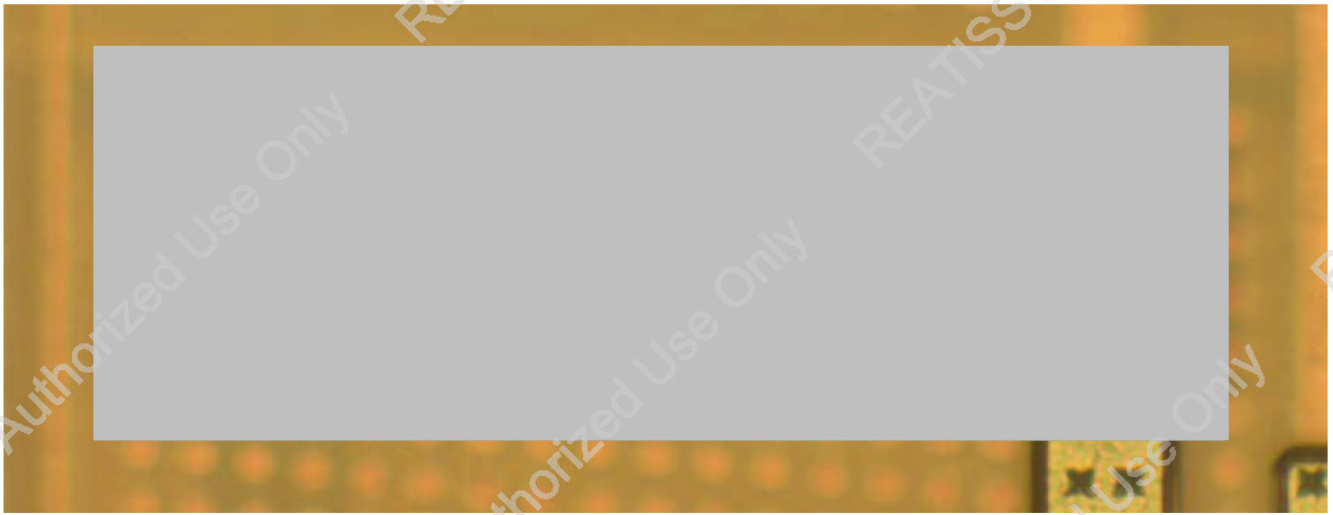
Figure 0.14 Die markings A



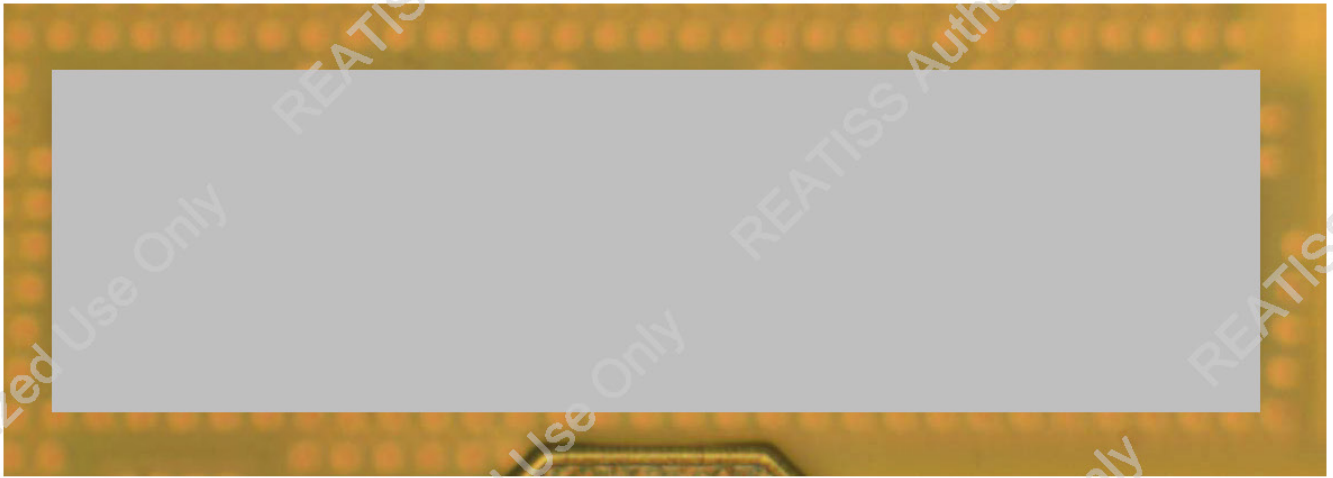
Figure 0.15 Die markings B



Figure 0.16 Die markings C



**Figure 0.17** Die markings D



**Figure 0.18** Die markings E





Figure 0.19 Die photo (Active layer)

# Die Functional Blocks

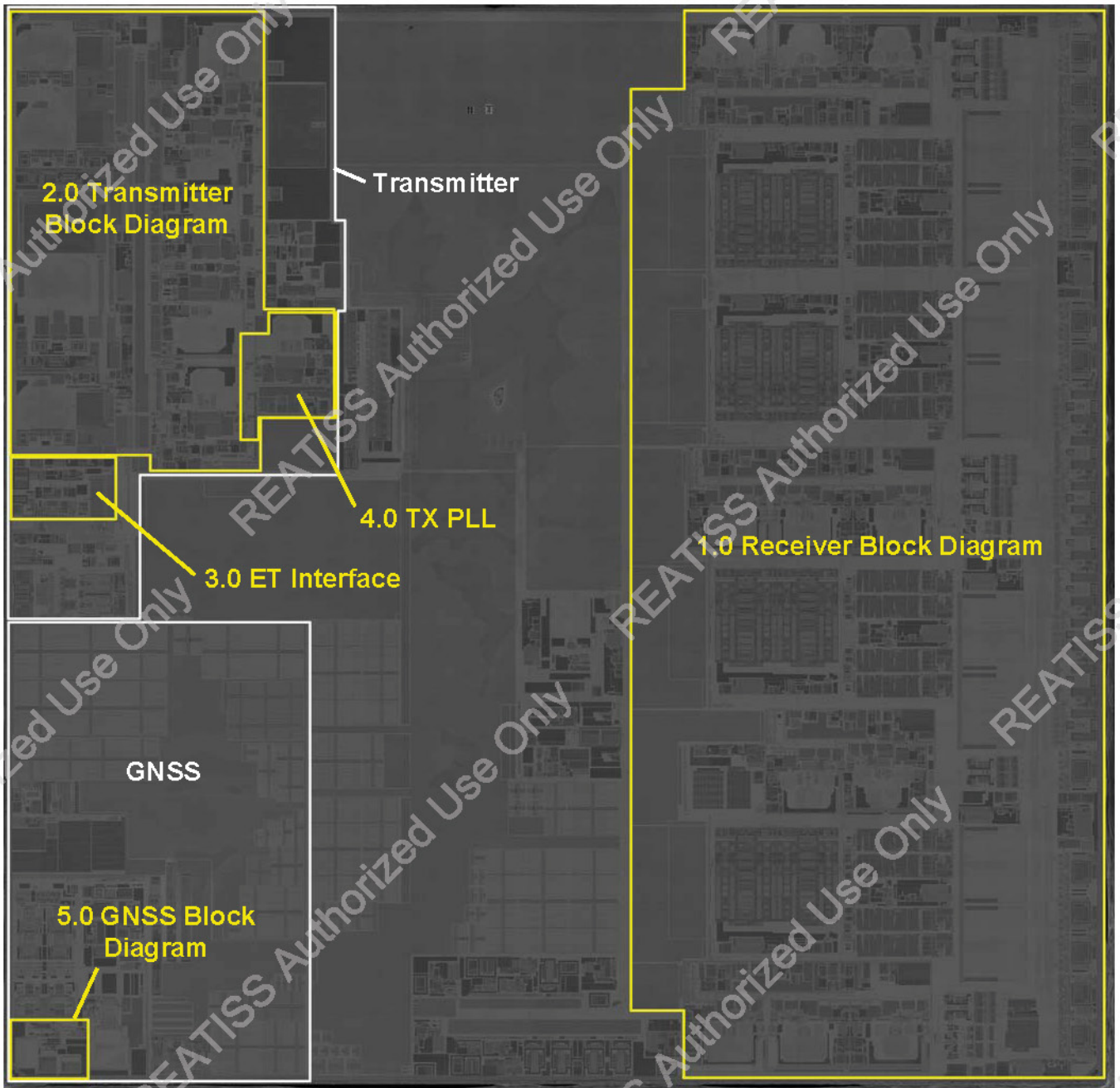


Figure 0.20 Intel Transceiver die functional blocks (Active layer)

# 1.0 Receiver Block Diagram



Figure 1.0 Layout of 1.0 RECEIVER\_BLOCK\_DIAGRAM (RDL2 layer)



**Figure 1.1** Layout of 1.0 RECEIVER\_BLOCK\_DIAGRAM (Active layer)

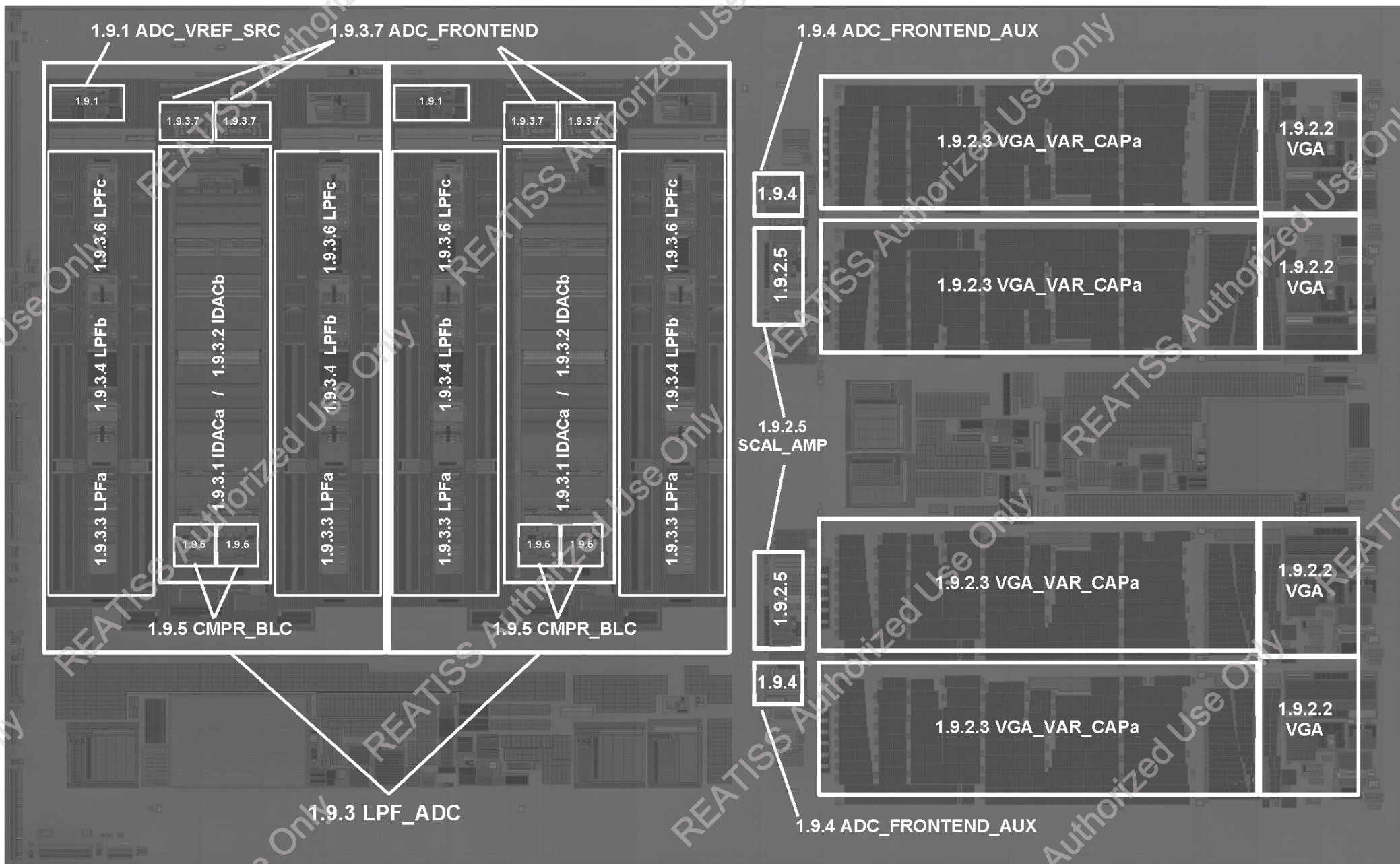
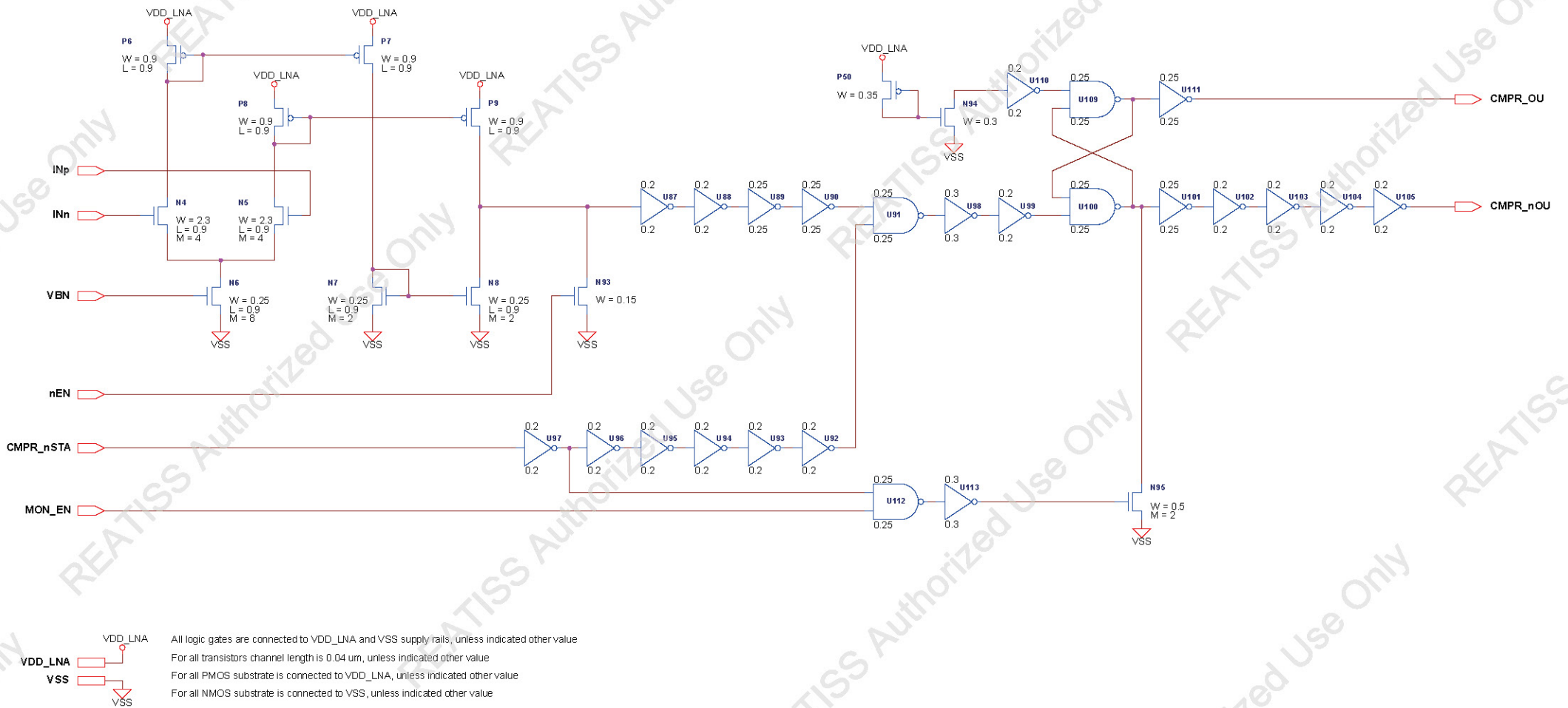


Figure 1.2 Layout of 1.9 RX\_ADC (Gate layer)





### 1.1.1.5.3 CMPRa

Comparator A





## 2.0 Transmitter Block Diagram

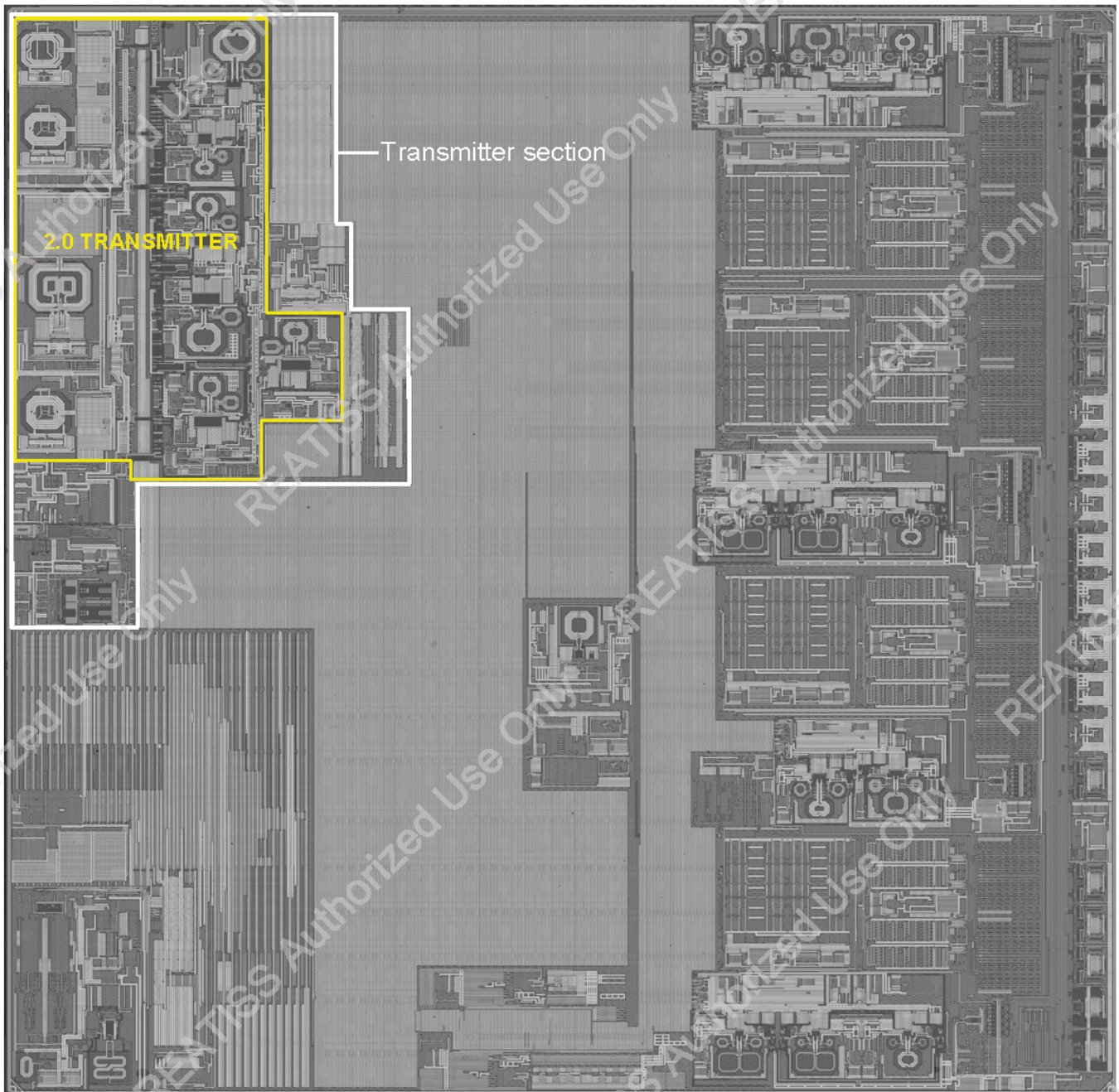


Figure 2.0 Die photo with Transmitter section and Transmitter block marked (Metal 7 layer)



**Figure 2.1** Layout of Transmitter section with analyzed blocks marked<sup>2</sup> (Active layer)

<sup>2</sup> Analyzed blocks highlighted in yellow

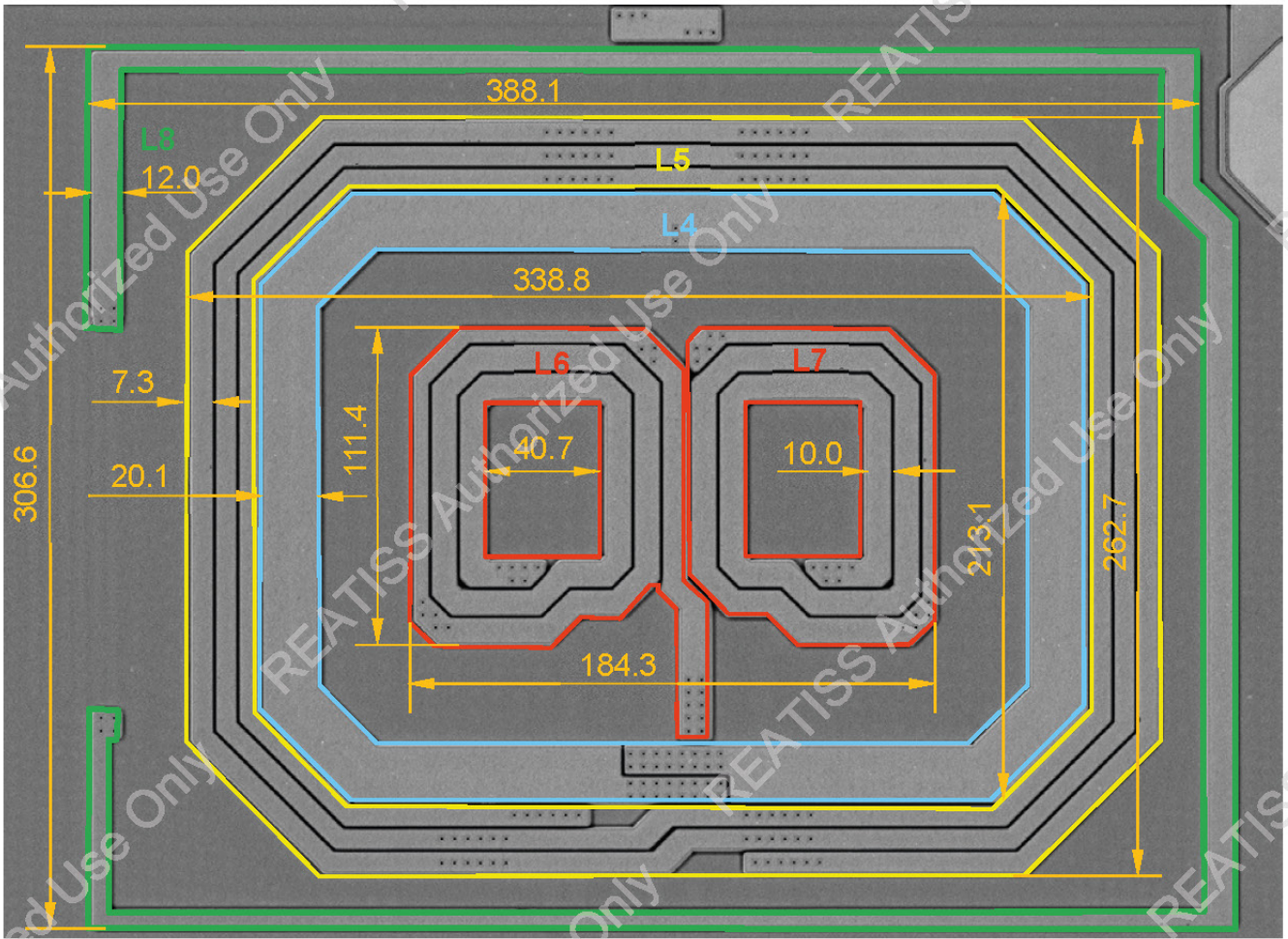
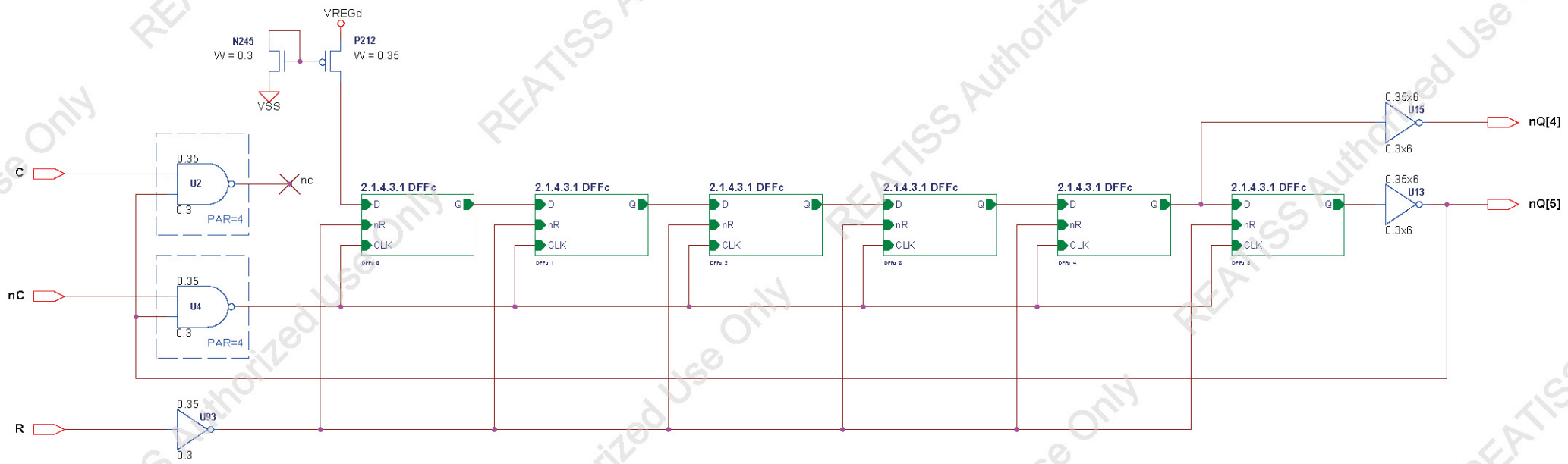




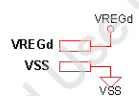
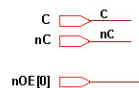
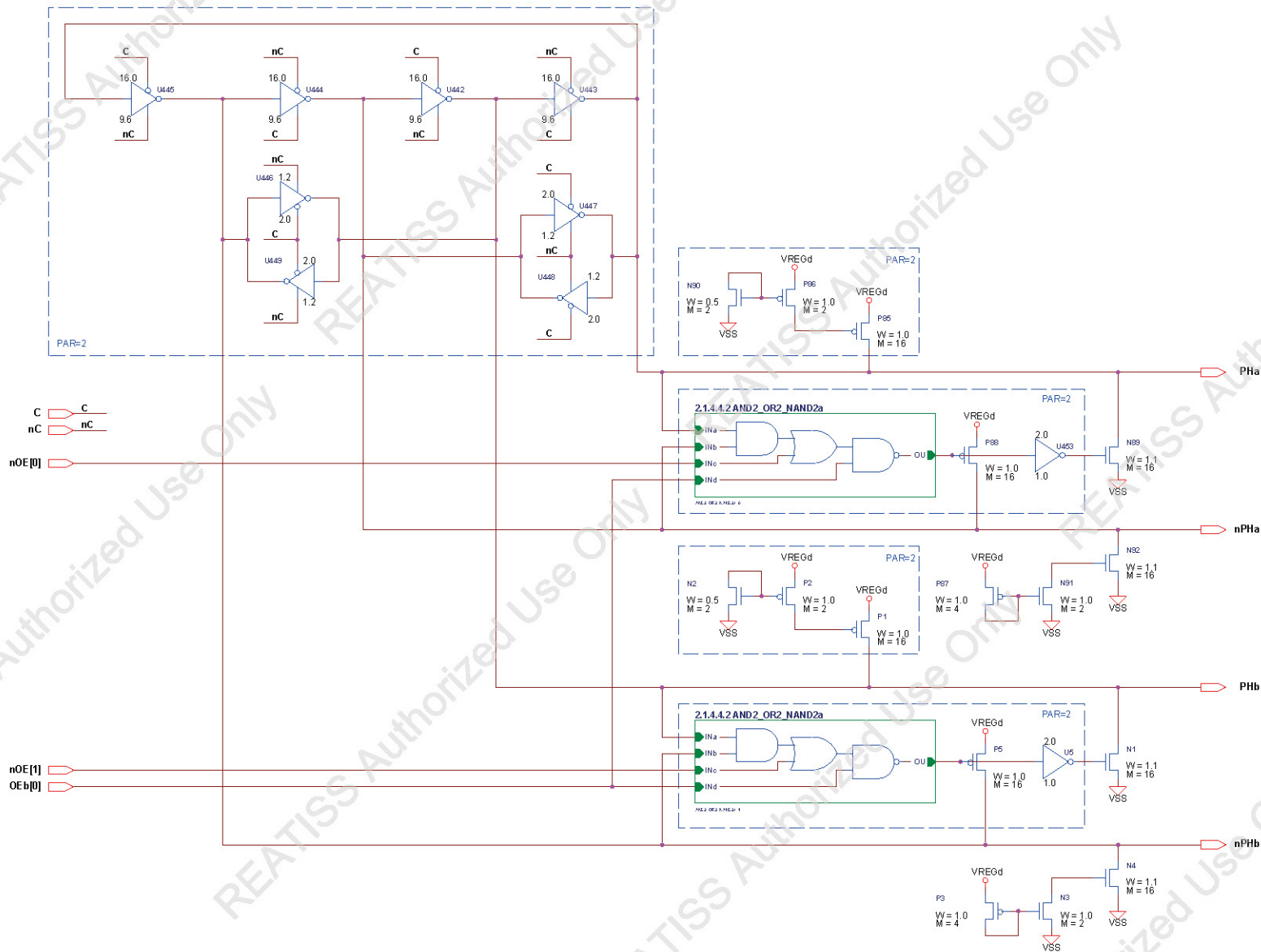
Figure 2.5 Layout of inductors L4, L5, L6, L7 and L8 of schematic 2.6 TRANSFORMERc (Metal 8 layer)



 VREGd  
 VSS

All logic gates are connected to VREGd and VSS supply rails, unless indicated other value  
 For all transistors channel length is 0.04 um, unless indicated other value  
 For all PMOS substrate is connected to VREGd, unless indicated other value  
 For all NMOS substrate is connected to VSS, unless indicated other value

**2.1.4.3 SHIFT\_RGa**  
Shift Register A



All logic gates are connected to VREGd and VSS supply rails, unless indicated other value  
 For all transistors channel length is 0.04 um, unless indicated other value  
 For all PMOS substrate is connected to VREGd, unless indicated other value  
 For all NMOS substrate is connected to VSS, unless indicated other value

**2.1.6.5 PH\_SPLITTERf**

Phase Splitter F

### 3.0 ET Interface

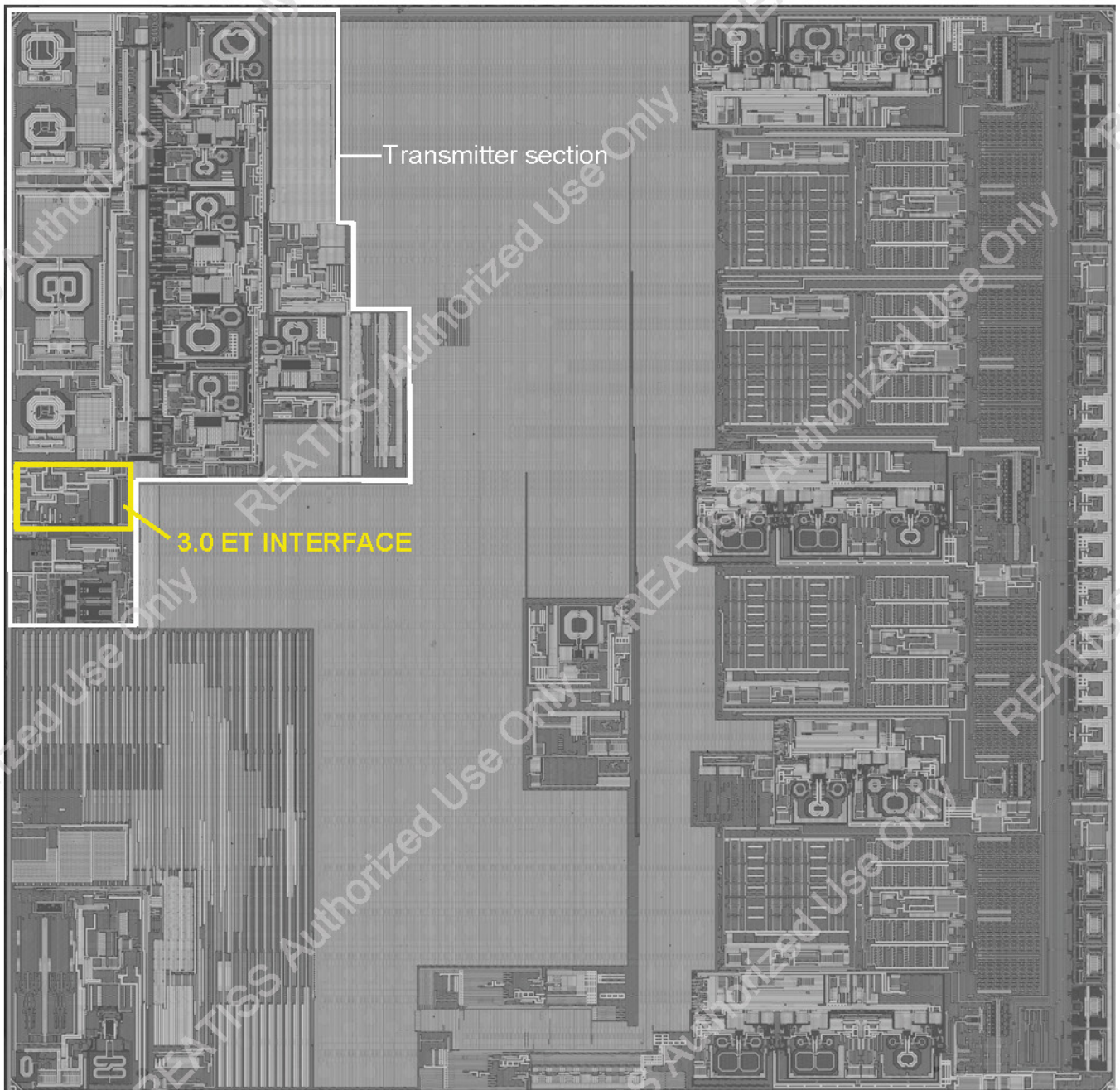
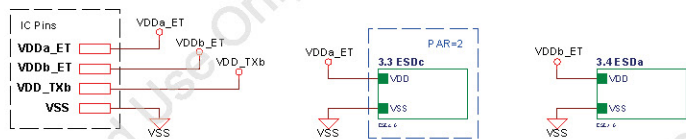
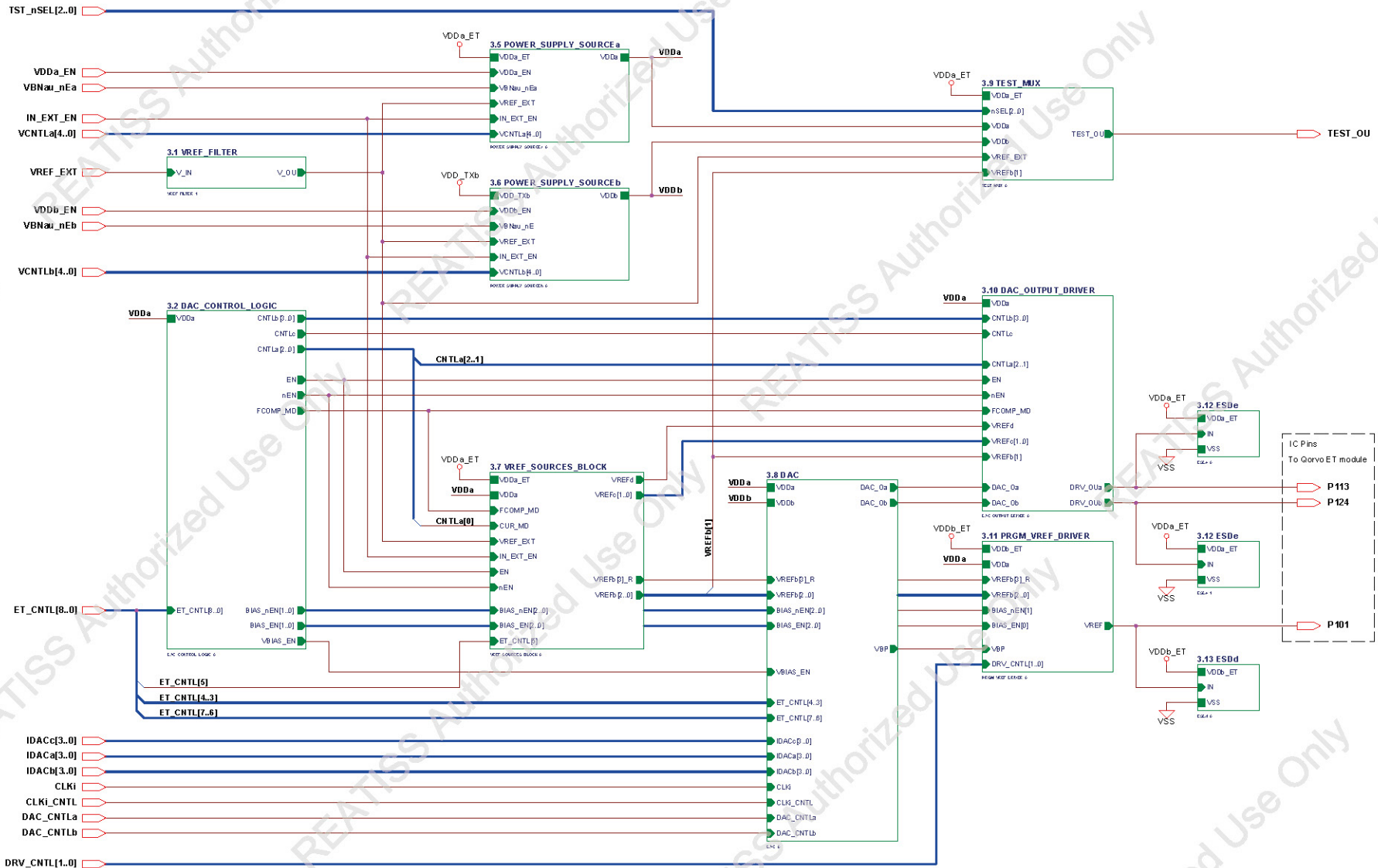


Figure 3.0 Die photo with Transmitter section and ET Interface block marked (Metal 7 layer)



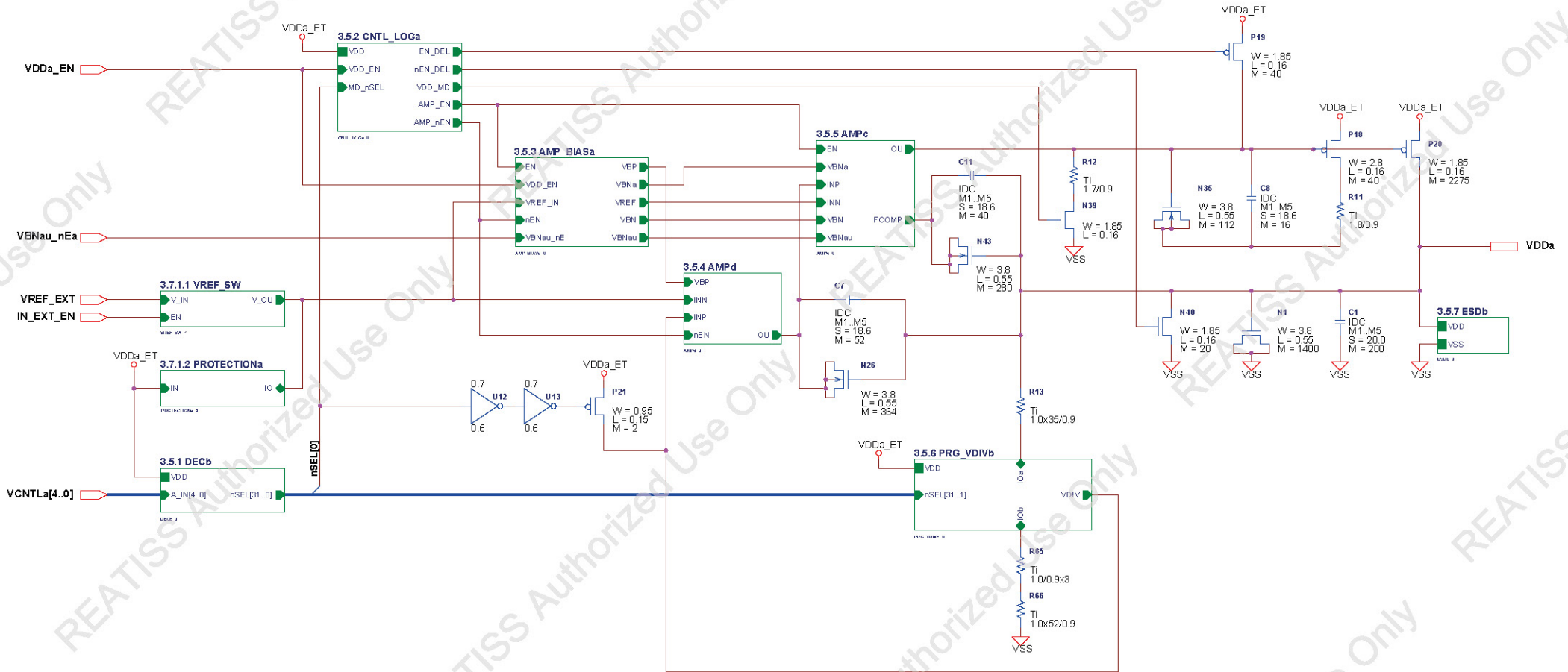
**Figure 3.1** Layout of ET Interface block with analyzed blocks marked (Metal 1 layer)



### 3.0 ET\_INTERFACE

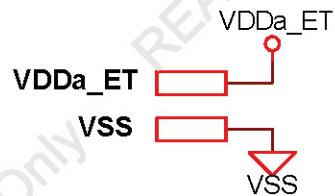
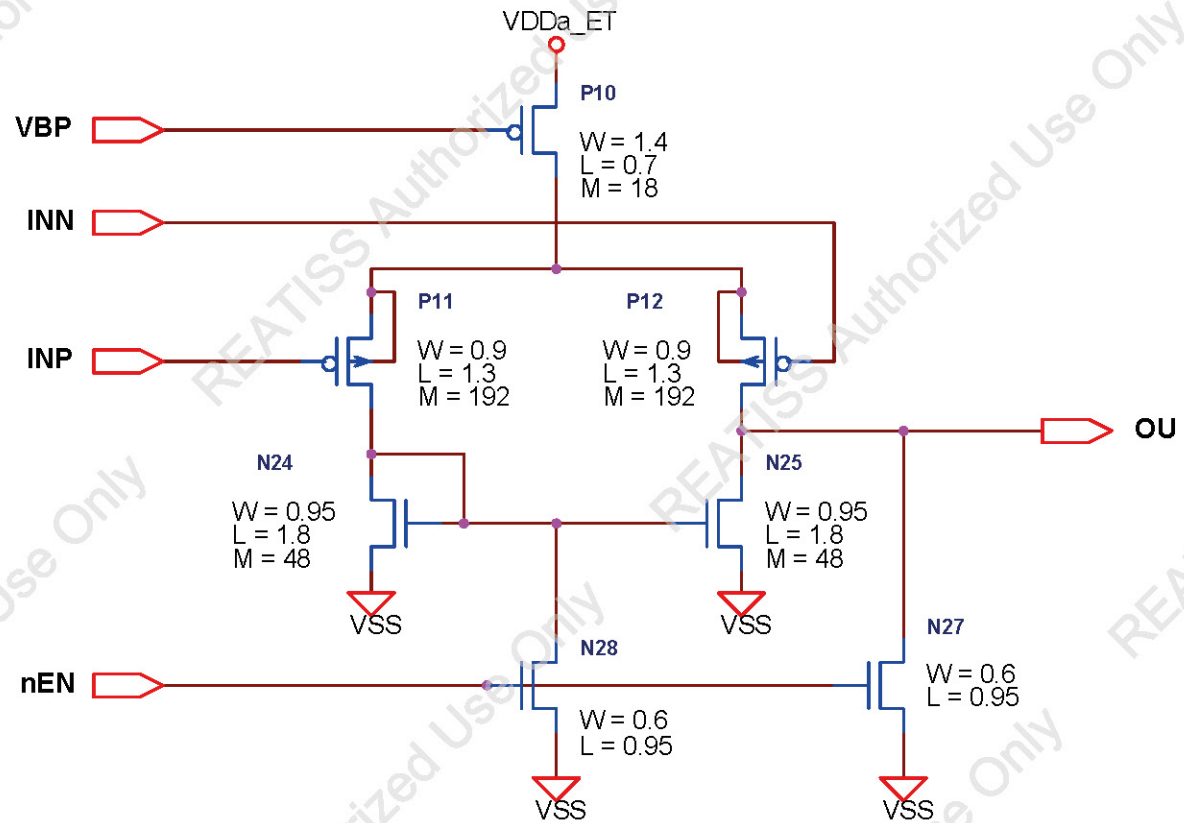
Envelope Tracker Interface. A Part of Circuits.





VDDa\_ET All logic gates are connected to VDDa\_ET and VSS supply rails, unless indicated other value  
 VDDa\_ET For all transistors channel length is 0.15 um, unless indicated other value  
 VSS For all PMOS substrate is connected to VDDa\_ET, unless indicated other value  
 VSS For all NMOS substrate is connected to VSS, unless indicated other value

### 3.5 POWER\_SUPPLY\_SOURCEa



For all PMOS substrate is connected to VDDa\_ET, unless indicated other value  
 For all NMOS substrate is connected to VSS, unless indicated other value

### 3.5.4 AMPd Amplifier D

# 5.0 GNSS Block Diagram



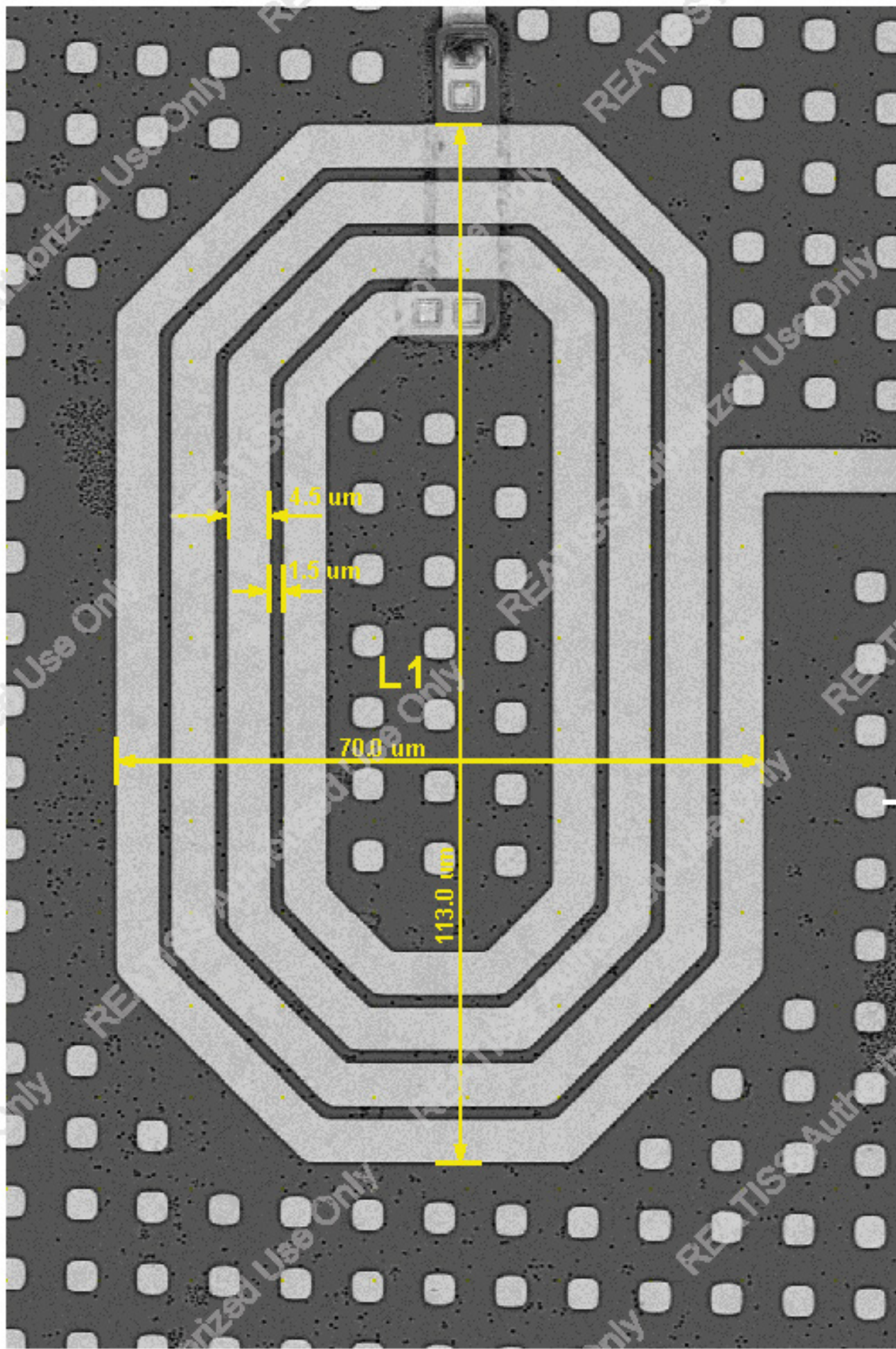
Figure 5.0 Die photo with GNSS section marked (Active layer)



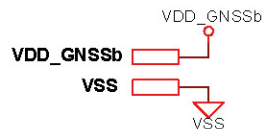
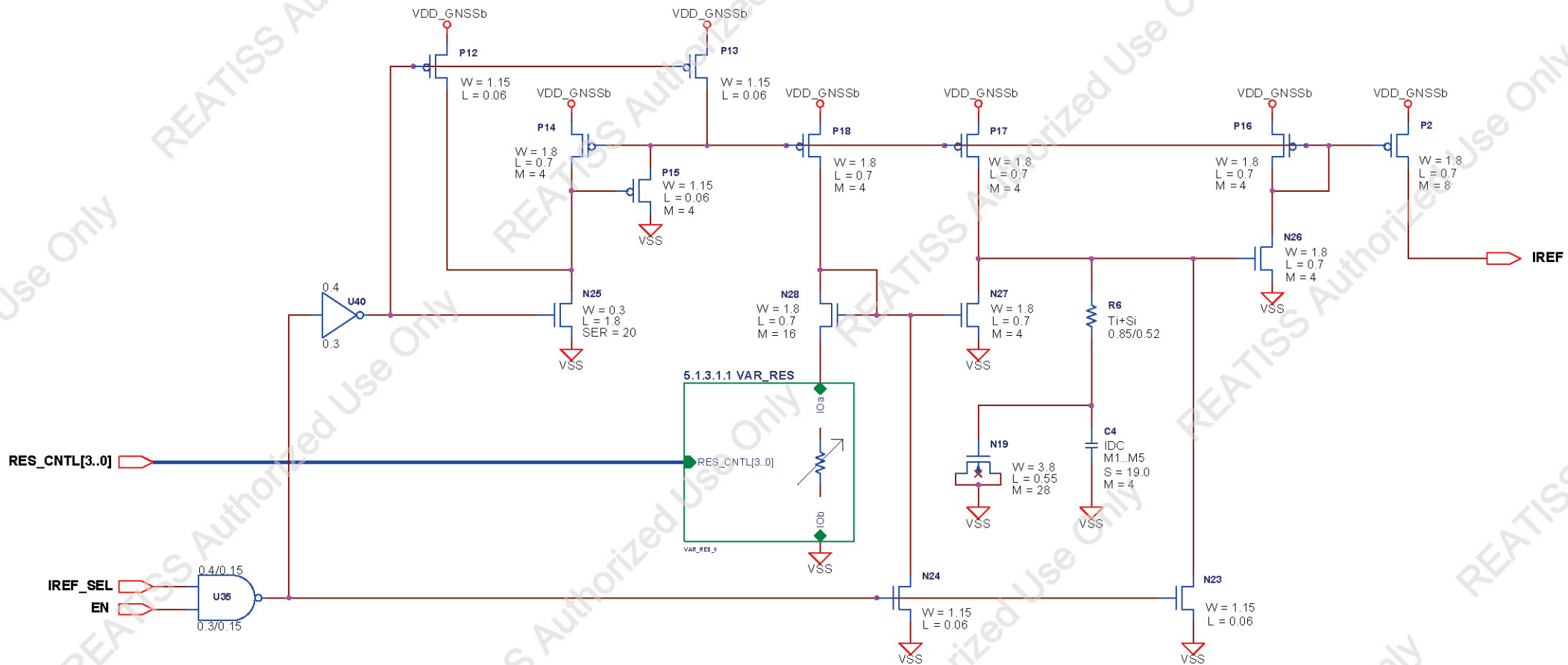
Figure 5.1 Layout of GNSS section with analyzed blocks marked (Active layer)



**Figure 5.2** Layout of 5.0 GNSS\_BLOCK\_DIAGRAM (Active layer)

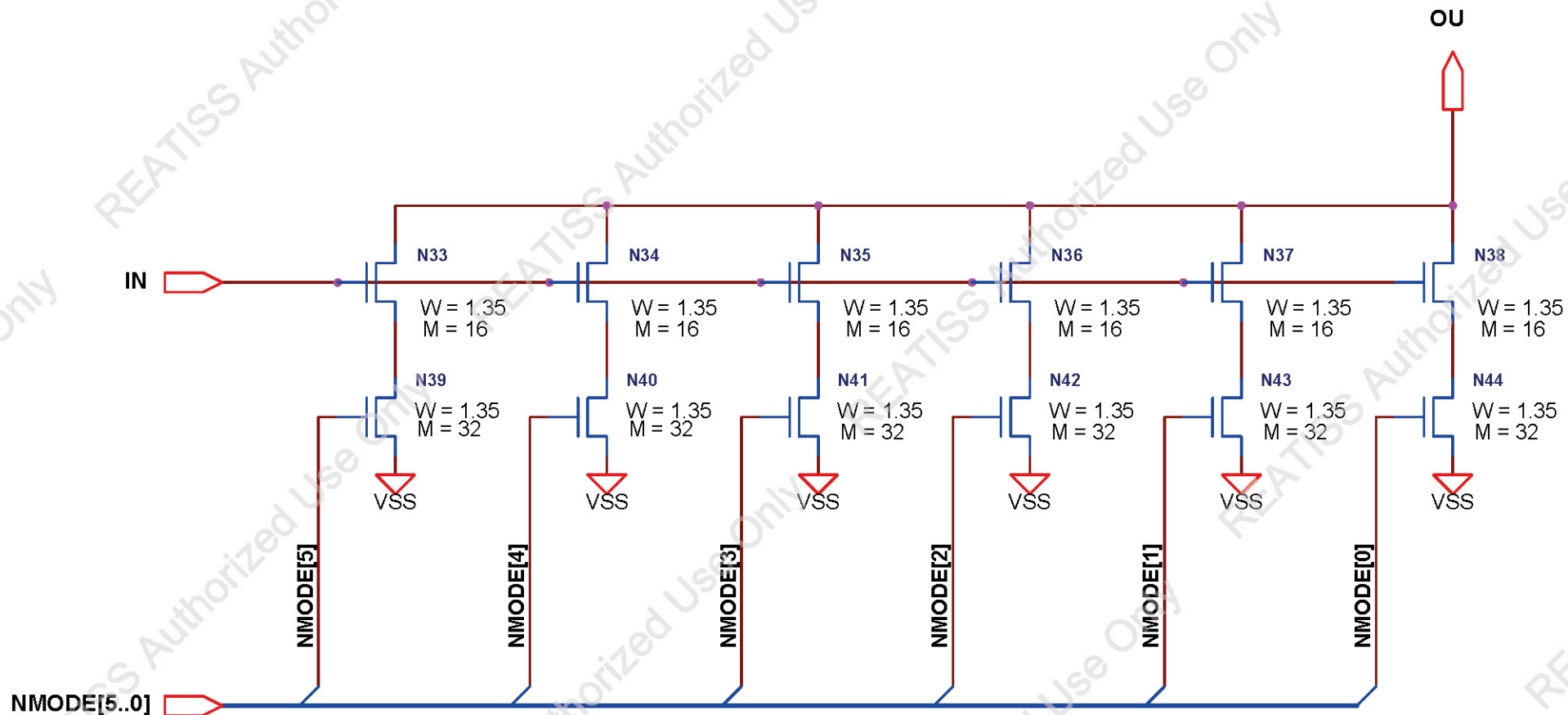


**Figure 5.3** Layout of inductor L1 of schematic 5.1 GNSS\_LNA (Metal 7 layer)



All logic gates are connected to VDD\_GNSSb and VSS supply rails, unless indicated other value  
 For all PMOS substrate is connected to VDD\_GNSSb, unless indicated other value  
 For all NMOS substrate is connected to VSS, unless indicated other value

### 5.1.3.1 IREF\_SRCa Reference Current Source A

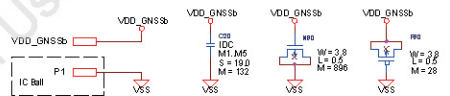
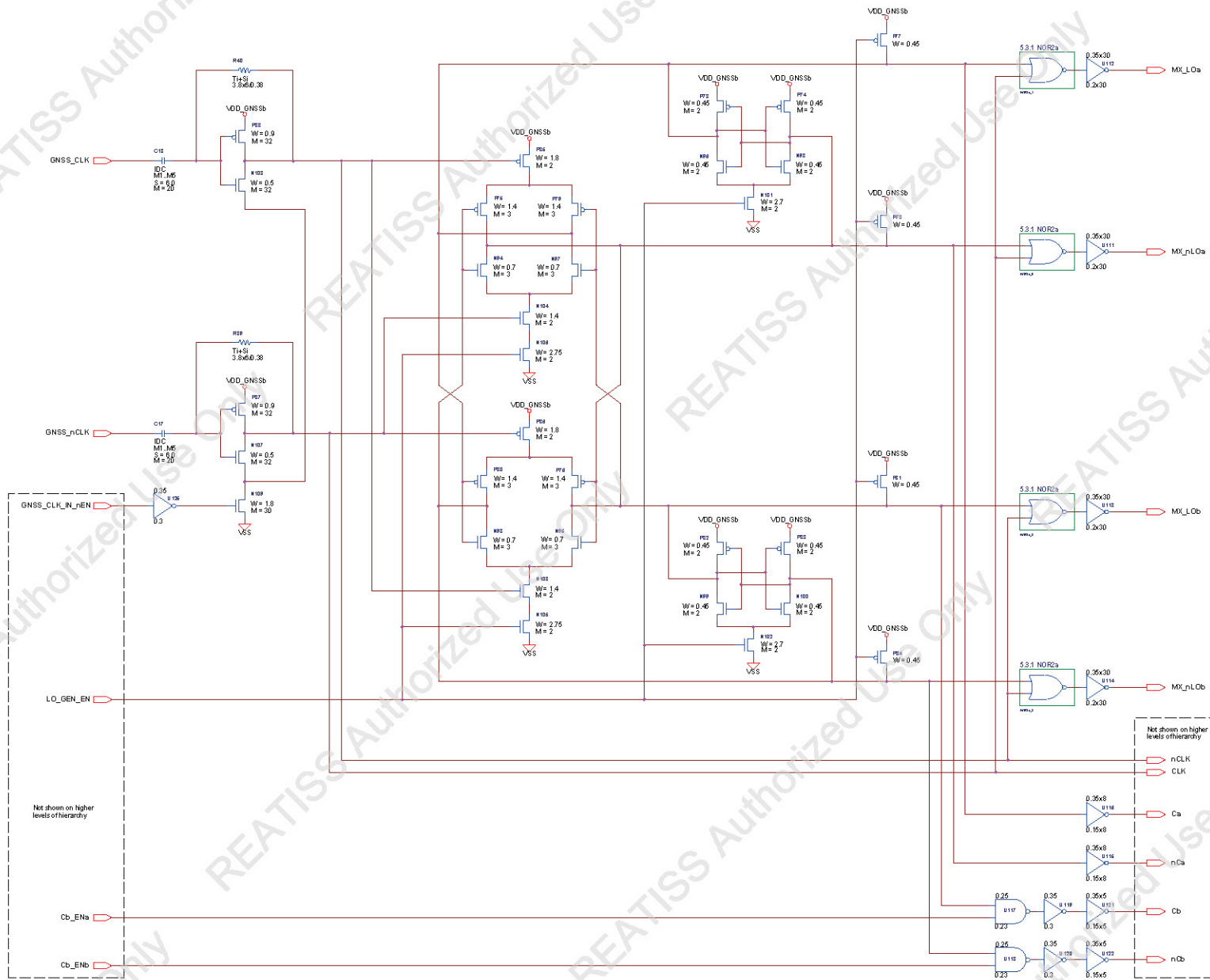


For all transistors channel length is 0.06  $\mu\text{m}$ , unless indicated other value  
 For all NMOS substrate is connected to VSS, unless indicated other value

### 5.1.9 NMOSa

#### Programmable NMOS Stack A





/All logic gates are connected to VDD\_GNSSb and VSS supply rails, unless indicated other value  
 For all transistors channel length is 0.03 um, unless indicated other value  
 For all PMOS substrate is connected to VDD\_GNSSb, unless indicated other value  
 For all NMOS substrate is connected to VSS, unless indicated other value

5.3 LO\_GENERATOR